Analog Electronics

UNIT-I

SINGLE STAGE AND MULTISTAGE AMPLIFIERS

1) Amplifier:

A amplifier is a circuit which increases the strength or weak signal.

2) CLASSIFICATION OF AMPLIFIER

1) CLASSIFICATION BASED ON FREQUENCY.

1) DC amplifier

2) audio amplifier (20 hz to 20khz)

3) video amplifier (few mhz)

4) radio frequency amplifier (khz to 20 mhz)

5) ultra high frequency (GHZ)

2) CLASSIFICATION BASED ON OPERATION.

1) CLASS A (Conduction angle 0 to 360^0)

2) CLASS B (conduction angle 0 to 180^0)

3) C LASS c (Conduction angle < 180^0)

4) CLASS AB (conduction angle grater than 180^0 & lesser than 360^0

3) CLASSIFICATION BASED ON COUPLING

1) RC coupling

2) Transformer coupling

3) Direct coupling

4) CLASSIFICATION BASED ON LOAD

1) resistive

2) inductive

5) CLASSIFICATION BASED ON APPLICATION

1) VOLTAGE AMPLIFIER

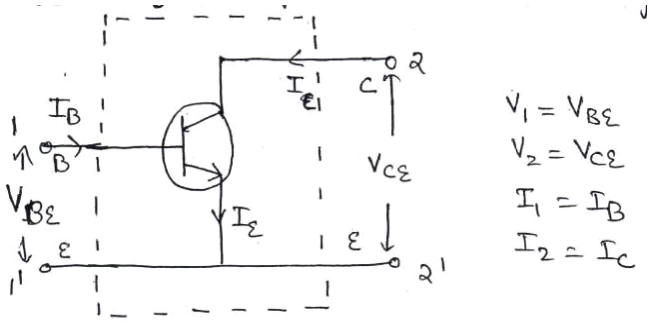
2) CURRENT AMPLIFIER

3) POWER AMPLIFIER

4) TUNED AMPLIFIER

TRANSISTOR HYBRID MODEL

1) consider a BJT as two part device (ce configuration)



h - parameter equations

$V_1 = h_{11} I_1 + h_{12} V_2$

$I_2 = h_{21} I_1 + h_{22} V_2$

For CE configuration

$V_{BE} = h_{ie} I_B + h_{re} V_{ce}$

$I_C = h_{fe} I_B + h_{oe} V_{ce}$

Short circuit port 22^1, $V_{ce} = 0$

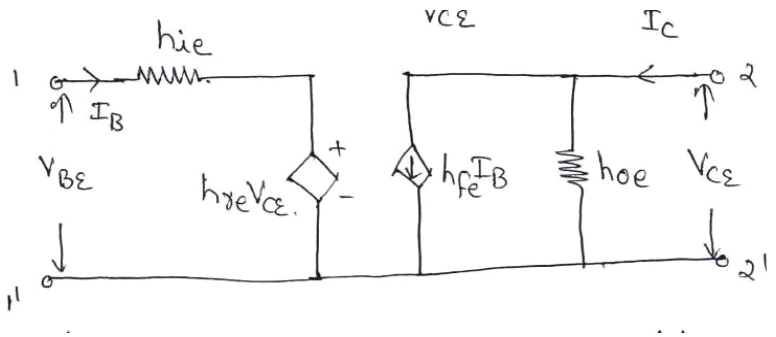
Input impendence h_{ie} =

Forward current gain h_{fe} =

Open circuit port 11^1, $I_B = 0$

Reverse voltage gain h_{re} =

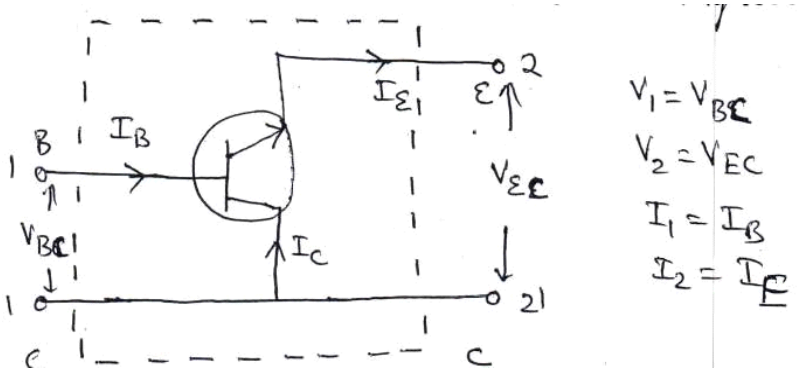
Output admittance h_{oe} =



Exact h- parameter small signal model

2) COMMON COLLECTOR CONFIGURATION

1) Consider a BJT as two port device (cc configuration)



H – Parameter equations

$V_1 = h_{11} I_1 + h_{12} V_2$

$I_2 = h_{21} I_1 + h_{22} V_2$

For cc configuration

$V_{BC} = h_{ie} I_b + Vh_{rc} V_{EC}$

$-I_E = h_{fc} I_B + h_{oc} V_{EC}$

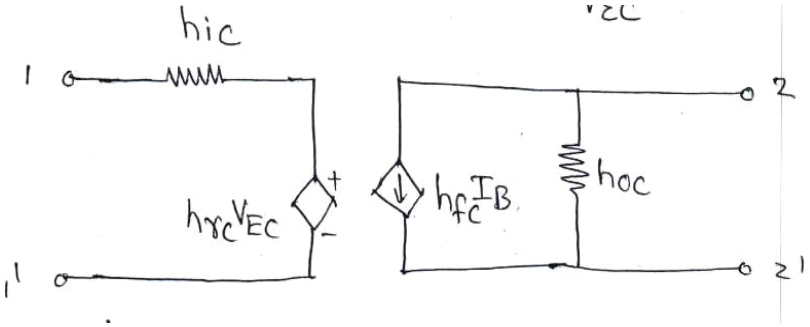
Short circuit port 22^1 $V_{EC} = 0$

Input impendence h_{ic} =

Forward circuit gain h_{fe} =

Open circuit port 11^1 = 0

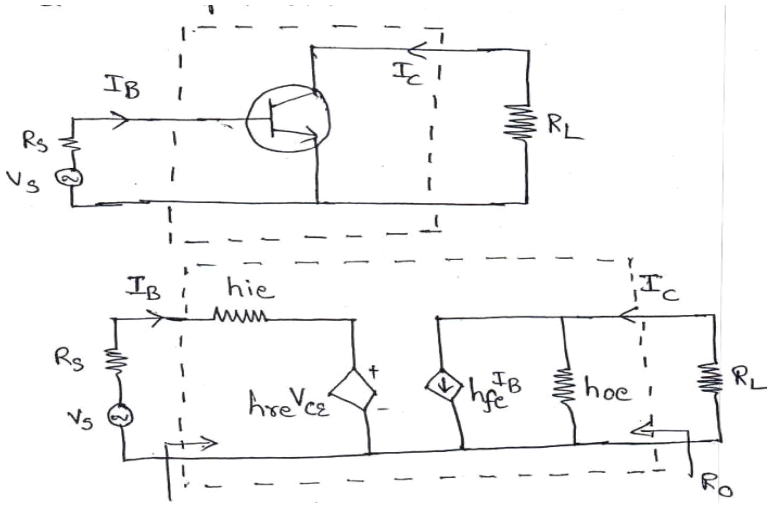
Reverse voltage gain h_{rc} =



Output admittance h_{oc} =

4) CE SINGLE STAGE AMPLITIER WITH R_S & R_L

1) Consider CE amplifiers



$V_{BE} = h_{ie} I_B + h_{re} V_{CE}$

$I_C = h_{fe} I_B + h_{oe} V_{CE}$

2) A.C analysis

1) Current gain

$A_I = =$

$I_C = h_{fe} I_B + h_{oe} V_{CE}$

I_B

$= h_{fe} + h_{oe}$

$= h_{fe} + h_{oe}$

$[\ 1 + h_{oe} R_L\ ] = h_{fe}$

=

A_I = =

2) INPUT IMPENDENCE

R_i = =

Consider equation (1)

$V_{BE} = h_{ie} I_B + h_{re} V_{CE}$

$V_{BE} = h_{ie} I_B + h_{re}$ (-)

= $h_{ie} I_B + h_{re}$ (-)

R_i = = $h_{ie} + h_{re} A_I . R_{L.}$

3) VOLTAGE GAIN

A_v = = =

I_B

=

A_v =

4) OUTPUT ADMITTANCE

Y_0 = =

= $h_{fe} I_B + h_{oe} V_{CE}$

V_{CE}

= h_{fe} + h_{oe}

Consider input 100p (KVL)

$V_s - I_B R_S - I_B h_{ie} – h_{re} V_{CE} = 0$

Let V_S = 0,

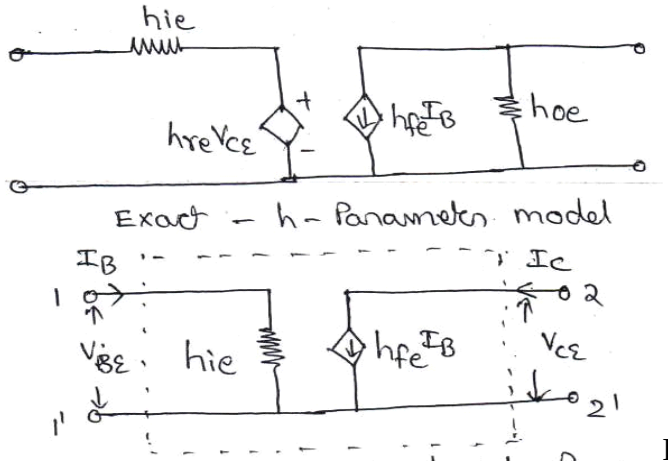
=

Using above equation

Output resistance R_0 =

3) SIMPLIFIED H- PARAMETER MODEL

In practice the voltage '$h_{re}\ V_{ce}$' is very less value when compared to $I_B\ h_{ie}$, hence $h_{re}\ V_{CE}$ is neglected similarly the load resistance R_L is selected minimum times lesser than (1/hoe) Ω, hence hoe is neglected.



By removing $h_{re}\ V_{CE}$ and h_{oe} simplified model is obtained. The approximate values are very near to the exact values.

Approximate h – parameter model

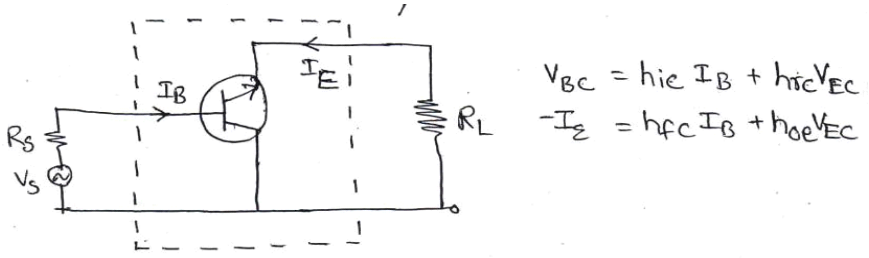
	EXACT	IMPLIFIED
1) Current gain	A_I =	A_I =
2) Input resistance	$R_i = h_{ie} + h_{re}\ A_I\ .\ R_{L.}$	$R_i = h_{ie}$

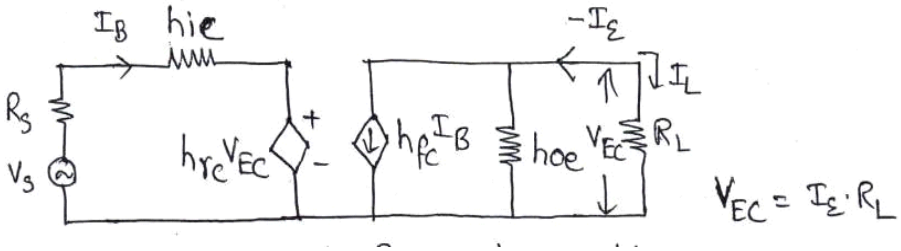
3) Voltage gain $A_v =$ $A_v =$

4) output admittance $Y_0 = h_{oe} -$ $Y_0 =$

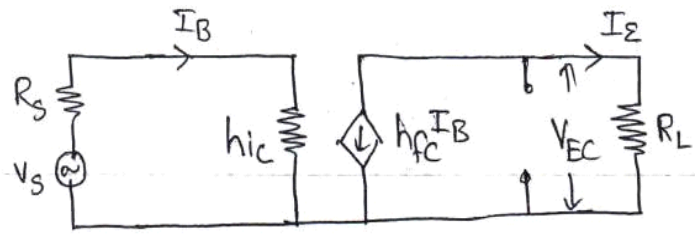
SIMPLIFIED C.C CONFIGURATION

1) consider common collector configuration





Exact – h- parameter model.



Simplified – h- parameter model.

2) CURRENT GAIN

$A_I = \ =$

$-I_E = h_{fc}\ I_B + h_{oe}\ V_{EC}$

$-I_E = h_{fc}\ I_B + h_{oe}\ I_E\ .\ R_L$

$-\ h_{fc}\ I_B = I_E + h_{oe}\ I_E\ .\ R_L$

$-\ h_{fc}\ I_B = I_E\ (1+ h_{oe}\ R_L)$

$A_I = \ = \qquad -\ h_{fc} \qquad = 1+ h_{fe}$

3) INPUT RESISTANCE

$R_i \ = \ =$

Consider eq (1) $V_{BC} = h_{ie}\ I_B + h_{re}\ V_{EC}$

$V_{BC} = h_{ic}\ I_B + h_{rc}\ V_{EC}$

I_B

$= h_{ic}\ I_B + h_{rc}$

$R_i \ = \ = h_{ic} + h_{re}\ A_I \qquad h_{ic} + 1.\ (1 + h_{fe})\ R_L$

3) VOLTAGE GAIN:

$A_V = \ = \ =$

I_B

Consider eq :

=

$A_{v\ =}$

$A_{v\ =}$

> >

Neglected

$A_v =$

$A_v = 1$

4) OUTPUT RESISTANCE

$R_0 = \quad =$

KVL to input loop

$$V_s - I_B R_S - I_B h_{ic} - h_{rc} V_{EC} = 0$$

Let $V_S = 0$,

$$- I_B R_S - I_B h_{ic} - 1. V_{EC} = 0$$

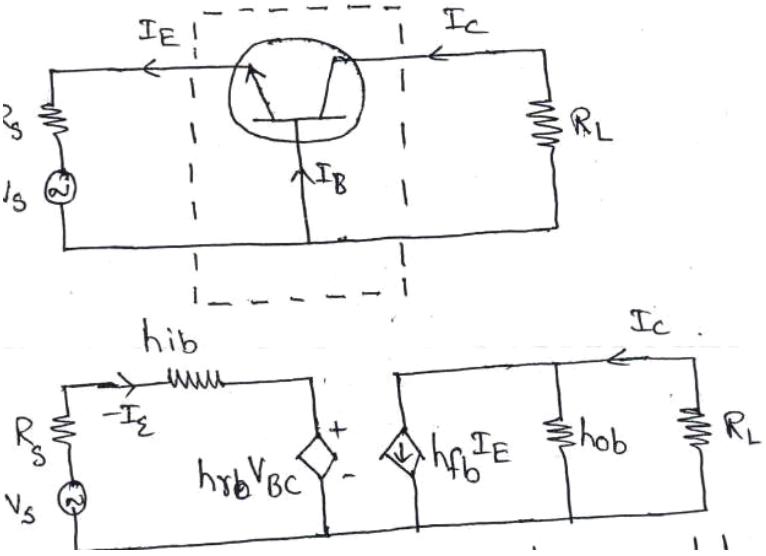
$$- V_{EC} = I_B (R_S + h_{ic})$$

$R_0 = \quad =$

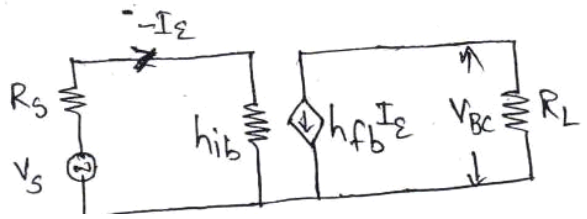
$R_0 =$

6) SIMPLIFIED CB CONFIGURATION.

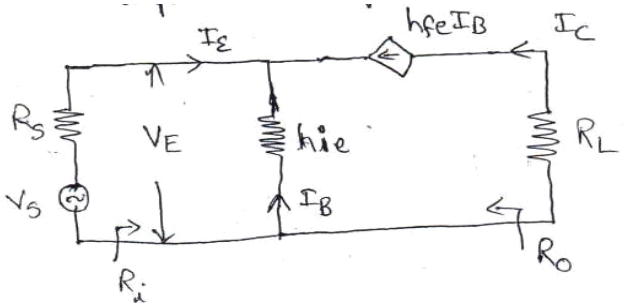
1) Consider CB configuration as shown below.



Exact – h- parameter model



Simplified hybrid model



1) current gain (A_I).

A_I = =

=

A_I 1

2) INPUT RESISTANCE (R_i)

R_i = = =

R_i =

3) VOLTAGE GAIN (A_V)

A_V = = =

A_V =

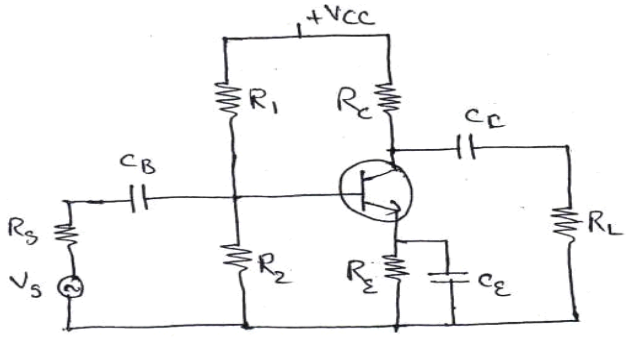
4) OUTPUT RESISTANCE (

= =

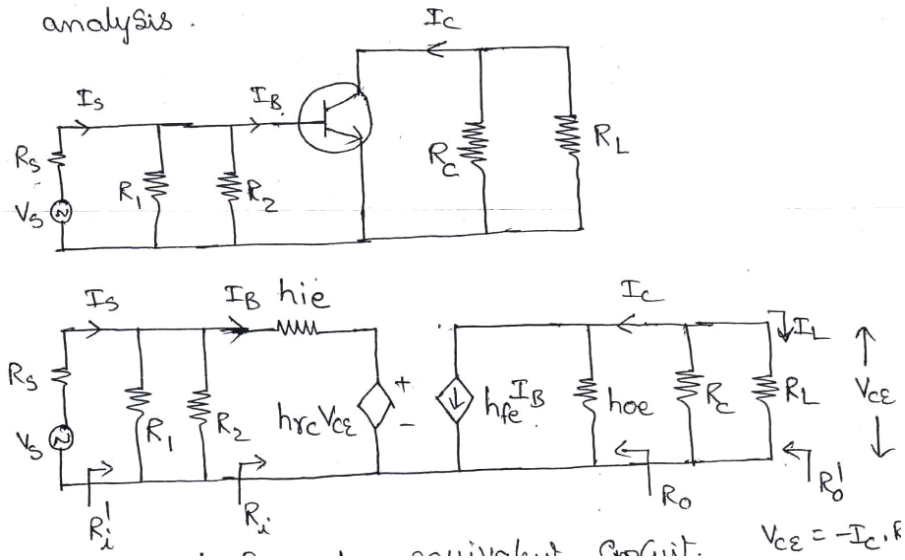
=

7)CE AMPLIFIER WITH R_E & CE (BY PASS CAPACITOR)

1) A single stage CE amplifier is shown blow.



2) A.C analysis



h- Parameter equivalent circuit $V_{CE} = - I_{C.}$

$= R_L \| R_C$

3) CURRENT GAIN A_I

$A_I = \ =$

$-I_C = h_{fe`1\ 2347890=}\ I_B + h_{oe} V_{CE}$

I_B

$= h_{fe} + h_{oe}$

$+ h_{oe} = h_{fe}$

$+ [\ 1+ h_{oe} = h_{fe}$

=

$A_I = \ =$

4) INPUT IMPENDANCE

$R_i = \ =$

$V_{BE} = h_{fe}\ I_B + h_{oe}\ V_{CE}$

$V_{BE} = h_{fe}\ I_B + h_{oe}\ (-I_C\ )$

I_B

$= h_{fe} + h_{oe}\ .$

5) VOLTAGE GAIN:

$A_V = \ = \ =$

I_B

$A_V =$

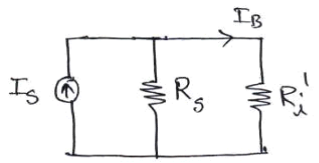
$A_V =$

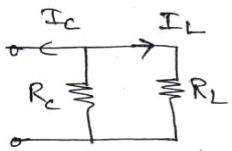
6) OUTPUT RESISTANCE

7) FOR CIRCUIT.

a) Current gain

$A_{IS} = \ =$





$I_B = I_S$ $I_L = -I_C$

= =

A_{IS} =

b) VOLTAGE GAIN.

A_{VS} = =

=

=

$A_{VS} = A_V$ yh

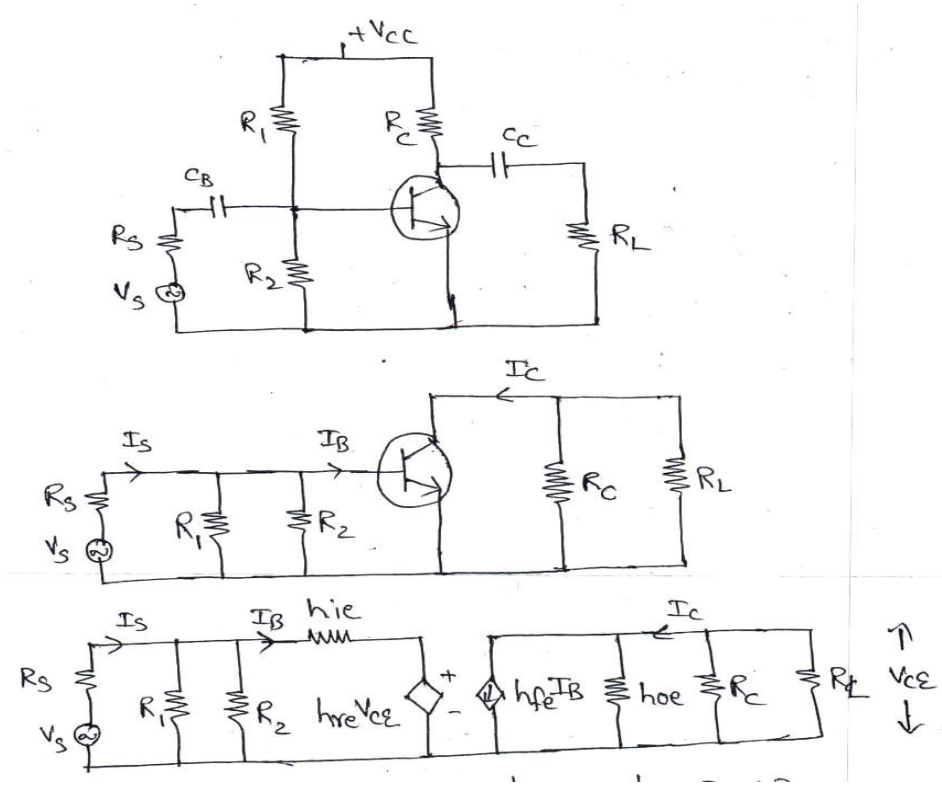
c) Input resistance

$= R_1 R_2 R_i$

4) Output resistance

$= R_L R_C R_O$

8) CE AMPLIFIER with EMITTER (short circuited = 0)



1) ACE amplifier is shown below.

$V_{CE} = -I_C . , = R_C \; R_L$

[NOTE**:** The previous circuit and this circuit are same]

1) A_I = → A_{IS} =

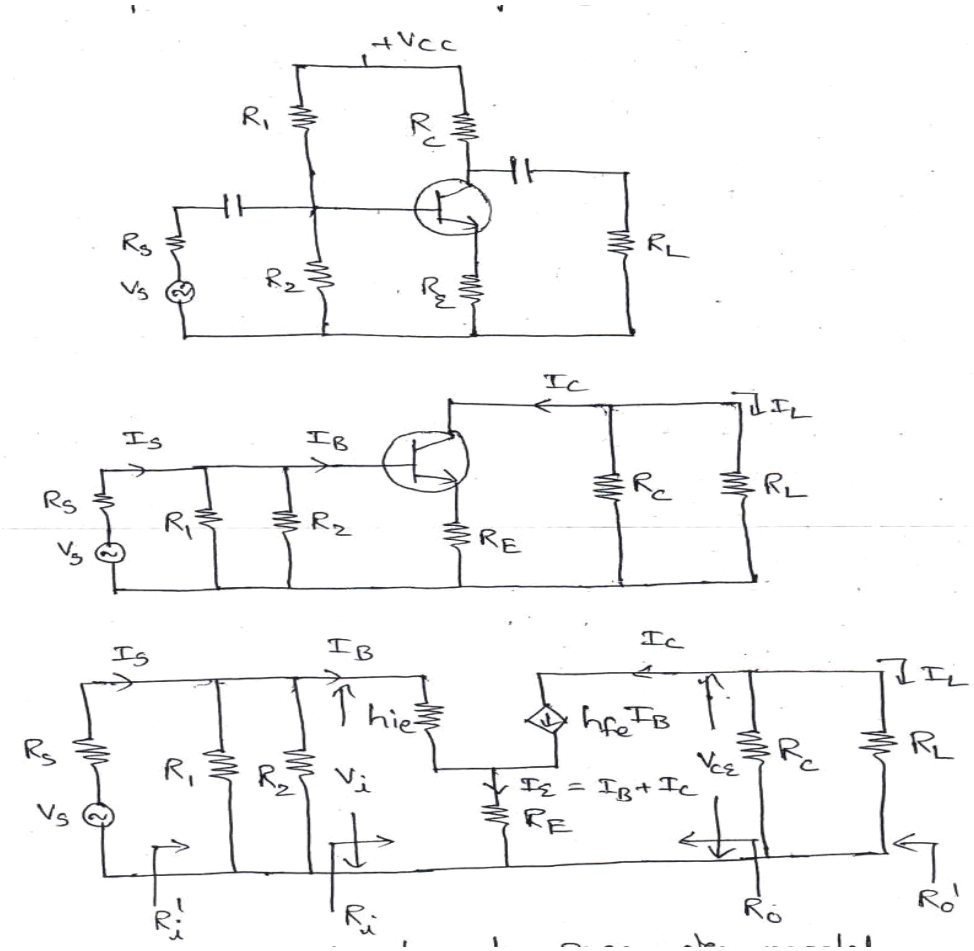
2) = + → = R_1 R_2 R_i

3) A_v = → A_{VS} = A_v

4) = → = R_L R_C R_O.

CE AMPLIFIER WITH R_E RESISTOR.

1) A CE amplifier with only R_E resistance is considered



Approximate h- parameter model

$I_E = I_B + I_C = I_B + h_{fe} I_B = I_B[1+ h_{fe}]$

$V_{CE} = -I_C . , = R_L R_C$

A.C analysis for transistor.

2) Current gain A_I

$A_I = =$

$A_I -$

3) Input resistance

$R_i = =$

$V_{BE} =+ I_E R_E$

$V_{BE} =+ (1+h_{fe}) R_E$

$R_i = = + (1+) R_E$

[Very high input resistance]

4) VOLTAGE GAIN

$A_V = = =$

=

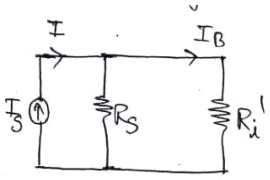
=

5) Output Resistance

R_O = =

A.C analysis for circuit

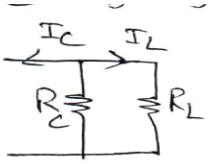
1) Current gain



= =

=

=



$I_L = -I_C$

=

A_{IS} =

2) VOLTAGE GAIN

A_{VS} = =

=

=

A_{VS} = AV

3) INPUT REISTANCE

= R_1 R_2 R_i

4) OUTPUT RESISTANCE

= R_L R_C R_O

10) COMMON COLLECTOR (OR) EMITTER FOLLOWER (OR) VOLTAGE FOLLOWER

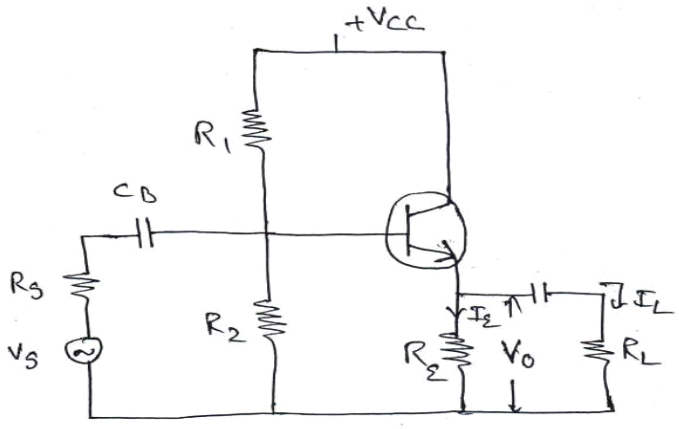
1) in the emitter or voltage follower circuit the output for voltage follow is input voltage hence named voltage follower. The voltage across R_E resistor is output voltage.

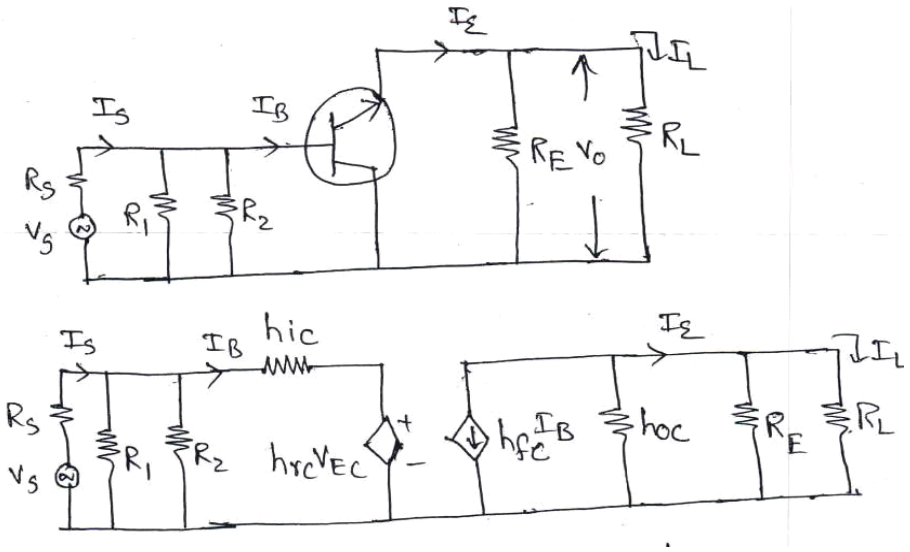
2) The voltage gain of this circuit is amity. Hence if can be used as voltage buffer circuit.

3) The emitter follower circuit has high current.

4) The input resistance of this circuit is very high.

5) A emitter follower circuit is shown in below.





$V_{EC} = -I_E.$, $= R_E\ R_L$

6) AC analysis for transistor

a) Current gain A_I =

$- I_E = h_{fc}\ I_B + h_{oc}\ V_{EC}$

$- I_E = h_{fc}\ I_B + h_{oc}\ I_E$

$= h_{fc} + h_{oc}$

$-h_{fc} = + h_{oc}$

$[1+ h_{oc}\ ] = - h_{fc}$

A_I = = = 1 +

B) INPUT RESISTANCE

R_i = =

V_{Bc} = h_{ic} I_B + h_{rc} V_{EC}

V_{Bc} = h_{ic} I_B + h_{rc} .I_E

= h_{ic} + h_{rc} .

R_i = = h_{ic} + h_{rc} .A_I = h_{ie} + 1 (1+ h_{fe})

C) VOLTAGE GAIN

A_V = = =

= = =

=

= ,

- neglected.

A_V = = 1

V_o = V_i, output voltage follows input voltage.

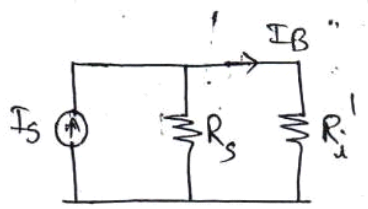
D) OUTPUT RESISTANCE. (R_O)

R_o =

7) A.C analysis for circuit.

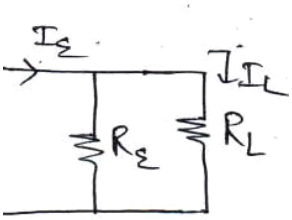
a) Current gain

A_{IS} = =



$I_B = I_S$

=



$I_L = I_E$

=

A_{IS} =

b) VOLTAGE GAIN

A_{VS} = =

=

=

$A_{VS} = A_V$

c) Input resistance

$= R_1 \ R_2 \ R_i$

b) Output resistance

$= R_L \ R_E \ R_O$

MILLERS THOREM.

1) According to millers theorem, when even a resistor is connected between two nodes fig (1), it can be replaced as shown in fig (2)

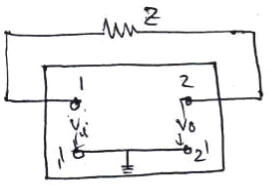
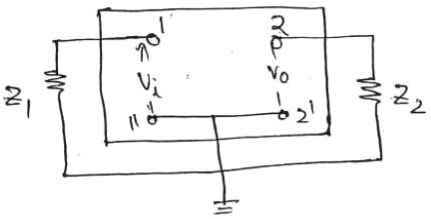


fig 1.



Where Z_1 & Z_2 are given by

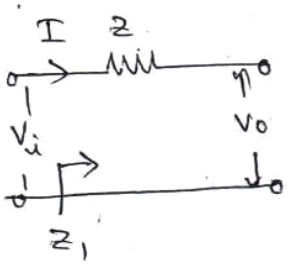
Z_1 = , Z_2 = Z

K = = A_V

Where V_i is voltage at node 1 and V_0 is voltage at node 2.

2) proof

Consider a circuit shown in fig.3



Z_1 =

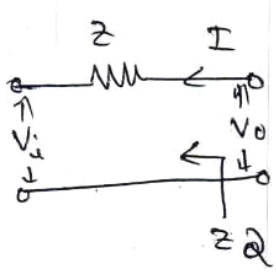
I =

=

Z_1 = =

Z_1 = =

Consider a net work shown in fig . 4



Z_2 =

I =

=

Z_2 = = =

Z_2 = = Z [K > > 1]

12) DUAL OF MILLER'S THWOREM

Consider a network shown in fig 1 (a) now Z^1 is the impendence between node 3 and ground N. according to dual of millers theorem Z^1 can be split into Z_1 and Z_2 such that Z_1 is placed in mesh 1 and Z_2 is added to mesh 2 as shown in fig 1 (b) and node 3 is grounded.

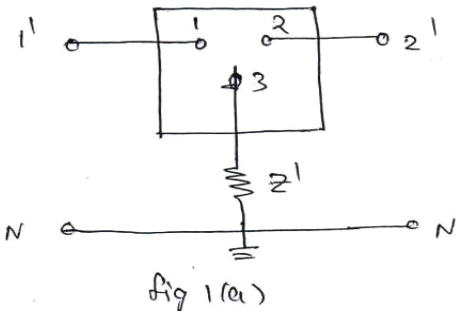


fig 1(a)

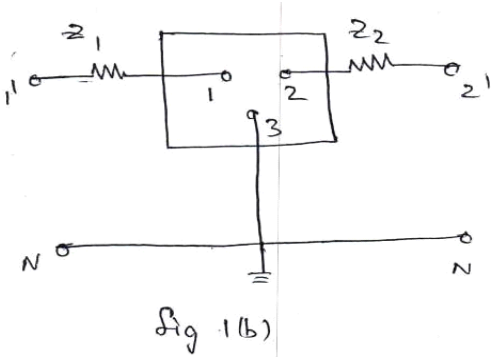


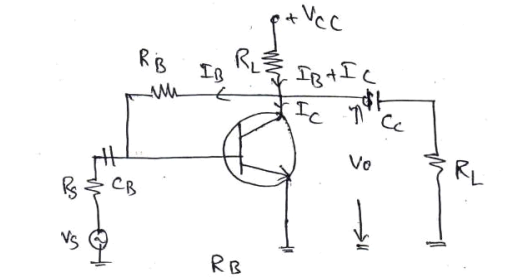
Fig 1(b)

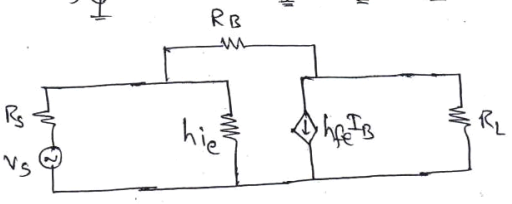
A_I = , $Z_2 = Z^1$

$Z_1 = Z^1 (1- A_I)$ Z_2 Z^1

COLLECTOR BASE BIAS CE AMPLIFIER.

1) A CE amplifier with collector base bias is shown below.



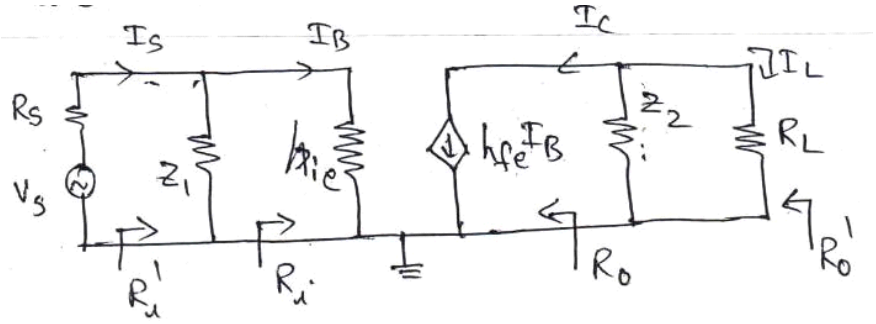


Miller theorem.

$Z_1 = \frac{R_B}{1 - A_V}$

$Z_2 \approx R_B$

Using miller theorem.



2) A.C analysis for transistor.

a) Current gain

b) input resistance

c) Voltage gain

A_I = = = -

= = = =

= = =

=

=

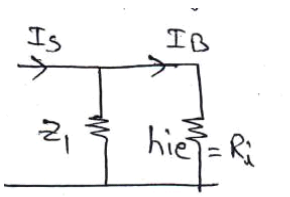
= Z_2

b) Output resistance R_0 =

3) A.C analysis for circuit

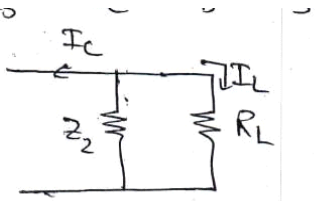
a) current gain

= =



$I_B = I_S \times \frac{Z_1}{Z_1 + R_i}$

$\frac{I_B}{I_S} = \frac{Z_1}{Z_1 + R_i}$



$I_L = -I_C \times \frac{Z_2}{Z_2 + R_L}$

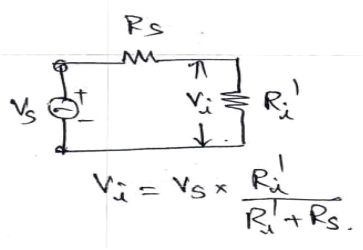
$\frac{I_L}{I_C} = \frac{-Z_2}{Z_2 + R_L}$

A_{IS} = $(-h_{fe})$

b) VOLTAGE GAIN

= =

=



C) Input resistance ()

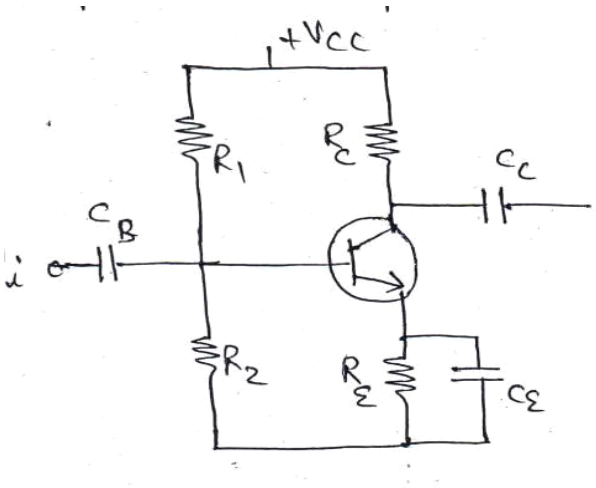
= Z_1 R_i

d) Output resistance

= R_L Z_2

RC COUPLED CE AMPLIFIER DESIGN.

1) A RC coupled CE amplifier is shown below



ASSIGNMENT – I

1) explain about single stage CE amplifier. Explain function of each component.

2) Explain CB, CE, CC configuration with h- parameter analys and draw equivalent circuits.

3) Explain how h- parameters can be obtained from the transistor characteristics.

4) list the benefits or h- parameter.

5) derive the expressions for A_I , A_{IS} , A_V, A_{VS}, R_i, R_i^1, R_0 , R_0^1 for CE amplifier.

6) give analysis for CE amplifier with R_E

7) draw the circuit of CB amplifier and its h- parameter equivalent circuit.

8) explain follower circuit.

(or)

Explain voltage follower circuit

(or)

Given analysis of C.C amplifier.

9) state and explain milter's theorem and its dual.

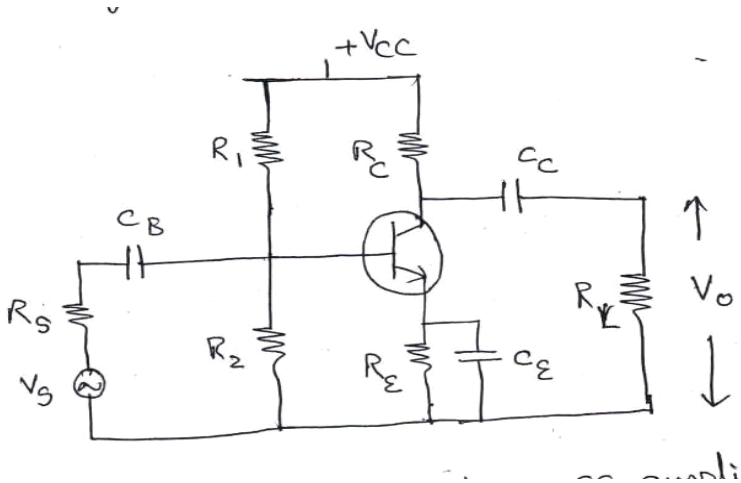
10) design a single stage RC coupled amplifier.

ASSIGNMENT – 2

CE AMPLIFIER

1) Consider a single stage CE amplifier with

R_S = 1k, R_1 = 50k, R_2 = 2k, R_c = 2k, R_L = 2k, h_{fe} = 50,



(h_{ie} = 1.1k, h_{oe} = 25 and h_{re} = 2.5 10^{-4} as shown in fig 1. Find A_V , A_{VS} , A_I , A_{IS} , R_i , R_i^1 , R_0 , R_0^1 ,

A_I = -50

A_{IS} = -15.9

A_V = -45.45

A_{VS} = -18.71

R_I = 1.1K

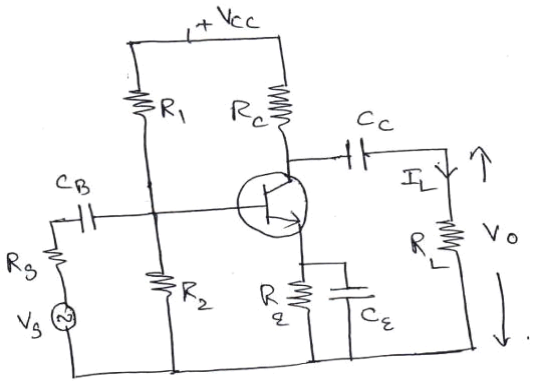
R_O = 40K

R_I^1 = 700Ω

R_o^1 = 1 k

2) Consider a single stage CE amplifier with Rs = 1 KΩ, R1 = 50KΩ, R_2 = 2K, R_c = 1KΩ, R_L = 1.2 kΩ, h_{fe} = 2.5 50, h_{ie} = 1.1K, h_{oe} = 25μA/V, h_{re} = 2.5 10^{-4}, as shown in fig.2.

Find A_I, $A_{IS, Ri}$, , A_V, A_{vs}, R_0,



A_I = -49.32

A_{IS} = -14.29

A_V = -25.61

A_{VS} = 10.1

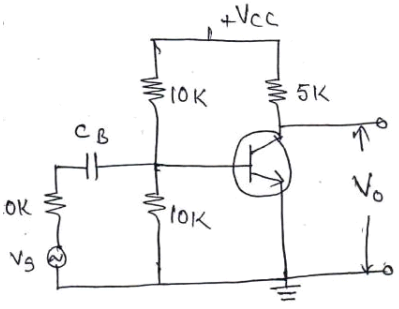
R_i = 1093Ω

R_O = 55.8K

R_i^1 = 696.9Ω

R_o^1 = 540Ω

3) the transistor amplifier shown in fig. 3 has h- parameter typical values h_{ie} = 1100Ω , h_{fe} = 50, h_{re} = 2.5 10^{-4} h_{oe} = . . Find A_{VS} , A_{IS} , R_o^1, R_i^1



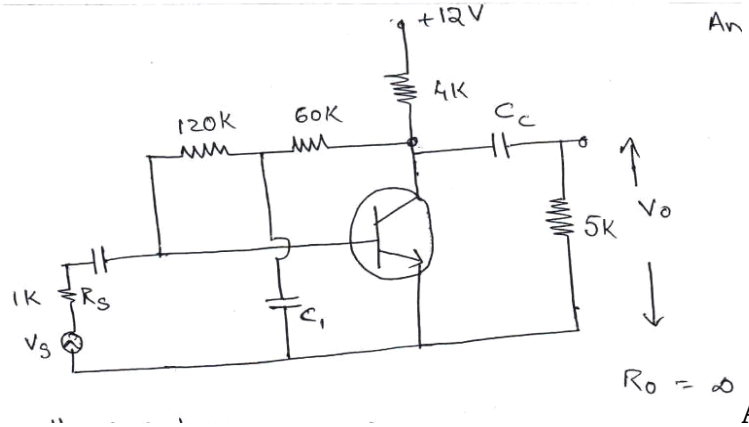
A_{VS} = 18.22

A_{IS} = -39.856

R_o^1 = 4487Ω

R_i^1 = 0.9367 KΩ

4) the transistor used in the circuit show in fig 4, has following values h_{ie} = 500Ω, h_{re} = 60, h_{oe} = 1/40k, calculate R_i , R_i^1, A_V , A_{VS} , A_I , A_{IS} , R_o, R_o^1



Ans

A_I = -60

A_{IS} = -25.58

A_V = -257.16

A_{VS} = -85.49

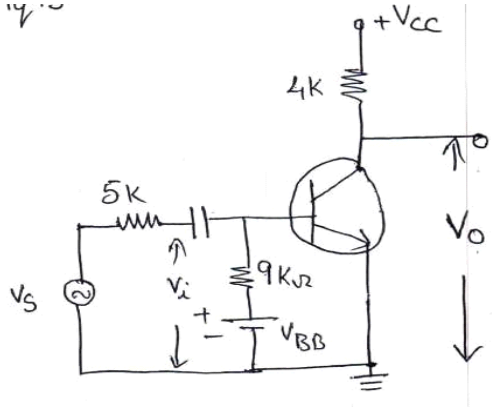
R_I = 500Ω

R_i^1 = 498 Ω

R_o^1 = 2.143K

5) For the circuit shown in fig .5:

Find, R_i , R_i^1, R_o, R_i^1, A_{VS}, A_I



Use typical values.

Ans:

A_I = -200

A_V = -200

A_{VS} = -71.13

R_i = 4K

$_{Ri}^{1}$ = 2.76K

R_o^1 = 4K

CE amplifier with R_E

6) Find current gain, voltage gain, input and output resistance for unbypassed CE amplifier. In fig 6.

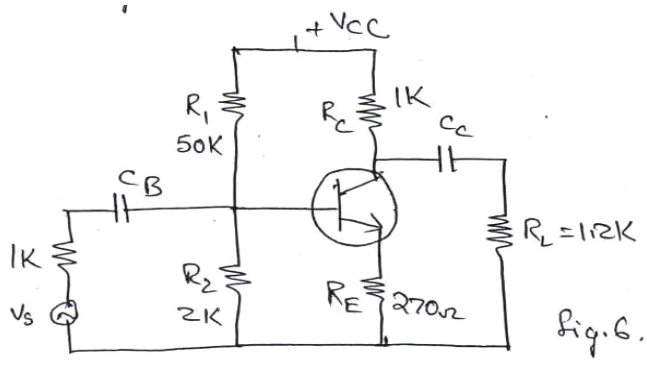


Fig. 6.

Ans:

A_I = -50

A_{IS} = -2.6

A_V = -1.834

A_{VS} = -1.15

R_i = 14.87

R_i^1 = 1.7K

A_I = -0.454

R_o^1 = 545.45Ω

7) For fig.6 use typical values of h parameter and Rs = 10K, R_1 = 100K, R_2 = 10K, R_e = 1K, R_L = 5k.

Find R_i , R_i^1, A_V , A_{VS} , A_I , A_{IS} , R_o, R_o^1

Ans: (A_I = -43.45, -7.24 , -4.77, -2.05, 45.48K, 7.576K, 215K, 4.8K)

CC Amplifier

8) A common collector circuit shown in fig .8 has the following parameters, Rs = 600Ω, R_1 = 27K, R_2 = 27K, R_e = 5.6K, R_L = 47kΩ. h_{ie} = 1K, h_{fe} = 85,

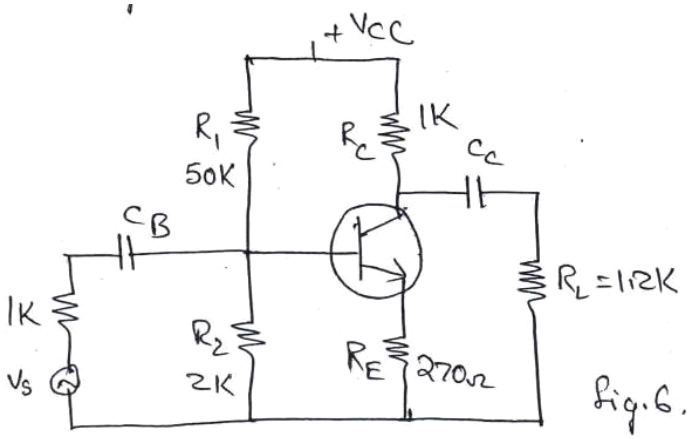


fig.6.

h_{oe} = 2μA/V,

Find R_i ,A_V , A_{VS} , A_I , A_{IS} , R_o

Ans:

A_I = 86

A_{IS} = -0.273,

A_V = 0.997,

A_{VS} = 0.953

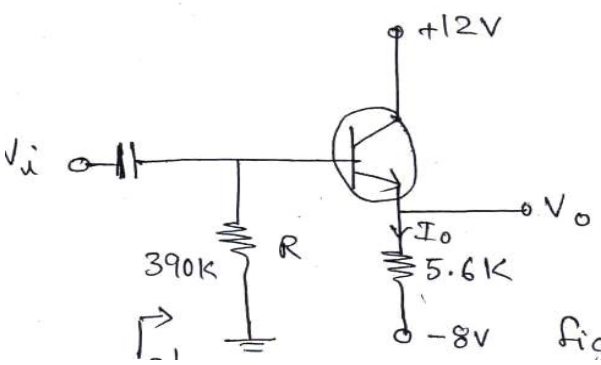
R_i = 431.33K

R_i^1 = 13.09K

R_o = 18.3Ω

R_o^1 = 18.23Ω

9) The circuit shown in fig 9. Has h_{fe} = 100, h_{ie}= 3.37KΩ neglected h_{re} , h_{oe} , find R_i^1, A_V, A_I.



A_I = 101

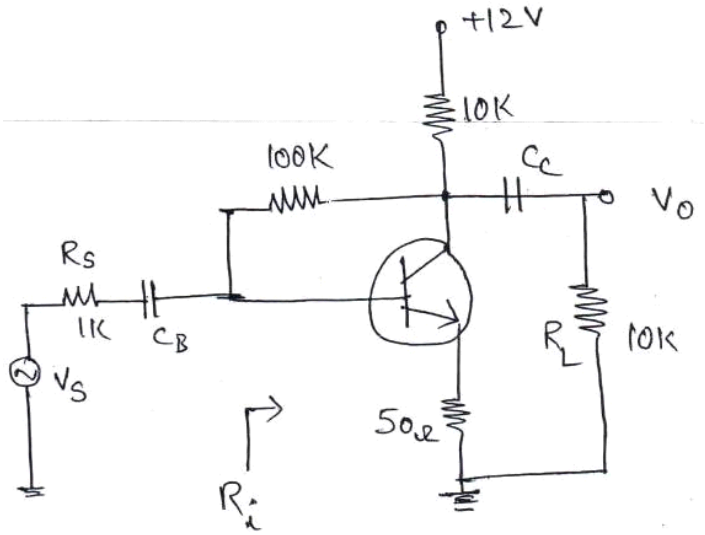
R_i = 568.9K

R_i^1 = 231.39K

A_V = 0.994,

A_{IS} = 41

MILLER'S CIRCUIT



10) Find, A_I, A_{VS}, R_i, R_o for circuit shown in fig .10

A_I = -8.25

R_i^1 = 1.048K

R_0^1 = 5K

A_{VS} = -69.8

MULTISATAGE AMPLIFIERS

1) INTRODUCTION

A single stage amplifier provides amplification of for a weak signal, but the gain of single stage may not be sufficient for contain applications. Under such cases we go for multistage amplification i.e., amplifying 'a signal again and again. Sometimes the impendance matching at source and load is not proper in such matching at source and load is not proper, in such cases using a cascaded amplifier, the above requirement can be achieved.

2)TWO STAGE RC COUPLED CE-CE CASCADED AMPLIFIER.

1) A CE -CE cascaded amplifier is shown below. fig.1

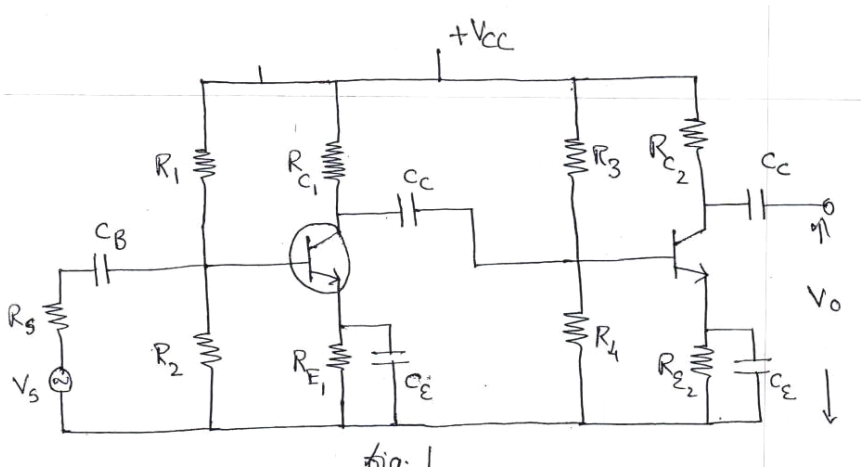
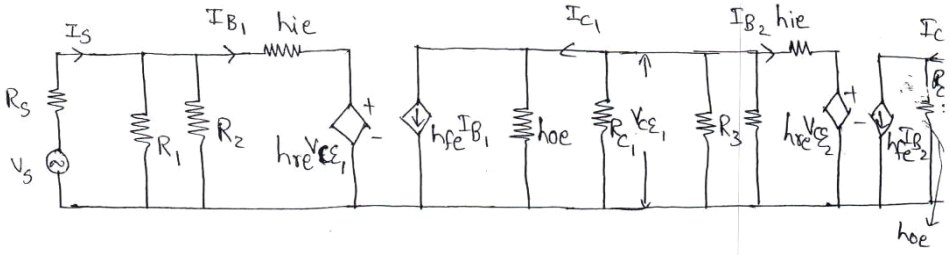


fig. 1

h- Parameter equivalent circuit for CE – CE cascade amplifier is shown below. Fig 2.



2) Analysis of second stage.

1) Current gain

A_{I2} = - =

2) Input resistance

= +

3) Voltage gain

=

3) Analysis of first stage.

The input resistance is load resistance for first stage.

= = $R_3 \parallel R_4 \parallel$

= ‖ = ‖‖‖

1) Current gain

= =

2) Input resistance

= +

3) Voltage gain

=

4) OVERALL GAIN.

1) Total voltage gain

A_V =

= A_V

2) Input resistance

= R_1

3) output resistance

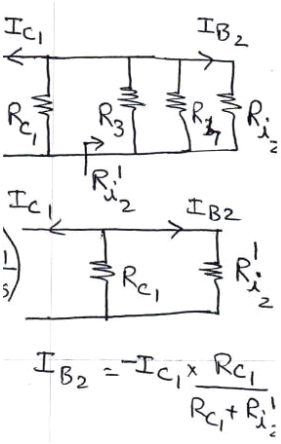
=

4) Current gain A_I

For finding current gain, loading effect must be considered. Hence the gain is calculated as shown below.

A_I = = =

A_I = -



With source resistance R_S

A_{IS} = =

A_{IS} =

A_{IS} = (- (-

= R_1

= $R_3 \parallel R_4 \parallel$

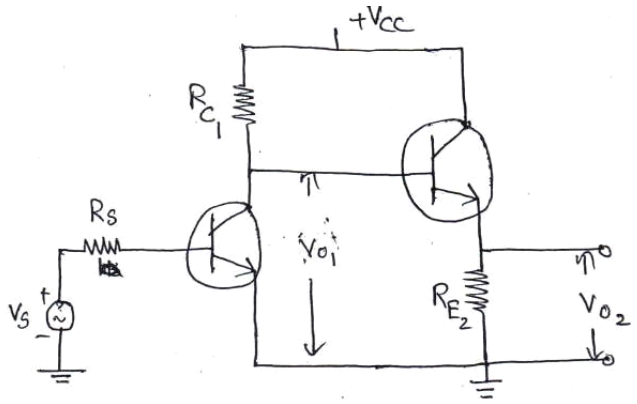
=

=

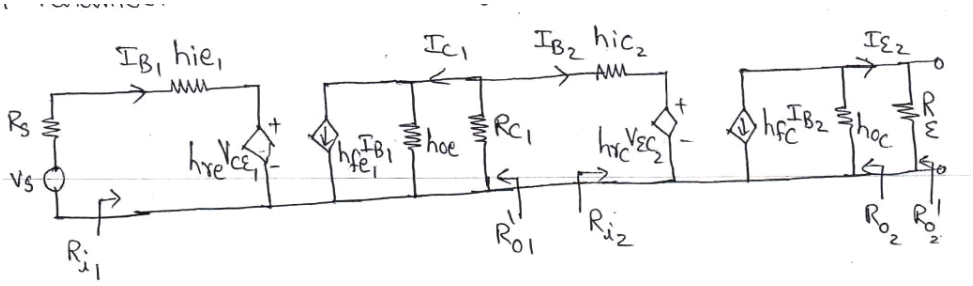
=

3) TWO – STAGE RC COUPLED CE-C.C CASCADED AMPLIFIER.

1) A two stage CE-C.C amplifier is shown below in fig .1



h- Parameter model of two stage CE – CC amplifier



2) A.C analysis of second stage.

1) Current gain

A_{I2} = -

2) Input resistance

= +

3) Voltage gain

=

3) A.C analysis of first stage.

1) Current gain

= ,

= =

2) Input resistance

= +

3) Voltage gain

=

3) Over all gain:

1) Voltage gain (A_V)

A_V =

= A_V

2) Current gain (A_I)

A_I = =

A_I =

3) Input resistance R_i

=

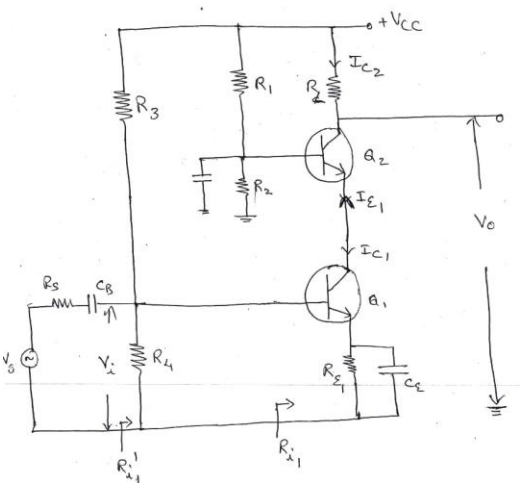
4) Output resistance R_o

R_o = ‖

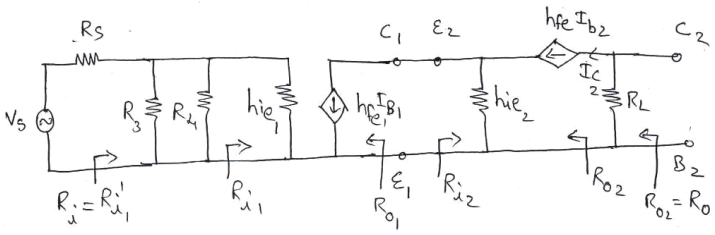
= -

R_o =

4) CE – CB CASCODE AMPLIFIER.



h- Parameter equivalent for CE – CB amplifier



2) A.C analysis of second stage (CB)

1) Current gain

A_{I2} = = 1

2) Input resistance

=

3) Voltage gain

=

3) A.C analysis of first stage (CE)

1) Current gain

= -

2) Input resistance

=

3) Voltage gain

=

4) Over all gain:

1) Voltage gain (A_V)

A_V =

=

2) Output resistance

R_O = ‖

3) Input resistance

R_i = ‖‖

4) Current gain

A_{IS} = =

= = -1

= = -1

= ,

= ‖.

A_{IS} = (-1)

A_{IS} =

5) DARLINGTON PAIR [high input resistance circuit]

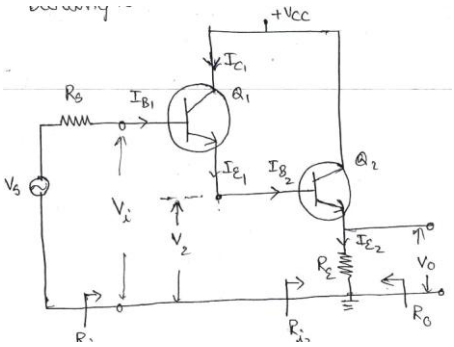
1) The common collector circuit has high input impendence about 200k Ω to 300kΩ. when considered with biasing resistors, for a emitter follower has input impendence lers 500kΩ

2) The input impendence of the circuit can be improved by direct coupling of two stages of emitter followers amplifier. By using following two methods.

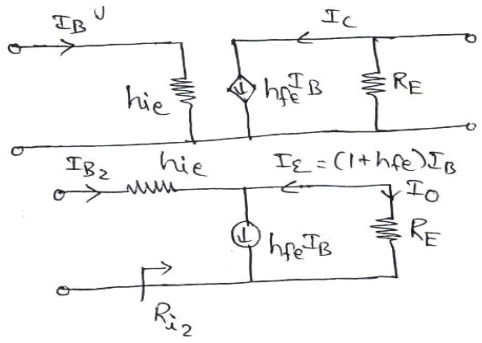
1) Using direct coupling (Darlington pair)

2) Using bootstrap technique

3) A Darlington pair is shown below.



4) A.C analysis of second stage.



1) Current gain

= =

=

Input resistance

=

- -

- -

=

= +

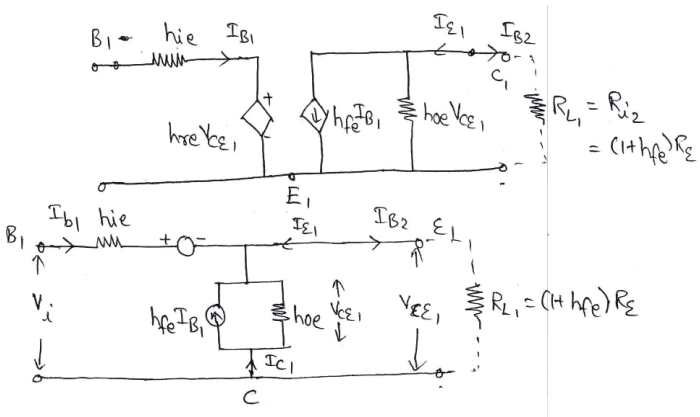
= +

3) voltage gain

= 1

5) A.c analysis of first stage.

The output resistance of first stage is input resistance of second stage. (= . As is very high exact model of transistor h- parameter is considered.



1) Current gain (

=

=)

= +

= +)

+)

Using eq of

=)

=)

=

[1+ = (1+)

=

= =

= =

2) INPUT RESISTANCE R_i

R_i =

KVL to input loop R_i

- -

- - u

$V_i = h_{ie} + h_{re}$ -

$= h_{ie} + h_{re}$ - (.)

$= h_{ie}$ - - (.)

$V_i = h_{ie} +$

$= = h_{ie} +$.

$= h_{ie} +$.

6) over all gain

1) Current gain $=$

$=$

$=$

2) overall voltage gain

$A_V =$

$A_V =$

$=$, > >

3) output impedance (

=

= +

6) Comparison of emitter follower and Darlington

	C.C	Darlington
R_i (168kΩ)	$R_i = (1+ h_{fe}) R_E$	$R_{i =}$ (1.65mΩ)
A_I	$A_i = 1+ h_{fe} = 51$	$A_i =$ = 500

7) METHODS OF COUPLING

When cascading amplifier is done, coupling of one stage to one stage is done based following 3 methods.

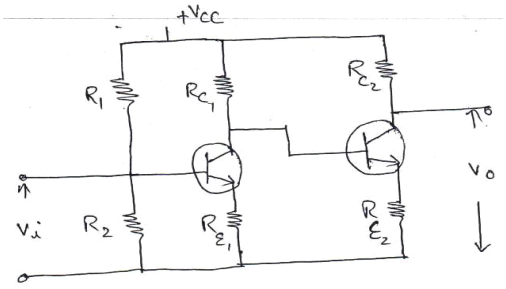
1) Direct coupling

2) RC coupling

3) Transformer coupling

1) DIRECT COUPLING

1) A two stage direct coupled amplifier is shown below.



2) the output of first stage is directly connected to next stage input.

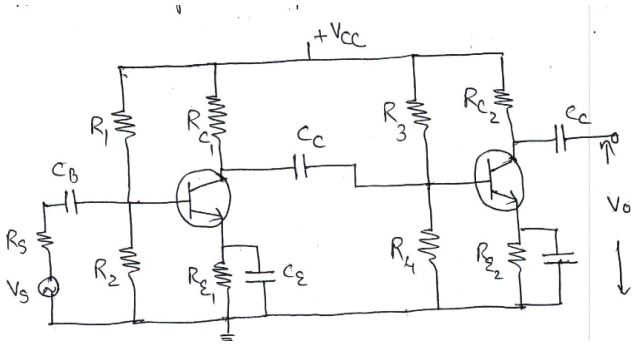
3) The d.c collector current of first stage passes to input of next stage is altered. This effects the biasing condition of second stage amplifier.

4) The low frequency response of this amplifier is gold, but hight frequency response is poor because of stray capacitance.

5) The change in temperature disturbs the V_{BE} and B of transistor, by which outout collector current is varied. The output is distorted.

2) RC COUPLED AMPLIFIER.

1) A RC coupled amplifier is shown below.



2) The output of first stage amplifier is connected to input of next stage amplifier through a capacitor and resistor.

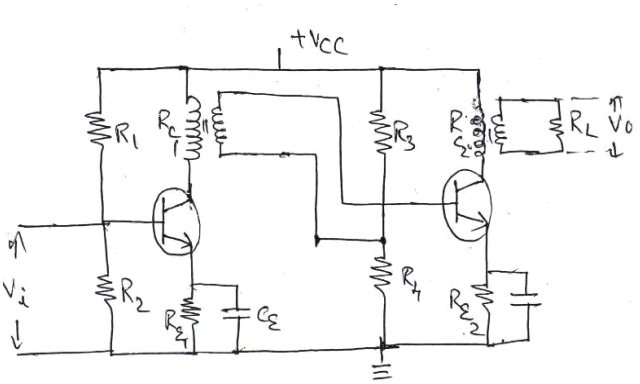
3) The capacitor 'C_C' blocks the d,c components therefore a point is maintained stable for both amplifier.

4) The frequency response is wide band in nature hence this amplifier provides stable gain for AF applications.

6)At very low frequency the coupling capacitor C_C effects the gain and at very high frequency gain falls to stray capacitance.

3) TRANSFORMER COUPLING.

1) A transformer coupled amplifier is shown in fig below



2) The output of first stage amplifier is connected to input of next stage through a transformer.

3) When impendence matching is criteria then this is achieved by proper selection of transformer between cascaded stage.

4) the d.c conditions of both stage are stable as the coupling does not effect Q point.

5) The frequency response of this amplifier is poor when compared to RC coupled amplifier.

6) The intertwining and leakage indolence does not allow amplifier to amplify the signals of different frequencies. Equally well.

7) these amplifiers when provided with a capacitor in shunt with transformer winding , faction as resistance circuit and provide very large or high gain at that resonant frequency.

8) The d.c resistance of the transformer winding is kept low. So that power loss is lers.

ASSIGNMENT-1

1) what is need for cascading ? explain

2) Draw and explain the block diagram of two stage CE –CE cascaded amplifier

3) Derive the overall gain of two stage cascaded

Derive the overall current and voltage gain Input and output resistance of CE-CE cascaded amplifier.

4) Find, A_I, A_v, ,, for CE –CE cascaded amplifier

5) Find, A_I, A_v, ,, for CE –CB or cascade amplifier

6) Explain any one circuit which is used to improve the input impendence of the amplifier.

7) What is Darlington connection ? derive current gain and input resistance.

8) What are draw backs of a Darlington amplifier, how it overcomes in Boot strap CC amplifier. Explain with neat diagram.

9) Compare emitter follower and Darlington pair with respect different A_I, A_v, R_i, R_O,

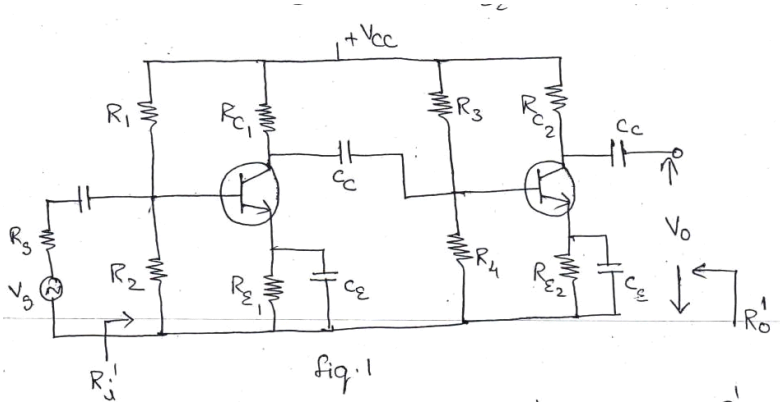
10) What are different types of coupling used in cascading of amplifiers? Explain.

ASSIGNMENT – 2

CE-CE cascading.

1Find A_V, A_{VS},,, consider – h- parameter typical values, for a CE-CE cascaded amplifier (fig .1)

R_1 = 22kΩ, R_2 = 3.3 kΩ, = 6 kΩ , = 1kΩ, R_3 = 16 kΩ R_4 = 6.2 kΩ, R_S = 1.1k.



= 700Ω, = 470 Ω.

(A_V = 1112.39, A_{VS} = 466.73 , = 795.18Ω = 700K)

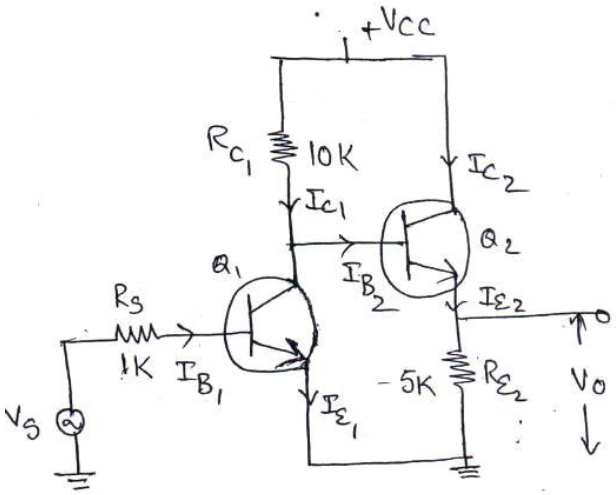
2) Find A_V, A_{VS},, for circuit shown in fig.1 given R_1 = 200k, R_2 = 20k = 15k , = 100Ω, R_3 = 47 k, R_4 = 4.7k, R_S = 1k, = 4k, = 330 Ω.

Consider h- parameter typical values.

Ans (A_V = 6123.45, A_{VS} = 3248.6, = 1.13k, = 4K)

CE –CC cascading.

3) Find over all voltage and current gain, , for shown in fig 2.



Ans (A_I = -76.56, A_V = -216.5, A_{VS} = -138.28, = 1.76k, = 199.69Ω)

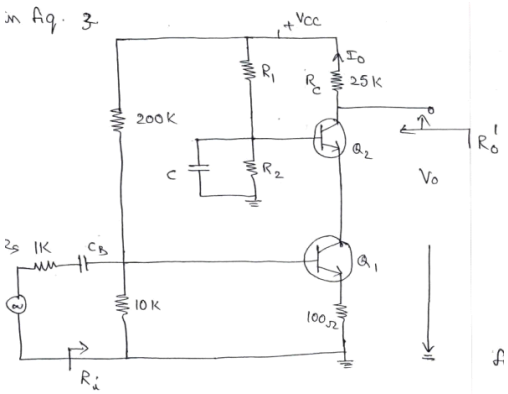
4) for the circuit shown in fig.2 find A_{VS}, A_{IS} h_{fe} = 76, h_{ie} = 1.5k, h_{re} = h_{fe} = 0.

= 10k, = 5k, R_S = 1k

Ans (A_{VS} = -295.2, A_{IS} = -58.52)

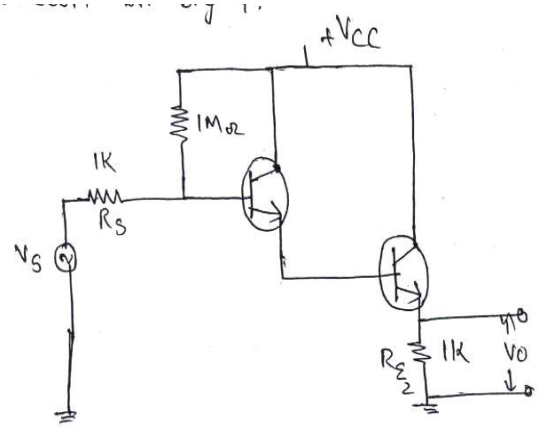
CE – CB

5) Calculate A_I, A_V, A_{VS},,, for cascade circuit shown in fig.3



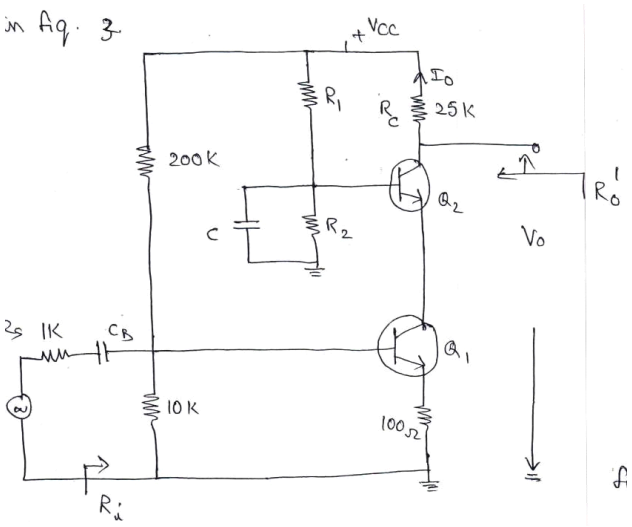
DARLINGTON PAIR.

6) Find R_i, A_{VS}, A_{IS},R_O for Darlington pair circuit shown in fig.4



Ans (A_{IS} = 889.23, A_V = 0.989, A_{VS} = 0.987, = 10.76Ω R_i = 0.89MΩ)

7) For the circuit shown in fig.5 calculate, A_I, A_V, h_{fe} = 50, h_{ie} = 1.1k, h_{re} =2.5 10^{-4}, h_{oe} = 25 A/V.

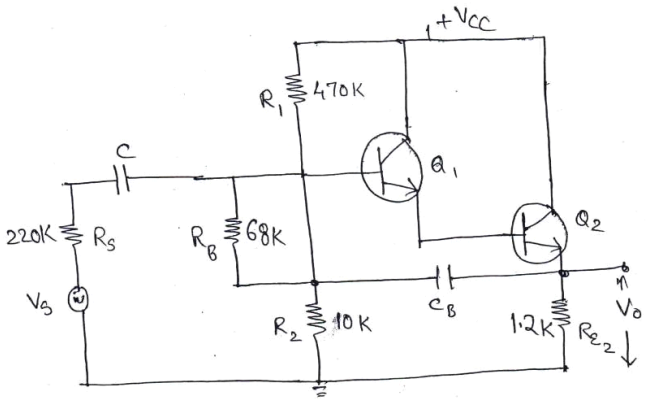


Ans A_V = 0.9918, = 2.02M, = 22.96 Ω.

= 51, = 0.258, =

BOOSTRAP CIRCUIT.

8) For the circuit shown in fig 6. Calculate A_V, A_{VS},,R_O consider typical values of h-parameter.



Ans (A_V = 0.979, = 286 k, = 92.28 Ω A_{VS} = 0.781, = 0.979, = 51.

9) For fig .6, calculate, A_V, A_{VS},,R_i

R_S = 10k, R_1 = 100k, R_2 = 10 k, R_B = 50k, = 10k,

Ans

(A_V = 0.997, A_{VS} = 0.9735, = 409.1k,R_O = 216.5Ω

= R_O ‖

UNIT – II

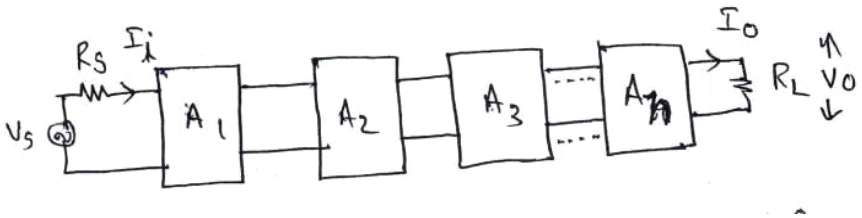
HIGH FREQUENCY AMPLIFIERS

1) GAIN IN DECIBELS.

The ratio of output voltage to inlput voltage is called voltage gain. The gain is expressed in logarithmic scale rather than a linear scale. The unit of this logarithmic scale is called decibel (dB).

$A_V = 2. \text{Log} | |$

2) GAIN FOR N- STAGE CASECADED AMPLIFIER.



The voltage gain of cascaded amplifier of n- stages is given by

=

For any single stage in cascaded amplifier

=

Gain in (dB)

+. …..

ADVANTAGES.

1) Overall gain is sum of individual gains in (dB).

2) Representation of gain is convenient for small and large values

Ex: A_V (dB) = -140 dB is for A_V = 0,0000001

3) In audio amplifier, output is measured in decibels hence logarithmic scale is better than linear scale.

3) FREQUENCE RESPONSE.

1) The frequency response and bandwidth of the amplifier get affected due to the cascade connection. The bandwidth of cascaded amplifier is always less than that of the bandwidth of single stage amplifier.

2) LOWER 3Db FREQUENCY

1) Let us consider the lower 3dB frequency of n identical cascaded stages is $f_L(n)$. The gain at $f_L(n)$. frequency is 0.707 or -3dB of its original value.

=

=

Squaring both sides.

2=

2=

=

= – 1

=

F_L = Lower 3dB of a single stage

= lower 3dB of a identical cascaded stages.

3) UPPER 3 Db frequency.

Let us consider the upper 3dB frequency of n identical stages is $f_{H(n)}$. it is the frequency for which the overall gain falls to 3dB of its original value.

Gain of n stage cascaded amplifier.

=

=

=

Squaring both sides.

=

$F_{H(n)}$ = cutoff frequency of cascaded amplifier.

= cutoff frequency of single stage

N = no. stages.

3) BANDWIDTH

On cascading, is always greater then f_L and $f_{H(n)}$ is always less than f_H. therefore bandwidth of multistage amplifier is always less than single stage amplifier.

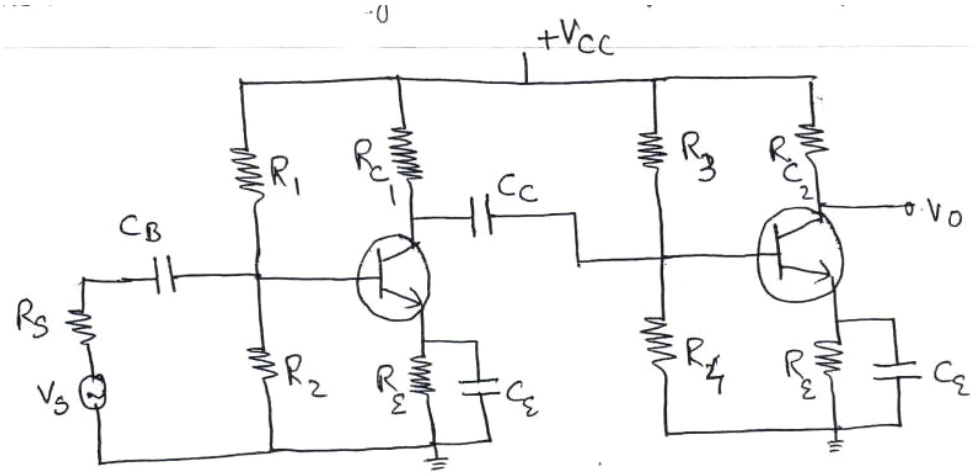
$(B.W)_n < (B.W)_{\text{single stage}}$

5) FOR n non identical stages of amplifier.

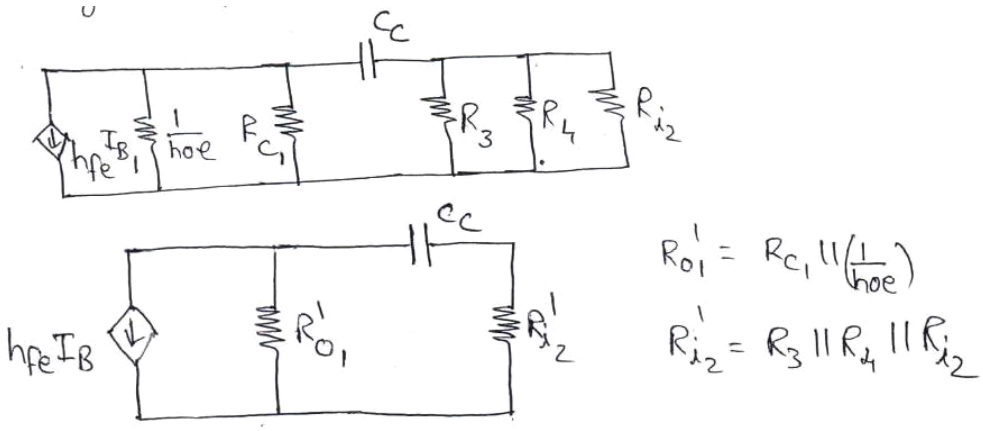
= 1.1

6) EFFECT OF COUPLING CAPACITOR.

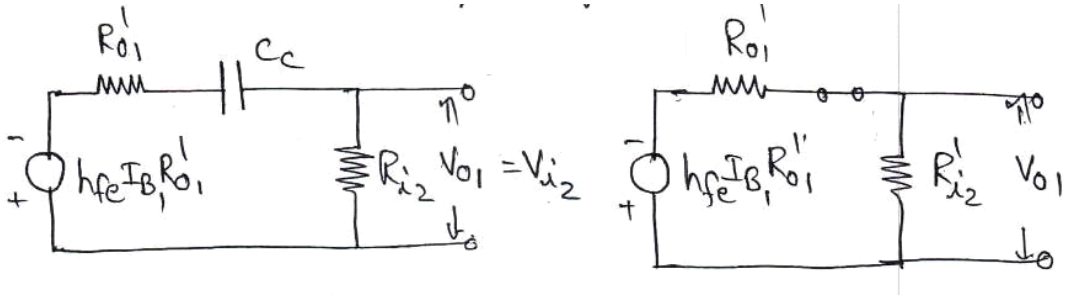
1) consider a two stage RC coupled amplifier.



2) Consider small signal model of first stage output and second stage input section.



3) VOLTAGE GAIN at mid frequency range.



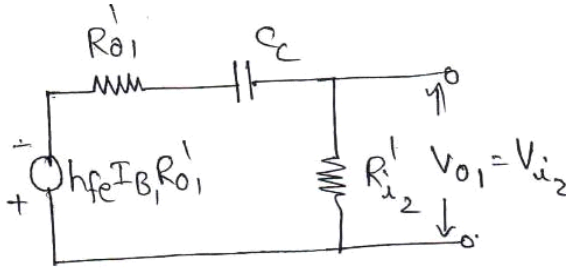
At mid and high frequency capacitive reactance is very small hence replaced by short circuit.

A_{Vmid} = =

4) VOLTAGE GAIN FOR LOW FREQUENCY RANGE.

At low frequency the capacitive reactance is considerable value.

Hence taking coupling capacitor into account as shown in figure.



V_O = -(h_{fe})

= - h_{fe}

V_O =

Dividing both sides by ,

$A_{V\ Low}$

$A_{V\ Low}$ =

=

=

At f =n

= = 0.707

At = 0 ,

= 1

At = , = 0

At cutoff frequency f_L the fells to 3dB from $A_{vMid.}$ This frequency is also called as lower 3dB frequency fig.7

5) VOLTAGE GAIN for high frequency.

At high frequency the capacitors have low reactance hence act as short circuit, there fore the gain drops to zero beyond frequency f_H

=

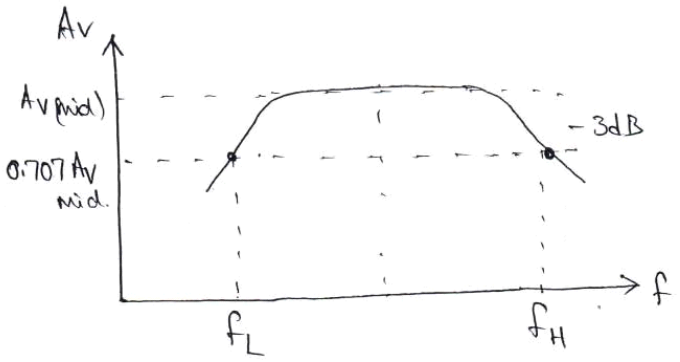
= = 0.707

= 0

At f=

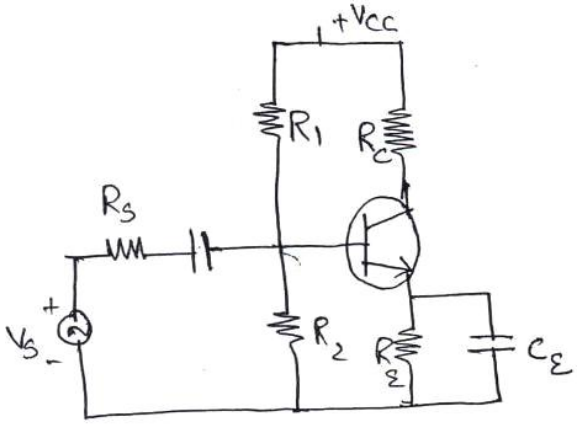
At f =

6) the gain frequency response is given below.

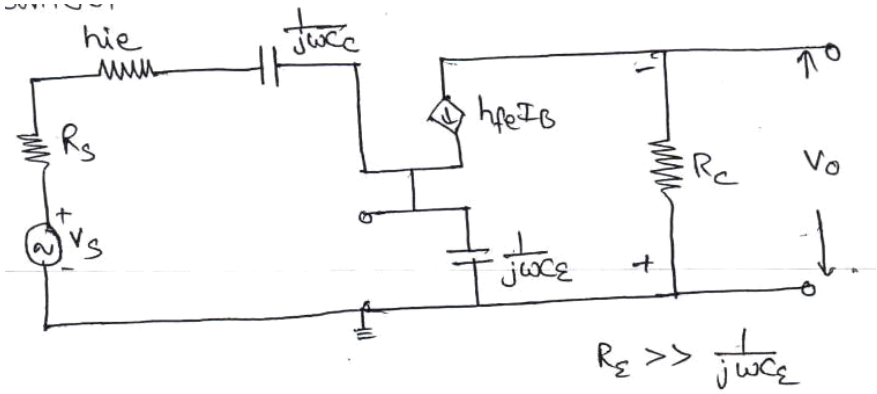


7]ANALYSIS OF EFECT OF COUPLING AND BYPASS CAPACITORS.

1) Consider a single stage amplifier.



2) h- parameter model.



Output voltage

$V_O = (-h_{fe} I_B) R_C$

Input voltage, Applying KVL to input loop.

- - - = 0

=

=

= ,

3) Voltage gain.

A_V = =

A_V =

4) VOLTAGE GAIN FOR mid frequency.

All capacitors provide low reactance at mid and high frequencies, hence capacitance are neglected.

= =

5) VOLTAGE GAIN for low frequency.

At low frequency capacitive reactance are considered.

=

=

$A_{V\ Low}$ =

=

=

=

= = 0.707.

At f = ,

The cutoff frequency or lower 3dB frequency is f_L, at this frequency gain falls to 0.707 from maximum.

8) HYBRID-TT MODEL

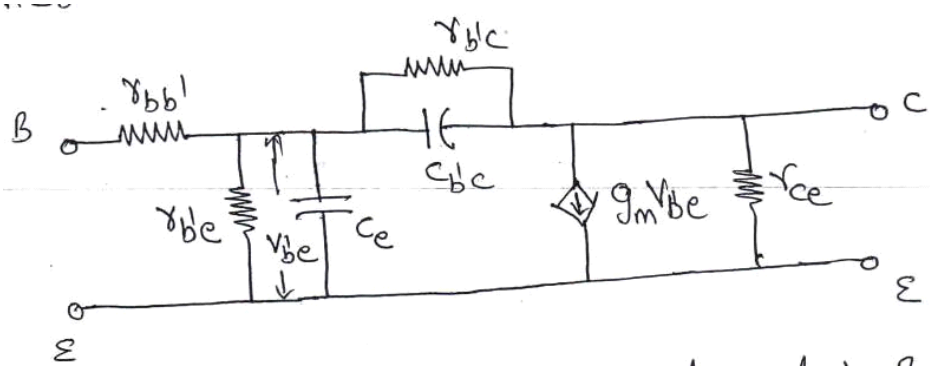
1) At high frequencies. The h- parameter model is not suitable, because of change in transistor behavior.

i) The values of h- parameter are not constant at high frequencies.

ii) At high frequency h- parameters behavior is complex.

2) Hence the h-parameter model is replaced by HYBRID – TT model.

3) HYBRID – TT CE trans conductance model.



The parameters considered are independent of high frequency but dependent on quiescent operating point.

Cb^1 e → diffusion capacitance (C_e)

Cb^1c → Transition capacitance (C_C)

$r_{bb}{}^{1}$ → The bulk resistance between external base terminal and internal node B^{1} is represented as $r_{bb}{}^{1}$ (base spreading resistance.)

$r_{b}{}^{1}{}_{e}$ → base emitter internal resistance.

$r_{b}{}^{1}{}_{C}$ → the variation of voltage across the collector to emitter junction results in base-width modulation. The change in the effective base width causes the emitter current to change. This effect between output and input is taken into account by connecting $r_{b}{}^{1}{}_{C}$ between collector and base.

g_{m} → Due to the small changes in voltage $V_{b}{}^{1}{}_{e}$ across the emitter junction, there is excers – minority carrier concentration injected into the base which is proportional to the $V_{b}{}^{1}{}_{e.}$ This results in small signal collector current, with collector shorted to the emitter is also proportional to the $V_{b}{}^{1}{}_{e.}$

This effect accounts for the current generation '$g_{m}\ V_{b}{}^{1}{}_{e}$'

G_{m} = |constant

→ The r_{ce} is the output resistance.

9) TYPICAL VALUES.

G_{m} = 50 mA/V

$R_{bb}{}^{1}$ = 100Ω

$r_{b}{}^{1}{}_{e}$ = 1kΩ

$r_{b}{}^{1}{}_{C}$ = 4MΩ

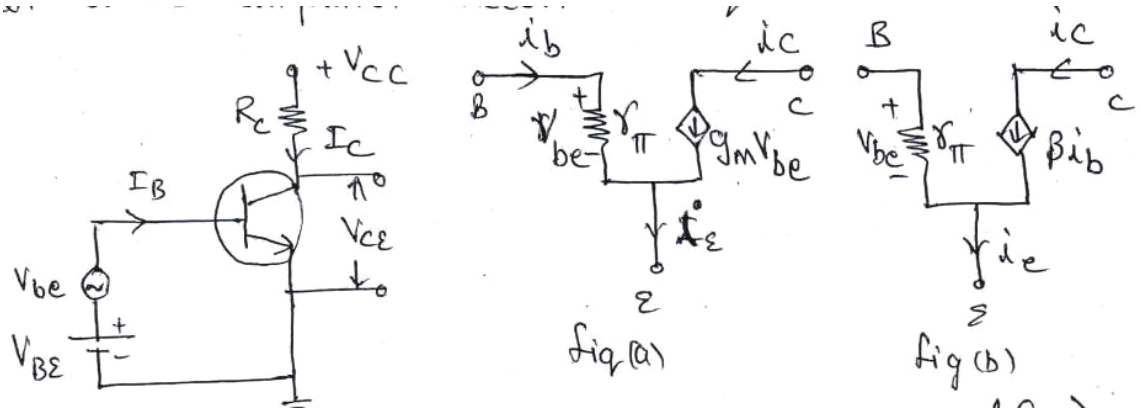
r_{ce} = 80kΩ

$C_{b}{}^{1}{}_{e = Ce}$ = 100PF

C_{C} = 3 PF

10] TRANSCONDUTANCE [gm]

1) consider a CE amplifier shown in fig.1



2) Consider the transistor in active region (amplifier)

a) D.C conditions

$I_C = I_O$.

$I_E = I_C$

$I_E = I_C$

$V_{CE} = V_{CC} – I_C.R_C.$

b) A.C condition.

Total collector current

[Sum of a.c d.c current]

$I_C = I_O$

$= I_O$

$i_C = I_O$.

$i_C = I_c$.

$i_C = I_c$

$i_C = I_c +$

I_C = d.c collector current

= a.c collector current.

Consider a.c component of collector current.

$i_C =$

$i_C = g_m$

Hence trans conductance is ratio of output current (I_C) to input voltage

$G_m = =$

NOTE:

1) g_m is slope of curve drawn between I_c and

[this model is valid for $<< V_T$]

2) The base current and the input resistance at the base

3) The emitter current and the input resistance at the emitter.

4) Relation between r_e and g_m

5) Relation between and

6) Voltage gain of CE amplifier is given by

A_V =

11] CE SHORT- CIRCUIT CURRENT GAIN.

1) Consider a single stage CE transistor amplifier with load resistor R_L short circuited fig.1

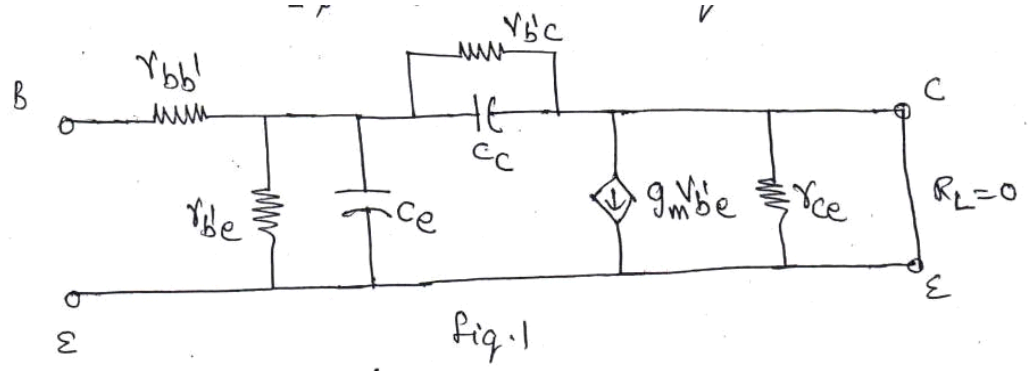
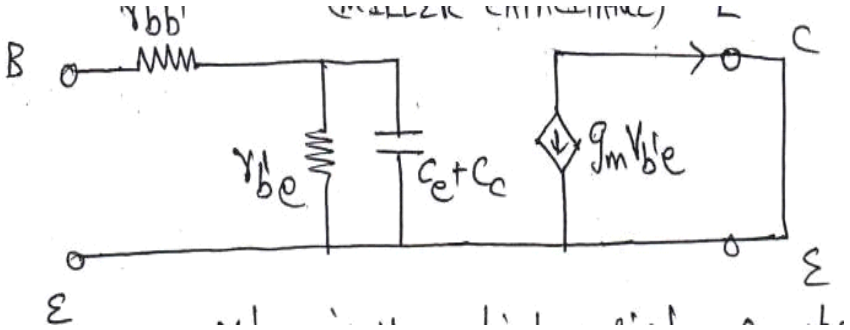


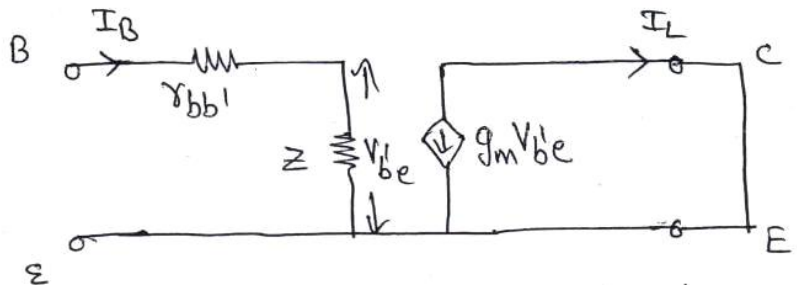
fig.1

(MILLER CAPACITANCE) IL



rb^1c is very hight resistance hence neglected

r_{ce} is shunt to short circuit



$Z = rb^1e \parallel (-j$

Z =

Input voltage $Vb^1e = .Z$

z =

Current gain of CE short circuit is given by

A_I =

A_I = = = =

The above equation indicates that current gain is dependent on frequency f.

At Low frequency A_I -

At Low frequency current gain falls as shown in fig 4.

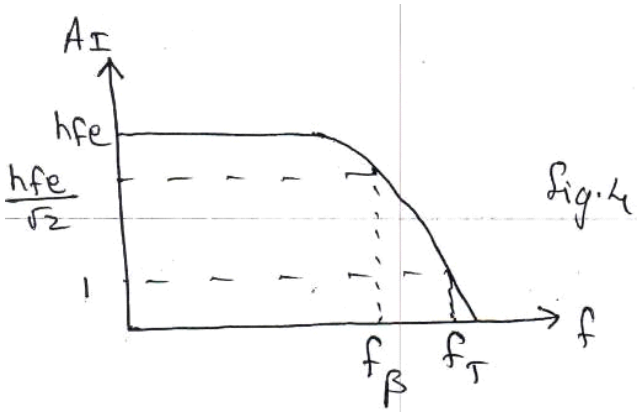


fig.4

At f = , | A_I| =

12) FREQUENCY , ,

a) cutoff frequency .

The frequency at which gain of CE amplifier falls to 3dB or 0.707 from its maximum value is called ‘’

b) cutoff frequency

The frequency at which gain of CB amplifier drops to 3dB or 0.707 from its maximum value is called ‘

At f =

c) cutoff frequency fT

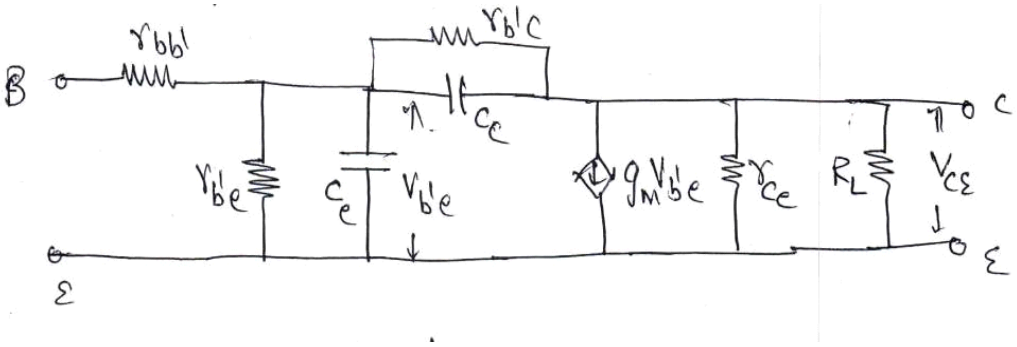
The frequency at which gain of CE short circuit amplifier becomes unity.

F =

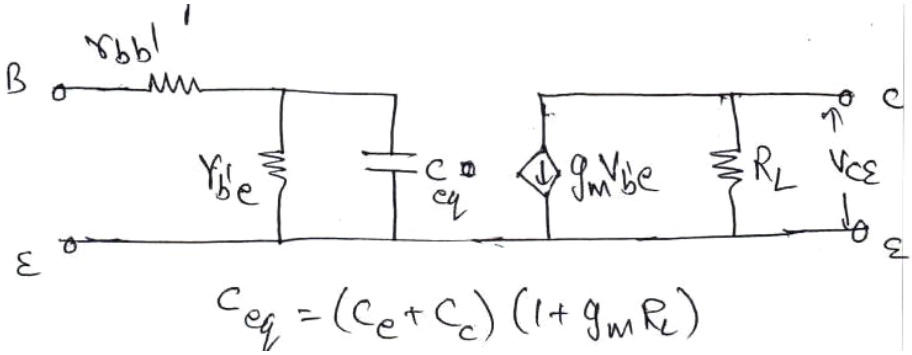
> > 1

13) CURRENT GAIN OF CE AMPLIFIER WITH RESISTIVE LOAD

1) A CE amplifier with is shown below (hybrid)



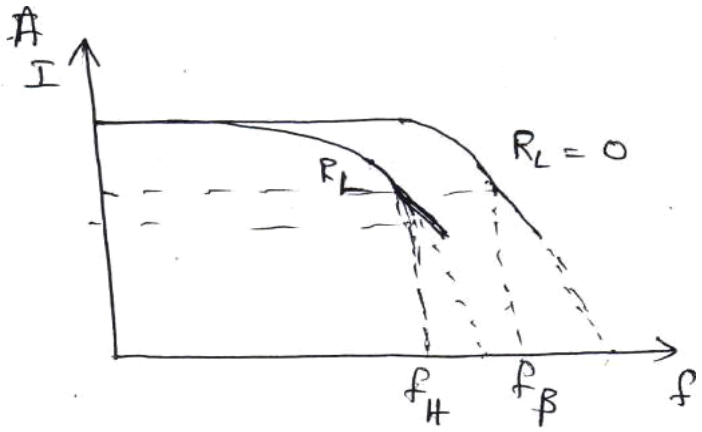
Considering millers theorem.



A_I = = =

At f =

Gain and frequency response is shown below



14) GAIN BANDWIDTH PRODUCT

a) Gain bandwidth product for voltage

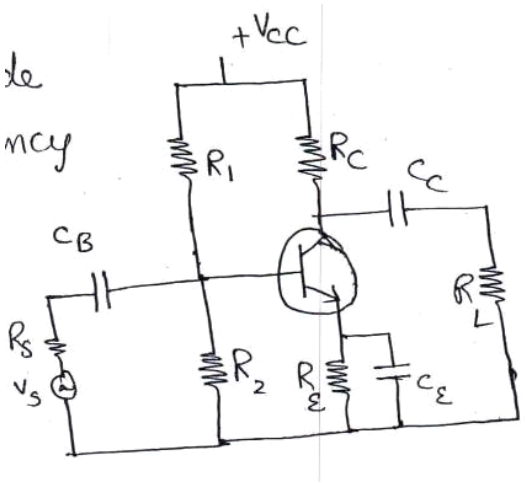
The product of gain and bandwidth is given by.

b) GAIN BANDWIDTH PRODUCT for current

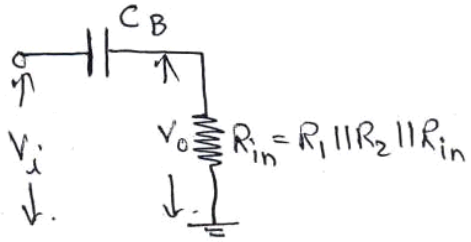
15) SINGLE STAGE CE AMPLIFIER RESPONSE

a) Low frequency analysis of BJT.

1) The capacitors, provide different reactance as frequency varies.



2) Input RC network.

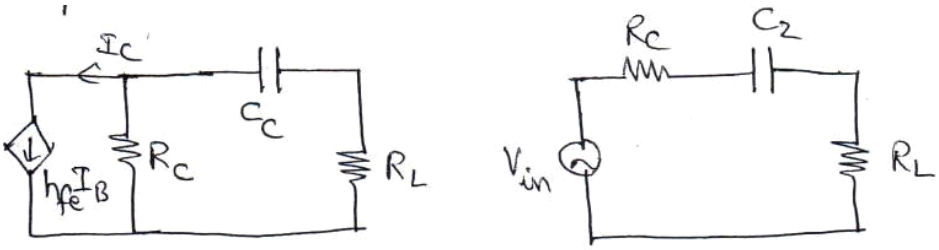


The voltage

At f =

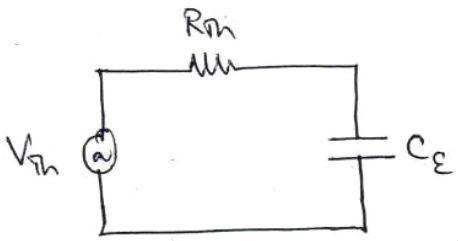
The cutoff frequency

2) Output RC network.



The cutoff frequency is given by

Phase angle

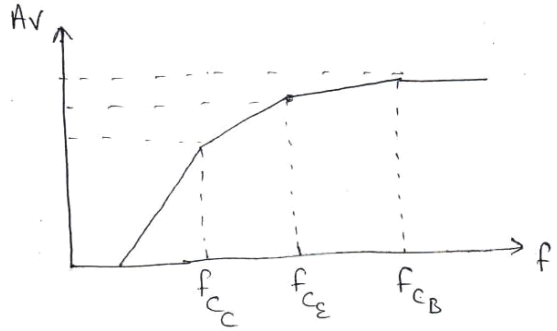


3) By pass RC network

The cutoff frequency is given by

4) Hence each RC network has a cutoff frequency.

The RC network with higher cutoff frequency will be dominant network, which determines the over all gain. Beyond the frequency the gain drops at – 20dB/dec



is highest hence capacitance is dominant pole.

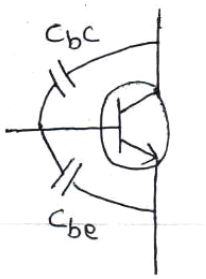
40) b) high frequency analysis of BJT

1) The capacitors C_B, C_c, C_E acts as short circuit at high frequency. Therefore they do not affect the amplifier gain frequency response.

2) At high frequency, the internal stray capacitance effect the gain of amplifier.

→ Collector base junction (Transition capacitance)

→ Base emitter junction (diffusion capacitance)

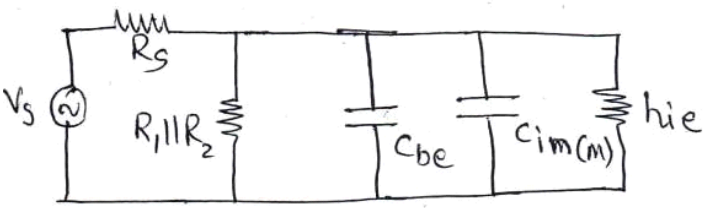


3) Considering miller effect of capacitance for CE amplifier

C_{in} (m) $= C_{bc}(1+A_V)$

C_{out} (m) $= C_{bc} = C_{bc}$

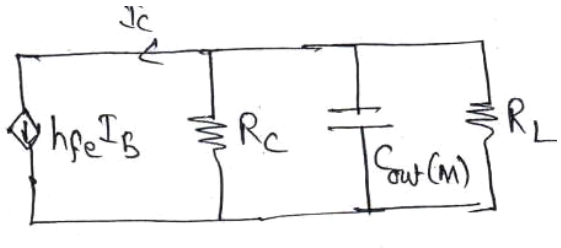
4) INPUT RC NETWORK



The cutoff frequency

Phase angle

5) OUTPUT RC NETWORK



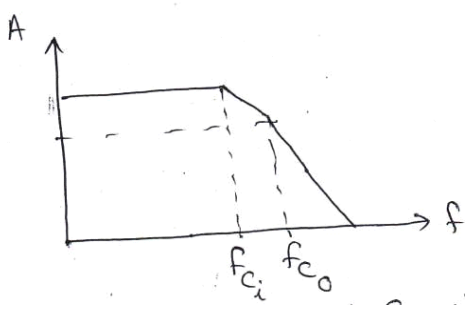
The cutoff frequency

R =

C =

Phase angle

6) The response of circuit is decided by lower cutoff frequence out of the two frequencies , .



is lower than hence the input capacitance dominates the response of amplifier with change in frequency.

ASSIGNMENT – I

1) explain the importance of gain in decibel in decibel unit.

2) Explain the frequency response of amplifier at low and high frequencies.

3) In a single stage RC coupled CE amplifiers, expain the effect of by pass and coupling capacitor.

4) Explain BJT hybrid model.

5) derive expression for trans conductance g_m.

6) Prove that the hybrid model the diffusion capacitance is proparional to the emitter bias current.

7) Consider CE single stage with a resistive load R_L, using millers theorem find out input capacitance at mid band frequencies and high frequencies.

8) Explain how the parameters of hybrid model varying with I_E , V_{CE} and temperature.

9) Derive the expression for CE short circuit current gain A_I as a function of frequency using hybrid model.

10) Derive the expression for CE amplifier current gain with resistive load.

11) Define , , and give relation between ,

12) Explain low frequency response of CE amplifier.

13 Explain high frequency response of CE amplifier.

14) Derive expression for gain band width product

15) derive F_L and f_H for n stage cascade amplifier comment on bandwidth of cascaded amplifier.

ASSIGNMENT – 2

GAIN

1) for an amplifier, mid band gain 100 and lower cutoff frequency is 1KHZ. Find the gain of an amplifier at frequency 20hz.

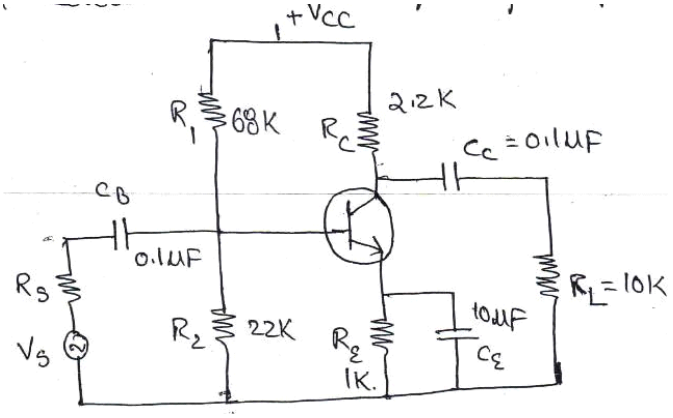
Ans = 2

2) For an amplifier, 3dB gain is 200 and higher cutoff frequency is 20khz. Find the gain of am amplifier at frequency 100 Khz.

Ans = 115.47

3) determine the low frequency response of the amplifier shown below. Draw the frequency response.

Ans:



4) at I_C = 1MA and V_{CE} = 10V, a certain transistor data shows = 3PF, = 200 and w_T =-500 M rad/sec

Calculate g_m , = and

Ans (g_m = 38.46 MA/V, , , = 2.5 M rad/sec)

5) Short circuit CE current gain of transistor is 25 at a frequency of 2Mhz. it = 200khz. Calculate

i) ii) iii) A_I at frequency of 10 Mhz and 100 MHZ

Ans (50 Mhz, = 250, A_I = 5 and 0.5)

6) for a BJT amplifier, the following values one known.

Operating temperature T = 300^0 k, I_{Ca} = 2MA, $r_{bb}{}^1$ = 100 Ω, = 1000Ω, = 2MΩ,

r_{ce} = 810KΩ, f_T = 50Mhz. obtain the h-parameter if K = 1.38 j/^{o}k and q = 1.6 10^{-19}

Ans (g_m = 77.23 A/V, = 5 =51.619)

7) A BJT has following parameter measured at I_C = 1MA, f_T = 4 Mhz

Find , and $r_{bb}{}^1$ for R_L

Ans (g_m = 0.038 A/V, , r_{bb}^1 = 400 Ω, f_H = 637.64 khz)

8) Given the following transistor measurement made at I_C= 5MA, V_{CE} = 10V and at room temperature A_{Ie} = 10 at 10 MHz, C_e = 3PF.

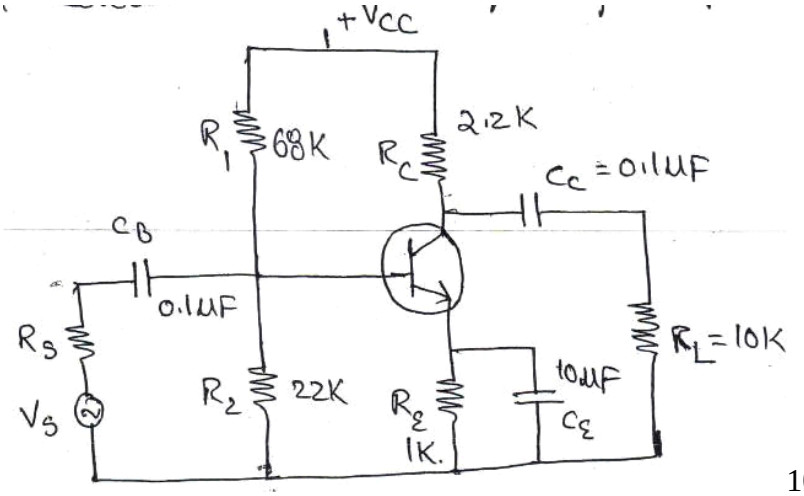
Find C_e , , and r_{bb}^1

Ans (C_e = 304 PF, , r_{bb}^1 = 80 Ω, f_T = 100.05 mhz)

9) The amplifier shown in fig below uses a BJT with g_m= 0.2 A/V, C_e = 200 PF, r_{bb}^1 = 100 0 Ω, C_c = 4PF,

Draw hybrid circuit and find $A_{V(mid)}$,

Ans (-100,

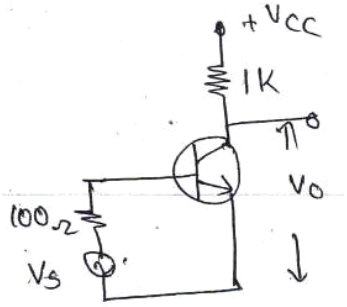


10) The hybrid –

parameters of the transistor used in the circuit of fig.below are g_m = 50 m A/V, C_e = 100 PF, , r_{bb}^1 = 100 Ω, C_c = 3PF,

Find a) upper 3dB frequency of A_I

b) The voltage gain A_{VS}.



Ans (f_H = 3.77MHZ, A_{VS} = -50)

11) For a single CE amplifier whose hybrid parameters are given below, what is half the value obtained with R_S= 0, Hybrid – parameter, g_m = 50 m A/V r_{bb}^1 = 100Ω, C_C = 3PF, C_e = 100PF.

Ans (R_S = 122.2 Ω)

12) A single stage CE amplifier has upper 3dB frequency of voltage gain f_H = 4 MHz, with a load resistance R_L= 600Ω it the transistor parameter are g_m = 50 m A/V, r_{bb}^1 = 100Ω,C_C = 3PF f_T = 300mHz, h_{fe} = 100.

Find 1) The value of R_S which will result in the required value of f_H.

2) The mid band gain with above value of R_S. Ans (311.8Ω , - 24.88)

13) A high frequency amplifier uses a transistor which is driven from a source with R_S= 0. Calculate value of f_H, if R_L = 1KΩ, Assume typical values of hybrid – parameters.

Ans (fH = 0.629 MHz) (fH = 1.545 MHz)

14) A high frequency amplifier uses a transistor which is driven from a source with R_S = 1K, calculate value of f_H, $A_{V(Low)}$, $A_{V(High)}$, it R_L = 0, R_L = 1KΩ, consider typical values of hybrid – parameters.

Ans (2.95 MHz, fH = 1.2 MHz, AV(Low) = -23.8)

GAIN BRAMDWIDTH PRODUCT

15) If tour identical amplifiers are cascaded each having f_L= 10mHz determine the overall lower 3dB frequency f_L.

Ans (229.9Hz)

16) if foure identical amplifiers are cascaded each having f_H = 100KHz, determine the over all upper 3dB frequency f_H.

Ans (43.5 kHz)

17) Three identical non – interacting amplifier stages in cascade have an overall gain of 1dB down at 30 Hz compared to midband. Calculate the lower cutoff frequency of the individual stages.

Ans (FLn = 15.23 Hz , fL = 7.782 Hz)

18) if the overall lower and higher cutoff frequencies of a two identical amplifier cascade are 600Hz and 18KHz respectively, compute the value of the individual cutoff frequencies of both the amplifier stages.

Ans (FH = 27.97 KHz , fL =386 Hz)

MOS AMPLIFIERS

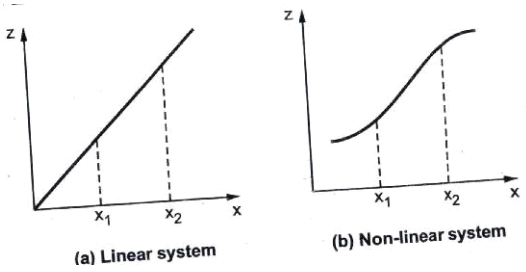
Basic concepts

Usually the input-output characteristics of an amplifier are non- linear. It can be approximated by a polynomial over some signal range:

For the narrow range of x the polynomial can be approximated to

Where : represents the operating point

= Represents the small signal gain



When > > x(t) we have This indicates the linear telationship between the input and output. The fig.4.1.1 (a) and 4.11 (b) shows the input – output characteristic of a linear and non – linear systems

In the design of a high performance amplifier the trade- off between noise. Linearity gain, bandwidth, supply voltage, power dissipation, input/ output impedance, speed and voltage swings impose many challenges. This is illustrated by the analog design octagon shown in fig. 4.1.1

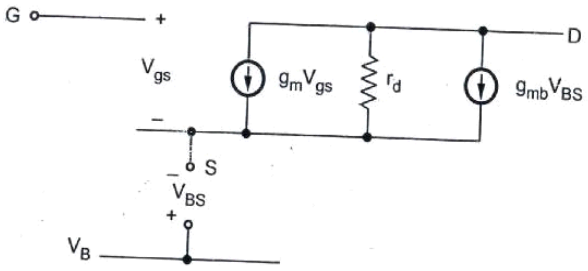
Noise Linearity

Gain

Speed

MOS small signal model

The fig shows the MOS small signal low frequency model. We know that the drain current is a function of the gate- source voltage. This is represented by a voltage dependent current source g_m V_{gs} in the model. The resistance between D and S is represented by r_o. it is the change in drain current due to the change in drain source voltage and it is given by



The drain current also changes due to a change in the back gate bias. This dependence is represented by another current source V_{bs} connected between D and S. in saturation g_{mb} can be given by

Neglecting the body effect the MOS small signal low frequency model is as shown in the fig

At the frequency, device capacitances have their own significance and they are represented in the model as shown in the fig.

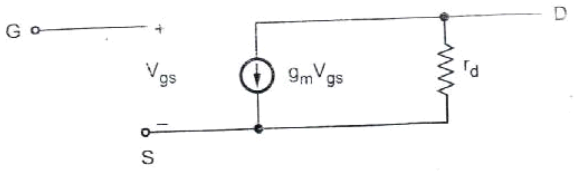


Fig. 4.2.2 MOS small signal low frequency model

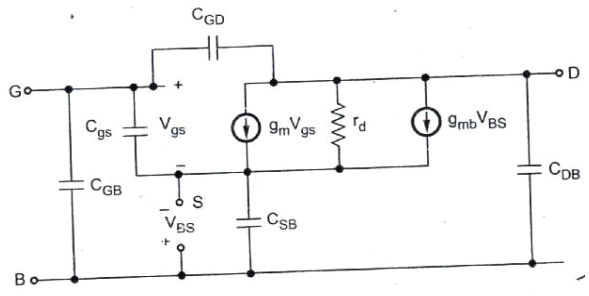


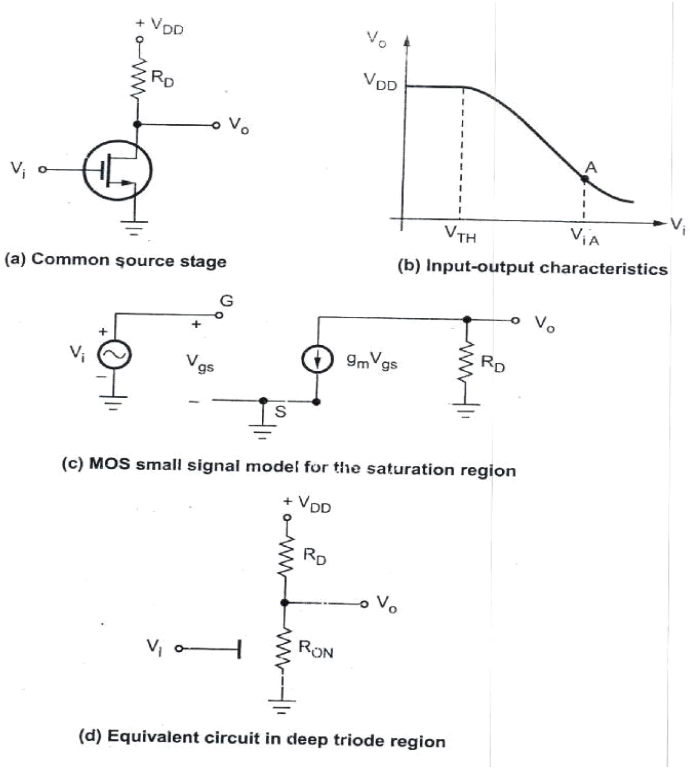
Fig. 4.2.3 MOS small signal high frequency model

Common source amplifier with resistive load

The fig shows a common source stage of MOSFET amplifier. Here, the variations in the gate-source voltage produce variations in the drain current. This current passes through a drain resistance (R_D) to generate an output voltage.

Operation

When $V_i = 0$, MOSFET is OFF and $V_0 = V_{DD}$. As V_i increases from zero and approaches V_{TH}, MOSFET start to turn on. Due to this, drain current I_D starts flowing through R_D reducing V_o. as we go on increasing V_i and if V_{DD} is not excessively low, M_1 goes in saturation. In saturation V_o is given by,



(a) Common source stage

(b) Input-output characteristics

(c) MOS small signal model for the saturation region

(d) Equivalent circuit in deep triode region

If we further increase V_i , V_o drops more and the MOSFET continues to operate in saturation until V_I exceeds V_o by V_{TH} as indicated by point A in the fig At point A, we have

In the triode region, $V_i > V_{iA}$ and V_o is given by

If V_i is large enough to drive MOSFET into deep triode region, $< < 2$ and from the equivalent circuit (See fig) we have

Voltage gain

Since itself varies with the input signal and it is given by

The equation (4.3.4) indicates that the gain of the circuit varies significantly with the signal swing if input signal (V_i) is large and in this case circuit operates in a large signal mode. The dependence of the gain upon the signal level leads to nonlinearity and this is nor desirable.

Maximizing voltage gain

We have

From equation (4.3.5) we can observed that, magnitude of A_V can be increased by increasing W/L or V_{RD} or decreasing I_D if other parameters are constant.

Trade off

- There is limitations on increasing device size, since larger device size leads to greater device capacitances.
- Higher V_{RD} limits the maximum voltage swings.

- Higher value of R_D increases output time constant and makes channel length modulation effect significant.

Thus more is a trade – off between gain, bandwidth and voltages swings.

Including effect of channel length modulation the voltage gain is given by

Using

The fig shows the small signal model for CS stage.

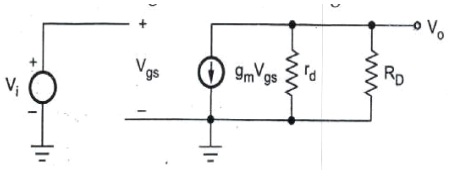


Fig. 4.3.2 Small signal model for CS stage

From the fig we have,

$V_o = g_m V_{gs}$

The expression for A_V in equation 10 and 9 are same, however, later one if easy to derive.

UNIT-III

FEEDBACK AMPLIFIERS

1) Feed back

feed back is a process in which part of outputn(i.e.faction) is fed back to input signal.

feedback improves performance of amplifier by reducing noise and distorstion and maintains stability.

2) Types of feedback

There are two types of feedback

i) Positive feedback

ii) Negative feed back

i) Positive feed back

When the input signal and part of output signal are in phase the feedback is called positive feedback.

$V_i = V_s + V_f$

ii) Negative feed back

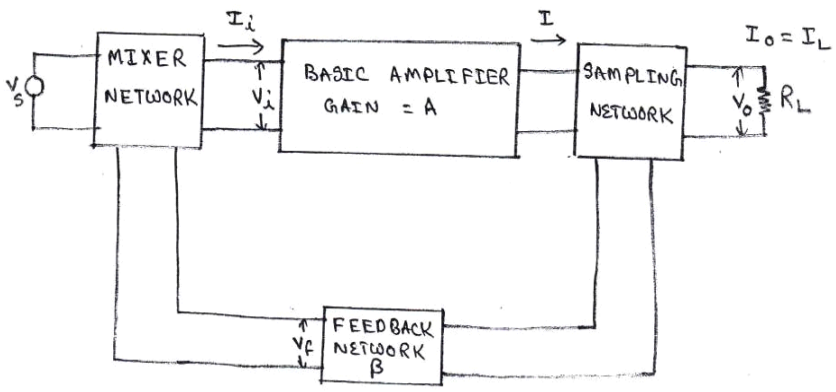
When the input signal and part of output signal (feedback signal) are out of phase, the feedback is called negative feedback.

$V_i = V_s + (-V_f)$

3) Feedback concept

The output voltage or current by means of a sampling network is applied to input through a feedback two part network, as shown fig.1

At the input the feedback signal is combined with the input signal through a mixer network and is feed back into the amplifier.



i) Sampling network:

There are two ways to sample the output voltage or current. The output voltage is sampled by connecting the feedback network in shunt across the output. The output current is sampled by connecting the feedback network in series across the output.

ii) Feedback network:

If may consists of resistors, inductors, capacitor or only resistive components. it provides reduced portion of the output as feedback signal to the input mixer network.

$$V_f = V_o$$

factor (lies between '0' and '1')

iii) Mixer network:

Like sampling there are two ways of mixing feedback signal with input signal.

There are two methods

1) Series input

2) Shunt input

4) Gain of feedback amplifier

An amplifier with feedback is considered

Let gain of amplifier without feedback = A =

Let gain of amplifier with feedback = A_f

Let input voltage without feedback = V_s

Let output voltage without feedback = V_o

Let the feedback voltage be = 'V_f'

But 'V_f' is fraction of output voltage

Feedback factor

Considering negative feedback

Input signal with feedback

Gain of amplifier with feedback

Divide both denominators is &
numerator with

For positive feed back

Gain with feedback

is positive if , the feed back is turned as negative feed back or degenerative feedback.

is negative if the feedback is tunned as positive feed back or regenerative feed back.

5) Sensitivity

The charge in the gain with feedback is less than the change in gain without feed back by the factor (1 + A).

The fraction change in amplification with feedback divided by the fractional change without feedback is called SENSITIVITY of the transfer gain.

6) De sensitivity

The reciprocal of the sensitivity is called the de sensitivity.

D = 1 +

is called loop gain

7) Frequency response and bandwidth

The gain of amplifier with negative feedback is given by

→ Response at lower cutoff frequency with feed back

cut off frequency without feedback.

Hence from above expression, it is clear that lower cutoff frequency with feedback is less than lower cutoff frequency without feedback a factor (1 +).

→ Therefore by introducing negative feedback low frequency response of the amplifier is improved.

→ Response at higher cutoff frequency with feedback

Hence from above expression it is clear that upper cutoff frequency with feedback is greater than higher cutoff frequency without feedback by factor (1 +).

→ Therefore by introducing negative feedback high frequency response of the amplifier is improved.

→ Band width of the amplifier.

B. = Upper cutoff frequency - lower cutoff frequency.

B. =

Hence from above expression it is clear that bandwidth of a amplifier increases by introducing negative feedback.

8) Frequency distortion

The feedback network may consist of R, l, C components if the feedback network does not contain reactive elements, the overall gain is not a function of frequency under such conditions frequency and phase distortion is substantially reduced.

if reactive components are present in feedback network, the reactance's or these components will change with frequency changing ... As a result gain also changes with frequency.

9) Non linear distortion and noise

Consider a large amplitude signal applied to a stage of an amplifier so that the operations of an active device (i.e, transistor) extend slightly beyond its range of linear operation. As a result of this the output signal is slightly distorted. Now if a negative feedback is introduced to the amplifier stage the voltage gain reduces. But if the input signal is increased by the same amount by which the gain is reduced, the output signal amplitude remains the same (i.e it was without feedback) considering distorting in both cases the distorting is reduced by employing negative feedback

is distortion without feedback.

→ **NOISE**

it has been observed that there are many sources of noise in an amplifier depending upon the active device used in the circuit. It will be interesting to know that with the use of feedback the magnitude of noise (N) is reduces by a factor of (

N = noise without feedback

10) Stabilization of gain

The gain with negative feedback of amplifier

On differentiation with respect ‘A’

fractional change in amplifier voltage with feedback.

fractional change in amplifier voltage with out feedback.

‘sensitivity’ it indicates ratio of percentage change in voltage gain with feedback to the percentage change in voltage gain without feedback.

‘de sensitivity’ it indicates the factor by which the voltage gain has been reduced due to feedback.

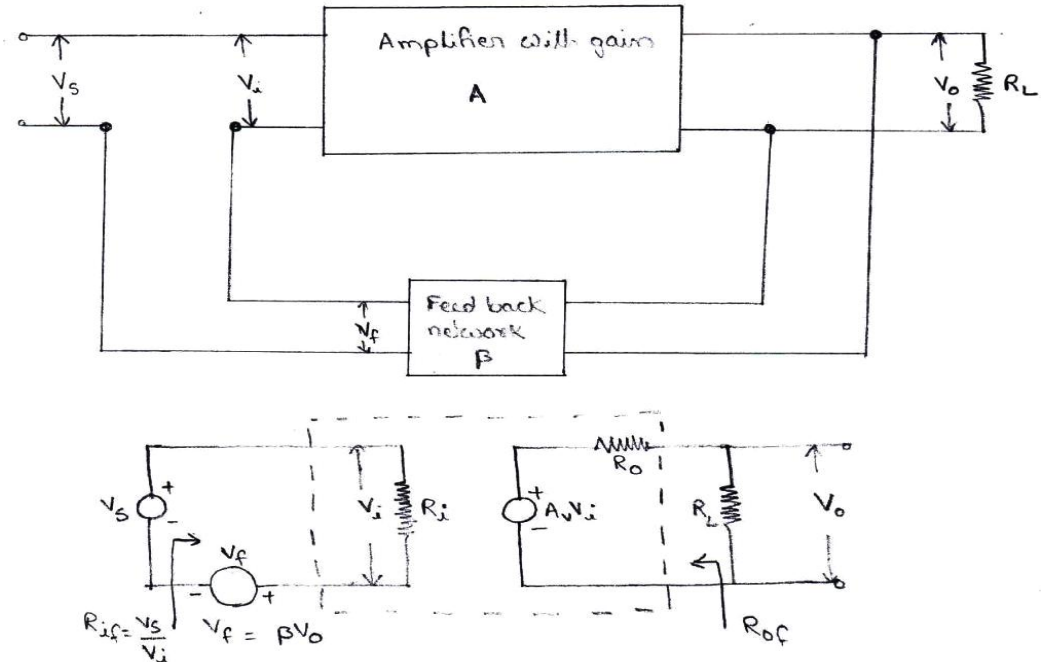
A. voltage – series feedback connection

1. The block diagram of a voltage series feedback is shown in fig. Below.

2) The input to the feedback network is in parallel with the output of the amplifier. A fraction of the output voltage through the feedback network is applied in series with input voltage of the amplifier.

3) The shunt connection at the input increases the input resistance

4) The amplifier in this case is a true voltage amplifier the voltage feedback factor is given by



Input resistance

Considering input loop in fig 2.

By using KVL

Hence input resistance with feedback increases by factor than input resistance () without feedback.

Output resistance

For determining output resistance,

is disconnected and V_s is set to zero.

A external voltage ‘V’ is applied across the output terminals and the current I delivered by ‘V’ is calculated.

By applying KVL to output loop

V = A + I

Hence, output resistance with feedback decreases by (1+) than output resistance without feedback.

B. Voltage shunt feedback

1) A voltage shunt feedback block diagram is shown below in fig.1

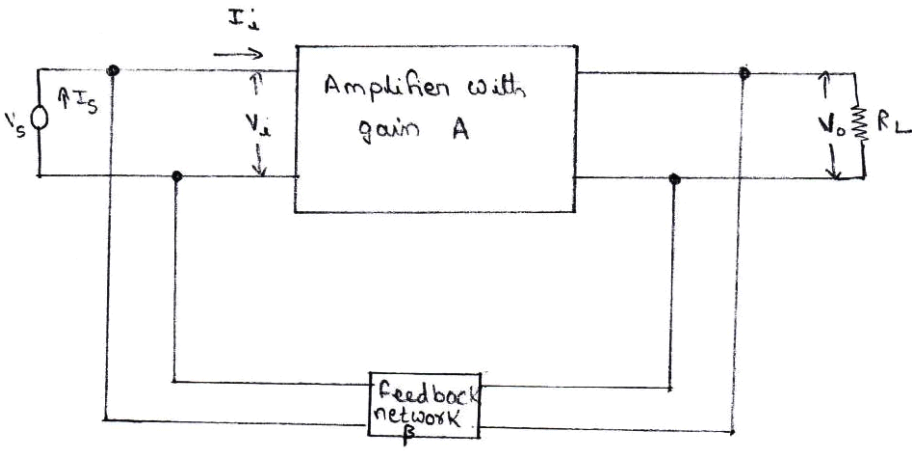
2) The fraction of the output voltage is supplied in parallel to input voltage through the feedback network.

3) The feedback signal is proportional to the output voltage.

Feedback factor

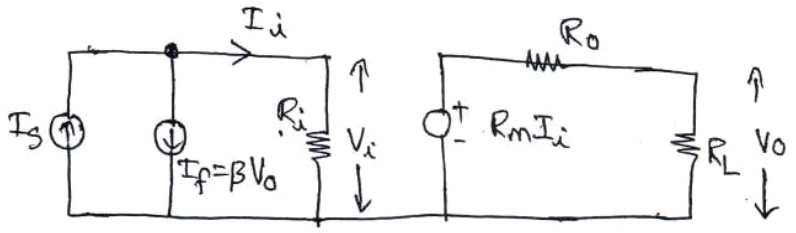
This type of amplifier is called a trams resistance amplifier.

4) The voltage shunt feedback provides a stabilized overall gain and decreases both input resistance by a factor



The voltage shunt feedback topology is shown below.

The amplifier input circuit is represented by Norton's equivalent circuit and output circuit is represented by terminals equivalent.



KCL at input node

Output voltage is given as.

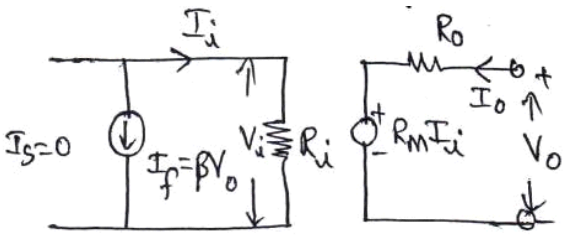
= open circuit trans resistance without feedback

trans resistance without feedback taking load resistance using in eq(1)

Input resistance

with feedback is given by

Output resistance



The output resistance is calculated by open circuiting input source and eliminating at output.

KVL to output loop

Input current

Using in eq (1)

C) Current series feedback

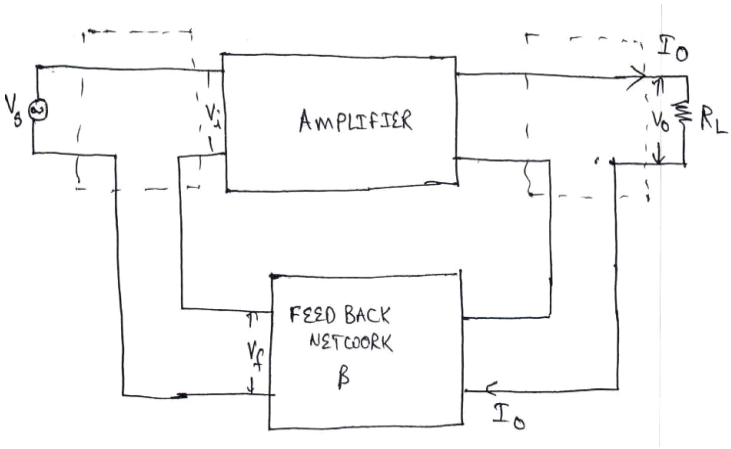
1) The block diagram of a current series feedback is shown below

2) In current series feedback, a voltage is developed which is proportional to the output current.

3) Because of the series connection at the input and output the input and output resistance get increased. This type of amplifier is called trans conductance amplifier.

4) The feedback factor is given by

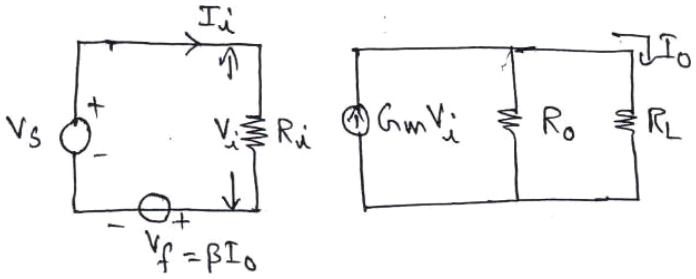
5) Input resistance



Output resistance

The current series feedback topology is shown below.

The amplifier input circuit is represented by Theremins equivalent circuit and output circuit by Norton's equivalent circuit.



KVL to input loop

Output loop

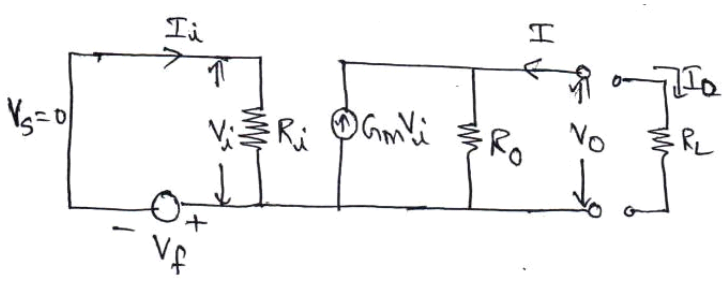
= Trans conductance without feedback.

trans conductance without feedback taking .

Input resistance

Using value in eq(1)

Output resistance



The output resistance can be calculated by short circuiting input source and without at output circuit.

KCL at output node

Input loop

D) Current shunt feedback

1) A current shunt feedback topology is shown below

2) It is called series derived shunt fed feedback system.

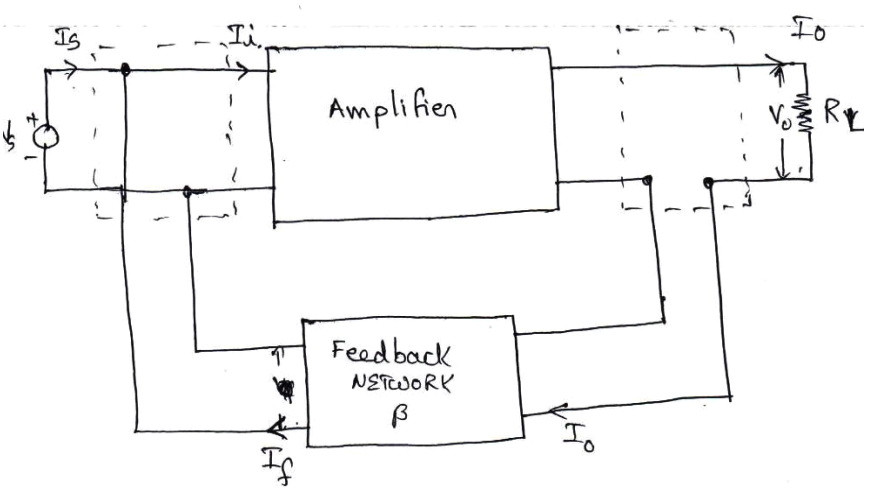
3) in this type of feedback connection, the input resistance is reduced and output resistance is increased.

4) this is a current amplifier.

5) The feedback factor

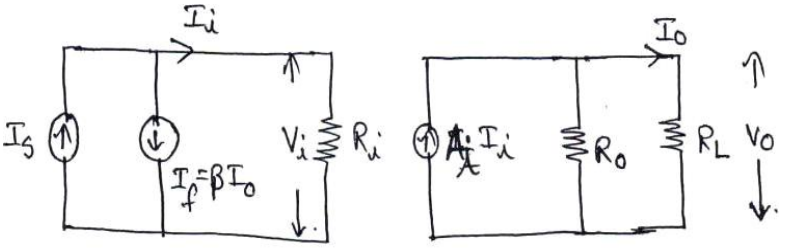
Input resistance

Output resistance



The current shunt feedback topology is shown below

The amplifier input and output is replaced by Norton's equivalent circuit.



KCL at input node

Output current

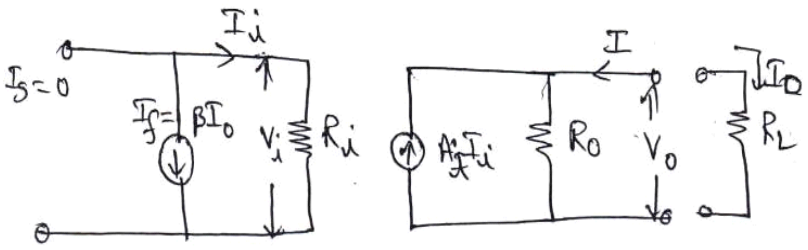
,

Using in eq (1)

Input resistance

Output resistance:

The output resistance is calculated by open circuiting the input source and is removed.



KCL at output node

Input node

[

Using in eq (1)

15) CLASSIFICATION OF AMPLIFIERS.

The amplifiers can be classified into four types.

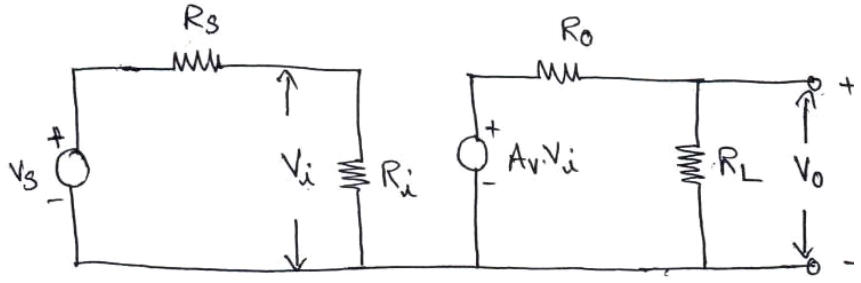
- Voltage amplifier.
- Current amplifier.
- Trans conductance amplifier.
- Trans resistance amplifier.

1) Voltage amplifier

If the amplifier input resistance is large compared with the source resistance then. If the external load resistance is large compared with the output resistance of the amplifier, then.. Such amplifier circuit provides a voltage output proportional to the voltage input, the proportionality factor does not depend on magnitude of the source and load resistance.

Hence this amplifier is called VOLTAGE amplifier. Ideal voltage amplifier has infinite input resistance and zero output resistance

Practical voltage amplifier has



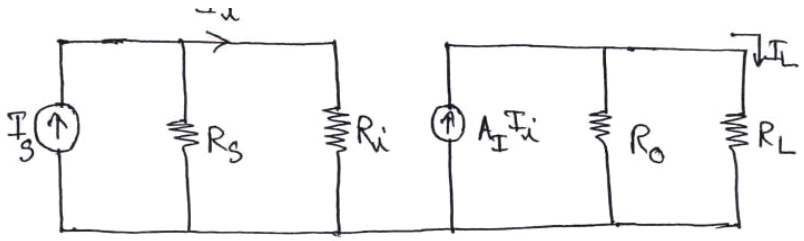
Equivalent circuit of voltage amplifier

2) Current amplifier.

If amplifier input resistance is zero then input current is equal to source current if amplifier output resistance is infinity, then such amplifier provides a current output proportional to the signal input current and the proportionality factor is independent of source and load resistance. This amplifier is called current amplifier.

Ideal current amplifier has = 0 , =

Practical current amplifier has < < , > >



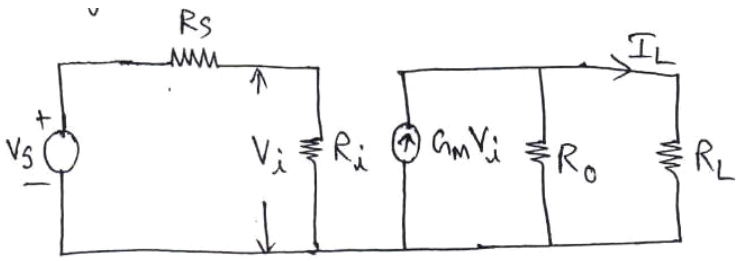
Equivalent circuit of current amplifier.

3)Trans conductance amplifier

In this amplifier, an output current is proportional to the input voltage and the proportionality factor is independent of the magnitudes of the source and load resistance.

Ideally this amplifier has = , =

Practical this amplifier has > > , > >



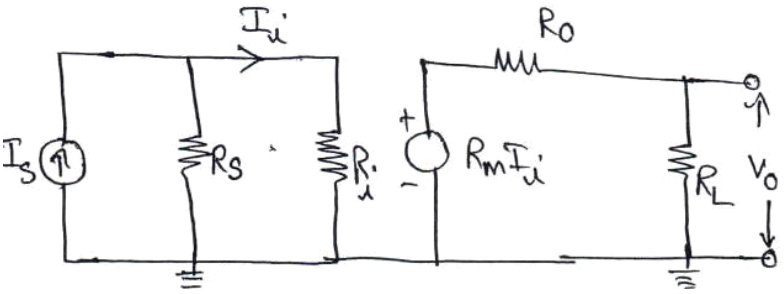
Equivalent circuit of Trans conductance amplifier

4)Trans resistance amplifier

In this amplifier an output voltage is proportional to the input signal current and the proportionality factor is independent of the source and load resistance.

Ideally this amplifier must have zero input resistance and zero output resistance .

Practically << and <<



Equivalent circuit of trans resistance amplifier

16) Analysis of feedback amplifier [identifying topology]

STEP 1) identifies topology.

- Sampling network.

a) by shorting the output $V_o = 0$, if feedback signal (V_f) becomes zero then it is voltage sampling.

b) by opening the output loop i.e. = 0, if feedback signal I_f becomes zero then it is current sampling

- Mixing network.

a) if the feedback signal is subtracted from the externally applied signal as a voltage in the input loop, then it is series mixing.

b) if the feedback signal is subtracted from the externally applied signal as a current in the input loop, then it is shunt mixing.

STEP (2) : finding input circuit

- For voltage sampling make $V_o = 0$ by shorting the output.
- For current sampling make $I_o = 0$ by opening the output loop.

Step (3) : finding output circuit

- For series mixing make $I_i = 0$ by opening the input loop.
- For shunt mixing make $V_i = 0$ by shorting the input.

Step 4): Draw the h-parameter model. For given circuit.

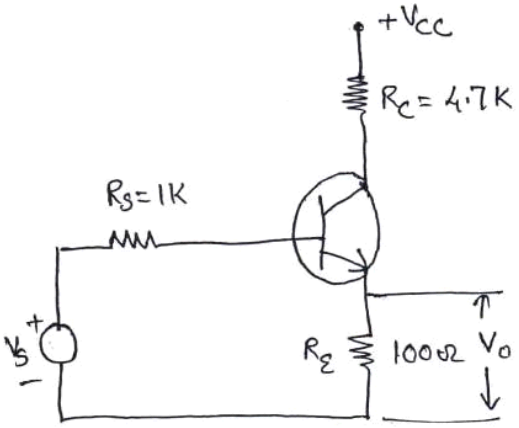
Step(5): Find gain 'A'

Step (6) : find feedback factor '

Step (7): find all parameters.

7) Voltage series feedback:

A emitter follower circuit is example of voltage series feedback.



The voltage across R_E resistor is output voltage, simultaneously R_E resistor voltage is considered for input loop also.

Here, in this circuit is feedback factor is unity.

- Output voltage

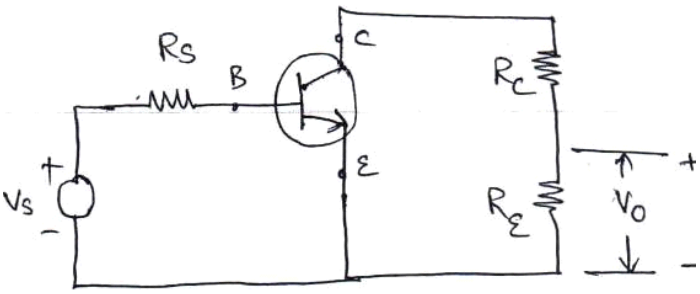
- KVL to input loop

3) If output port is short circuited then feedback signal becomes zero. There voltage sampling is done here.

As the feedback signal ‘’ is subtracted from input signal, their input mixing is series.

Therefore the feedback used in this circuit is voltage series feedback.

4) For finding input and output circuit and a.c analysis the circuit is rearranged.



For input circuit

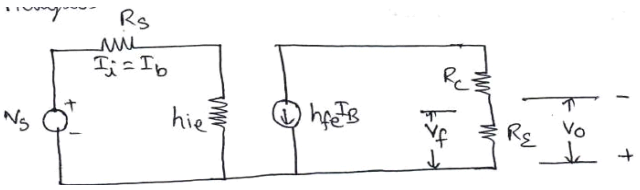
As output sampling is voltage, make output $V_o = 0$.

Then input loop is.

For output circuit,

Now, making input current , , so R_E appears only in output circuit as shown above.

5) A.C analysis



6) Open loop voltage gain:

Feedback factor

De sensitivity D = 1 +

1) Open loop voltage gain

2) Feedback

3) De sensitivity

D = 1+

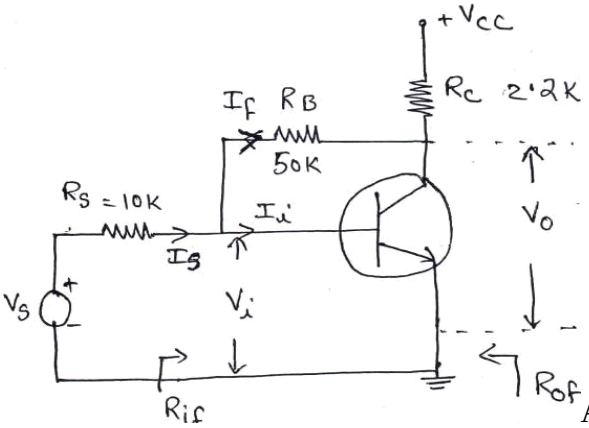
4) Voltage gain

5) Input resistance

= 1000 + 1100 = 2100 Ω

6) Output resistance

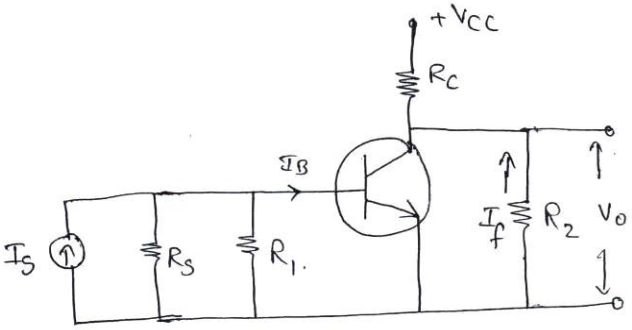
18) Voltage shunt feedback



A collector base bias circuit is example of voltage shunt feedback. The circuit is shown below.

1) By short circuiting the output, V_O becomes zero hence feedback current I_f becomes zero. Hence it is voltage sampling. As the feedback current is given to input the mixing network is shunt network. The topology is called voltage shunt feedback.

Using miller's theorem is rearranged at input and output as R_1 and R_2



To find input circuit set $V_o = 0$, then is connected at base and emitter. To find output circuit, set = 0, then is connected between collector and emitter.

We have

Input resistance

Find

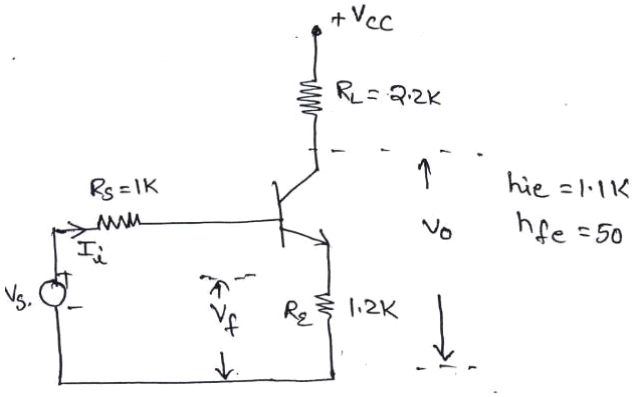
D = 1+

= 2.854

19) Current series feedback

1) The common emitter circuit with un by passed is example of current series feedback.

2) A. CE amplifier is shown below.



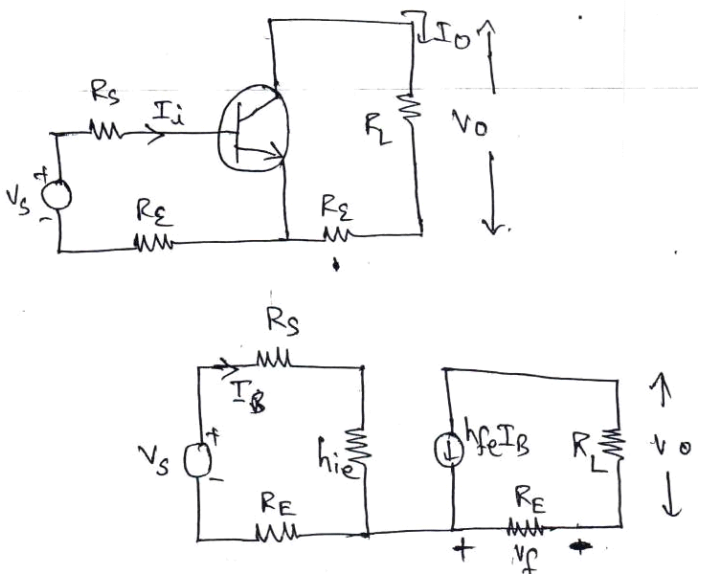
3) The R_E resistor is common to both input and output loop. Therefore voltage across R_E is considered as feedback voltage. V_F

Hence output current I_o = is sampled and it is converted to voltage by feedback network.

Now, feedback back voltage is subtracted from to produce. Hence the circuit uses current series feedback.

4) Input and output circuit

In absence of output current (then R_E belongs only to input when, then belongs to output circuit. Therefore R_E appears in input and output loop. The modified circuit is shown in below.



5) Open loop transfer gain.

Feedback factor

6) Find

[Take the values from ckt.]

1) De sensitivity D = 1 +

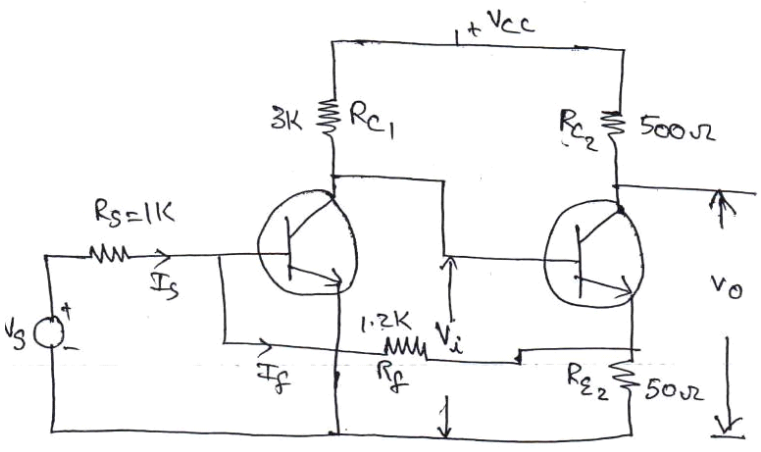
= -1.72

,

,

20) Current shunt feedback.

1) A CE amplifier in cascade mode with feedback can be considered as example of current shunt feedback.



2) Two stage cascaded with feedback CE amplifier is shown below.

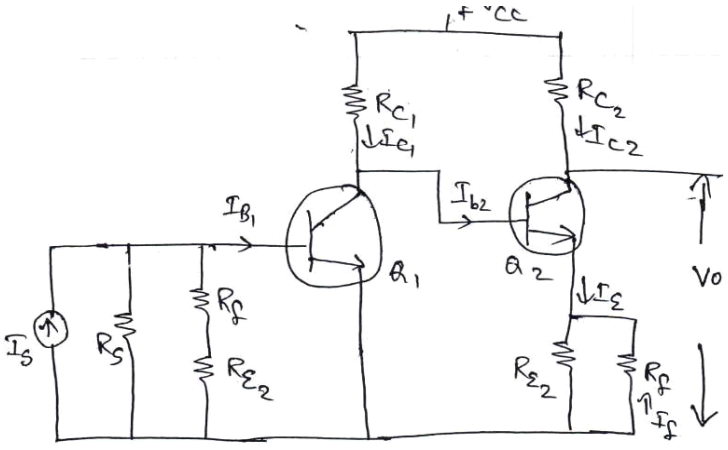
3) The feedback network consists of R_F and the output current = - = - is divided by the two resistors and feedback current is subtracted from and given to . Hence this configuration is current shunt feedback.

4.Input and output circuit.

As the resistor is connected to input and output of Q_1 and transistor respectively. This resistor is replaced in shunt between base and emitter of by making

Similarly making is in parallel to of transistor.

The modified circuit is shown below.



4) Open circuit transfer gain

5) Find

[take the values from ckt.]

1) De sensitivity D = 1 +

= 0.394K

,

,

OSCILLATORS

1) OSCILLATOR

An oscillator is a circuit which generates an a.c signal without a.c input. An oscillator is a signal generator if produces a signal of constant amplitude and constant frequency.

2) Classification of oscillators.

The oscillators are classified based nature of signal , frequency and components, applications.

a) Based on wave forms

b) Relaxation oscillators.

c) Based on feedback

c) Based on frequency generated..

Audio frequency OSC [upto 20 KHz]

Radio frequency OSC [20 KHz to 30 KHz]

Very High frequency OSC [30 MHz to 300MHz]

ULTRA HIGH frequency OSC [300MHZ to 3GHz]

MICRO WAVE frequency OSC.[above 3 GHz]

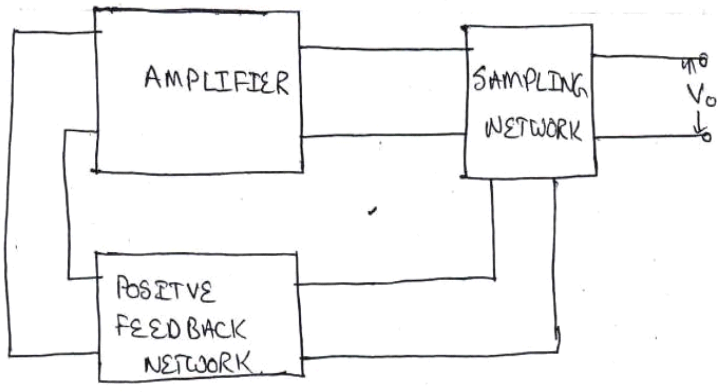
e) Based on components

LC oscillators

RC phase shift oscillators

3) Conditions for oscillations.

1) The oscillator circuit positive feedback. In order to produce oscillations the circuit must satisfy BARHAUSEN criterion. The black diagram of oscillator circuit is shown below.



Block Diagram of Oscillator

2) Barkhausen criterion

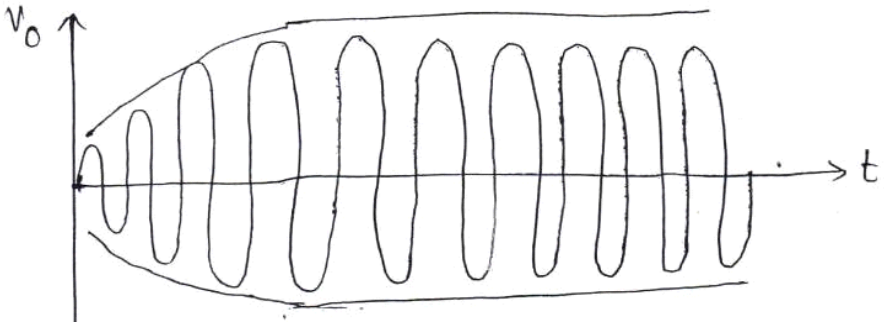
The essential conditions for maintaining oscillations are.

i) $|A| = 1$, magnitude of loop gain should be unity.

ii) The total phase short of feedback signal should be 0^0 or 360^0

3) The condition that loop gain) $|A| = 1$ gives a single and precise values of) A, which should be set throughout the operation of the oscillator circuit , but in practice as transistor character tics and performance of other circuit components change with time, $|A|$ will becomes greater or lesser than unity

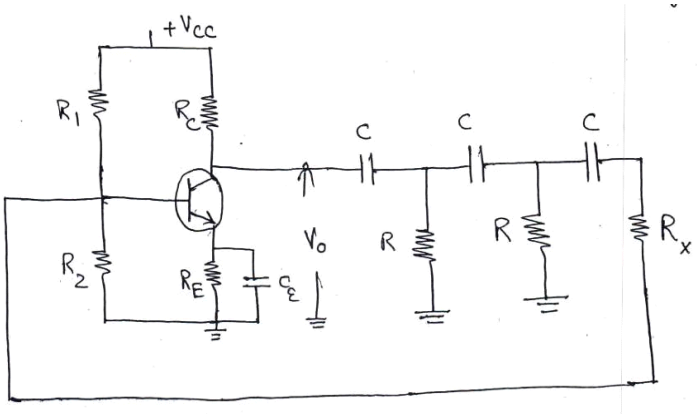
4) Hence in all practical circuits $|A|$ should be set greater than unity so that the amplitude of oscillations will continue to increase without limit.



Sustained oscillations

4) RC- phase shift oscillator

1) The Rc – phase shift oscillator are used in low frequency applications. The feedback circuit consists of resistors and capacitors.



2) A RC phase shift oscillator is shown below in fig.1

3) The circuit consists of CE amplifier with three RC network connected to the feedback path. The feedback used in this circuit is voltage shunt feedback.

4) In order to generate sustained oscillations, the loop gain $A \geq 1$ and phase shift of feedback signal must be 0^0 or 360^0 [BARKHAUSEN criteria]

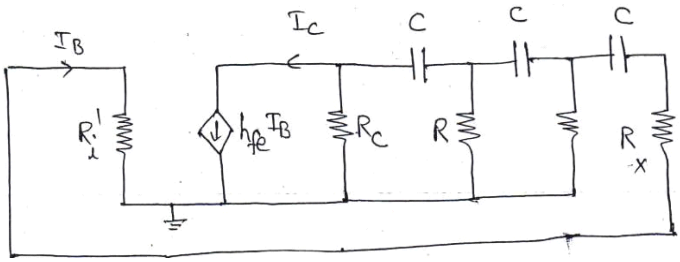
5) Operation:

a) The oscillator circuit is not given any input signal. The output signal V_0 is given to the feedback network. The feedback circuit takes fraction of output gives to input through resistor R_X. the feedback signal I_F is input to oscillator circuit. This signal is amplified again and again until loop gain A is equal to or greater than unity. Once sustained oscillations are developed.

b) The phase shift is provided by RC network. Each RC network introduces a phase shift of 60^0 and in total three RC network provide 180^0

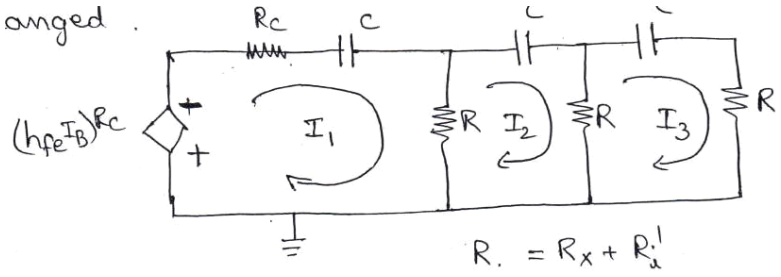
The CE amplifier introduces -180^0 phase shift and RC feedback network introduces 180^0 phase shift hence total phase shift of feedback signal is 0^0 or 360^0

c) As the Barkhausen criteria is satisfied, now the circuit produces sustained oscillations the output is a sinusoidal signal with constant amplitude and frequency.



6) The frequency of oscillator is determined by the feedback network. The h-parameter equivalent circuit model is shown below.

The resistor R_X is in series with the circuit is re arranged.



KVL to loop (1)

-

KVL to loop (2)

KVL to loop (3)

Using 3 equations find and (Cramer's rule).

=

I_3 = output current or feedback current =

On solving above equation, the loop gain is obtained as

Where

To have 0^0 as phase angle of feedback signal the imaginary part is made zero.

Solving for

The frequency of oscillator is given by

Now, the loop gain is unity

$|A| = 1$

Consider real part and equate to unity

The minimum value of must bet 44.54

Hence by changing capacitor and resistors desired frequency of oscillations can be produced.

7) Advantages

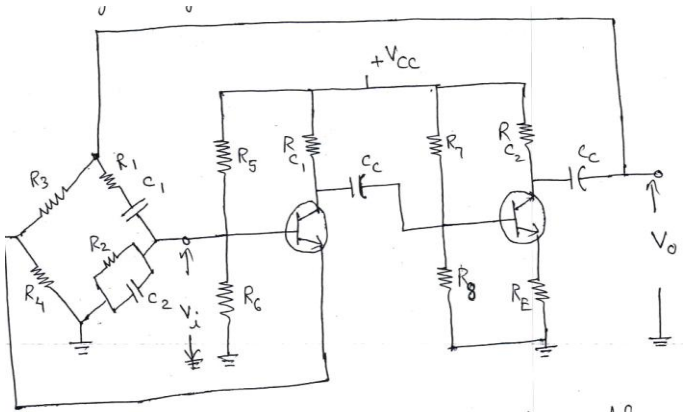
- Simple in design
- Complete audio frequency range is covered.
- Produces sinusoidal output
- Fixed frequency oscillator.

8) Disadvantages

- If frequency has to be altered all capacitors must be changed to same value.
- Frequency stability is poor.

5) Wien – bridge oscillator

- The weign bridge oscillator is a phase shift oscillator used for low frequency applications. The frequency of oscillator can be varied from 10 HZ ti 1MHZ.
- Weight bridge oscillator circuit is shown below.



- The circuit consists of a two stage RC coupled amplifier which provides a phase shift of 360^0 or 0^0. A balanced bridge network used as shown in fig. the feedback is provided by bridge network and no need for any additional phase shift in feedback circuit.
- In order to generate oscillations the loop gain A should be greater than or equal to unity and phase angle of feedback signal should be 0^0 or 360^0 (Barkhausen rule)
- Operation

  a) The oscillator circuit is not provided any input signal the output signal V_0 is given to the feedback network (bridge circuit) the feedback circuit takes fraction of output and gives it to input i.e voltage across R_2 and C_2 parallel branch. This is obtained by voltage division rule.

  b) Now, the amplifier has feedback voltage V_f as input and this signal is amplified again and again in the loop, At certain point the loop gain of amplifier becomes unity or greater than unity and sustained oscillations are developed.

  c) Once Barkhausen condition is satisfied. Sustained oscillations are obtained. The desired frequency can be obtained by varying the capacitor values. By using common shaft both capacitors can be varied simultaneously.

  d) By using wien-Bridge feedback network the oscillator becomes sensitive to a signal of only one particular frequency. Hence good frequency stability is obtained.

  e) The frequency of oscillator circuit is given by

6) Expression for frequency

The feedback voltage

Feedback factor

On solving above equation

To have zero phase shift of feedback network, imaginary part must be zero.

Let = = R, = = C

Consider feedback factor ‘

Consider loop gain | A| ≥ 3.

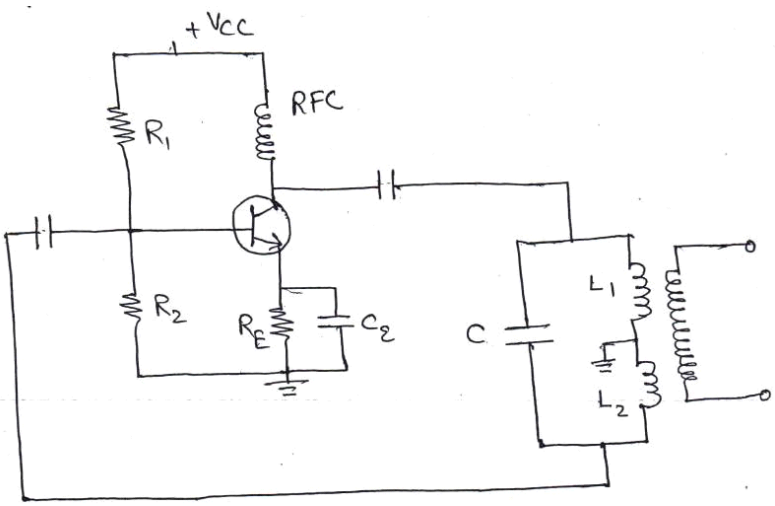
In order produce sustained oscillation the gain of amplifier should be greater than or equal to 3.

LC oscillators

6) Hartley oscillator

1) The LC oscillator use inductor and capacitor (tank circuit) for producing oscillations. These oscillators are used for high frequency range from 200 KHz up to few GHz.

2) A Hartley oscillator circuit is shown below.



3) The circuit consists of CE amplifier with a LC tank circuit connected to output of amplifier. A coil called RFC (radiofrequency choke) is connected between the collector and V_{cc} supply

4) The feedback circuit consists of a tank circuit .it consists of two inductors L_1 and L_2 the inductorL_1 is inductively coupled to coil L_2 and the combination works as an auto transformer. A capacitor 'C' is connected in shunt with inductors L_1 and L_2

5) In order to generate oscillations, the loop gain A should be greater than or equal to unity. The phase angle of feedback signal should be 0^0 or 360^0 [Barkhausen rule]

6) Operation

a) The output of amplifier is taken at collector and given to feedback network. The feedback network (LC) takes fraction of output and gives to input hence the oscillator has feedback voltage V_f as input V_i. this signal is amplified again and again at certain point the loop gain becomes unity or greater than unit by which oscillations are developed.

b) The CE amplifier introduces 180^0 phase shift and the feedback network introduces a phare shift of 180^0.

Hence total phase shift is 360^0 or 0^0

c) As conditions for oscillations are satisfied (barkhusen criteria) now sustained oscillations are produced.

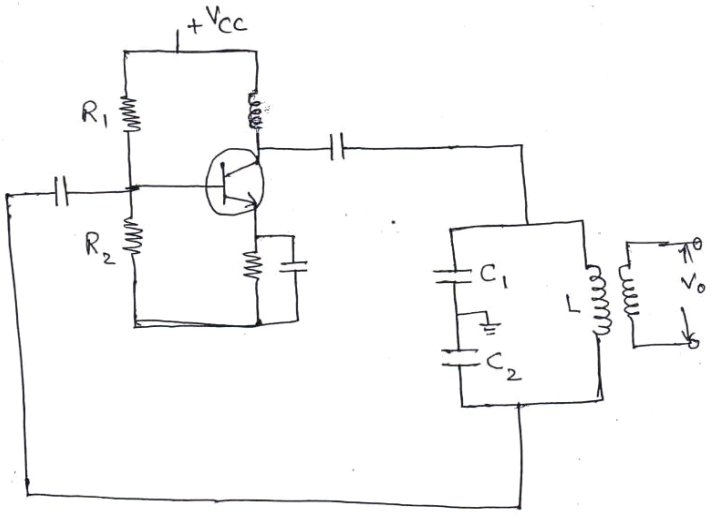
d) The transistor should be for oscillation to start.

e) When the circuit is energized by switching on the supply, the collector current flows, then oscillations are produces be caused of positive feedback from the tank circuit.

f) The frequency of oscillations are given by

7) Colpitt's oscillator

1) The LC oscillators use inductor and capacitors (tank circuit) for producing oscillations. These oscillators are used for high frequency range from 200 KHz to few GHz.



2) A colpitts oscillator circuit is shown below.

3) The circuit consist of CE amplifier with a LC tank circuit connected to output of amplifier. A coil called RFC (Radio frequency choke) is connected between the collector and V_{cc} supply.

4) The feedback circuit consists of a tank circuit. It has two capacitors C_1 and C_2 and a inductor L in shunt with capacitors. The output is taken at secondary of coupled coil with inductor L

5) In order to generate oscillations the loop gain A should be greater than or equal to unity. The phase angle of feedback signal should be 0^0 or 360^0 [Barkhausen Criteria].

6) Operation

a) The output of amplifier is taken at collector and given to feed back network. The feedback network (LC) takes fraction signal acts as input to amplifier. This signal is amplified again and again, at certain point the loop gain becomes unity or greater than unity by which oscillations are developed.

b) The CE amplifier introduces 180^0 phase shift and the feedback network introduces a phase shift of 180^0.hence total phase shift is 0^0 or 360^0 hence the feedback is positive.

c) As conditions for oscillations are satisfied (Barkhausen criteria) now sustained oscillations are produced.

d) The transistor = , for oscillation to start.

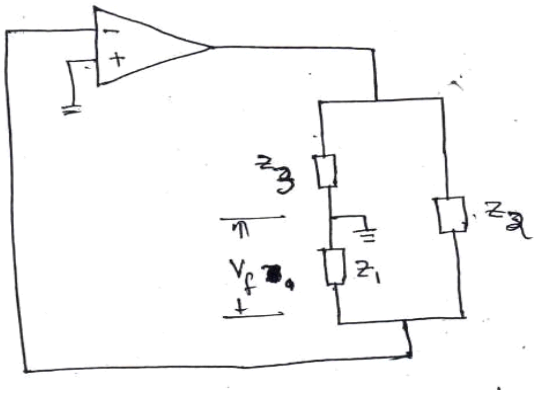
e) When the circuit is energized by switching on the power supply, the collector current flows. Then oscillator is produced because of positive feedback from the tank circuit.

f) The frequency of oscillations are given by

7) Expression for frequency of oscillations

{HARTLEY & COLPITTS]

Consider the following feedback amplifier circuit

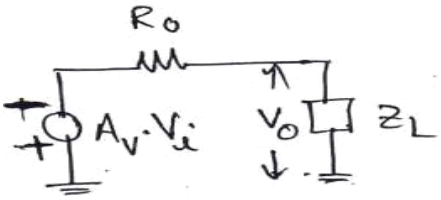


The feedback voltage is given by

Feedback factor =

As phase of feedback network is 180^0

Consider therein equation circuit of amplifier



Gain of amplifier

Consider equation (1) and multiply both sides by A.

According to Barkhausen criteria – A=1, for oscillations

This is required Loop gain, substituting value.

Are purely reactive elements

To have 180^0 phase shift the imaginary part of the denominator must be zero.

i.e.

According to the Barkhausen criterion must be positive and greater than or equal to unity. As is positive is positive, then will be positive only when and will have same sign. That is and must be of same type of reactance either both inductive or capacitive.

→ if are inductive then is capacitive then circuit is Hartley oscillator

→ if are inductive then is indicative then circuit is colpitts oscillator.

a) For Hartley oscillator, frequency is obtained by.

b) For colpitts oscillator the frequency is obtained by

8) Crystal oscillator

- The crystal oscillator is basically a tuned oscillator. The crystal oscillator uses a piezo electric crystal as a resonant tank circuit.
- The crystal is usually made of quartz material and provides a high degree of frequency stability and accuracy.
- A slab is mounted between two metal plates and housed in a package which is equal to the size of postal stamp. The package as a whole is known as crystal and its symbol is shown in fig.1
- When a crystal is placed across an a.c source its starts vibrating. The amount of vibrations depends upon the frequency of applied voltage.
- A crystal oscillator circuit is shown in fig.2. A crystal is connected as a series element in the feedback path from collector to the base.
- The circuit frequency of oscillations is set by the series – resonant frequency of the crystal equivalent circuit shown in fig.3
- The frequency of crystal oscillator is given by

- The changes in supply voltage transistor device parameters have no effect on the circuit operating frequency, which is held stabilized by the crystal.

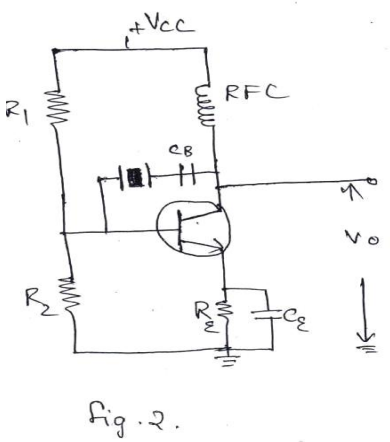


fig. 2.

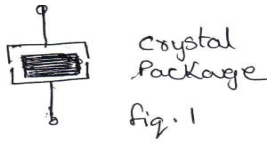


fig. 1

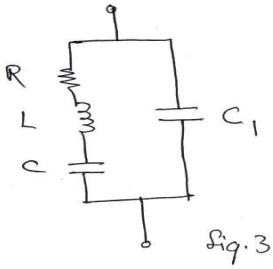


fig. 3

Equivalent Circuit of Crystal.

9) Frequency stability of oscillator

- The frequency stability of an oscillator is a measure of its ability to maintain the required frequency as precisely as possible over a long time interval as possible.
- The accuracy of frequency calibration required may be anywhere between 10^{-2} and 10^{-10}
- The main draw back in transistor oscillator is that the frequency of oscillation is not stable during a long time of operation. The following are the factors which contribute to the change in frequency.

  a) due to change in temperature the values of the frequency determining components viz resistor, inductor and capacitor will change.

  b) Due to variation in the power supply unstable transistor parameters change in climatic conditions and aging.

  c) The effective resistance of the tank circuit is changed when the load is connected.

- Due to variation in biasing conditions and loading conditions.

The variations of frequency with temperature is given by

Where , are the desired frequency of oscillation and the operating temperature respectively.

- As PIEZO ELECTRIC crystal have high Q values of the order of 10^5 they can be used as parallel resonant circuit in oscillators to get very high frequency stability of 1 ppm.

ASSIGNMENT – I

- Define oscillators how are oscillators classified ?
- What type of feedback is employed in oscillators? What are the advantages? Discuss the condition for sustained oscillations.
- What is Barkhausen criteria? Explain.
- Explain Hartley oscillator and derive the expression for frequency.
- Explain eoLLPIS oscillators and derive the expression for frequency
- Draw the circuit diagram of a Rc phase shift oscillator using BJT. Derive the expression for frequency of oscillation of RC – phase shift oscillator using BJT.
- Explain the principle of operation of a weign bridge oscillator with the help of a neat diagram obtain an expression for its frequency of oscillations.

  Show that the gain of weign bridge oscillator using BJT amplifier must be at least 3 for the oscillations to occur.
- What is piezo electric effect? Explain the working of crystal oscillator?
- What is the range of frequency over which a crystal oscillator may be normally used and why?
- What are the advantages and limitations of a crystal oscillator?
- Explain briefly about frequency and amplitude stability of oscillators.

ASSIGNMENT -2

1) in Hartley oscillator, calculate L_2 IF L_1 = 15 mH Sc = 50PF mutual inductance of 5 and the frequency of oscillations is 168 Hz.

2) In a transistorized Hartley oscillator the two inductance are 2mh and 20 while the frequency is to be changed from 950 KHZ to 2050 KHZ. Calculate the range over which the capacitor is to be varied.

(Ans: C= 2.98FF , to 13.89 PF)

3) A colpitts oscillator has , C_1 = 0.001, C_2 = 0.001 and L = 5 . What is approximate frequency ? what will be the new frequency it the value of L is doubled ?

What should be the inductance to double the frequency ?

(Ans f =3.183mHz, L = 1.25 H)

4) For phase shift oscillator the feedback network uses R = 6Ω and C = 1500PF. The transistorized amplifier used, has a collector resistance of 18Ω. Calculate the frequency of oscillations and minimum value of of the transistor.

(Ans: f = 4.168 KHZ,)

5) find C and of a transistor to provide f_0 of 50 KHZ of a RC transistorized phase shift oscillator.

Given,

(Ans: C = 111.062Pf,)

6) A crystal has L = 0.1H, C = 0.001PF, R = 10 KΩ, and C_M = 1 PF. Find the series resonance and a factor

(Ans:)

7) A crystal has L = 2H , C = 0.01 PF and R = 2Ω its mouting capacitance is 2 PF. Calculate its series and parallel resonance frequency.

(Ans: C_M = 2PF, ,)

8) A crystal L = 0.4H, C = 0.085PF and C_M = 1 PF with R = 5KΩ. find.

- Series resonant frequency.
- Parallel resonant frequency.

- By what percent does the parallel resonant frequency exceed the series resonance frequency ?
- Find the Q factor of crystal.

(Ans:)

9) A crystal has L = 0.1H, C = 0.01PF, R = 10 KΩ and C_M = 1PF find

- Series resonance frequency
- Q factor.

(Ans: f = 10 KHZ, R_D = 7.87KΩ)

Sol:

OSCILLATOR

1) What type feedback is employed in oscillators? What are the advantages? Discuss the conditions for sustained oscillations.

2) Define

- Damped oscillator
- Un dammed oscillations.

3) Classify different type of oscillators based on output waveforms, circuit components operating frequency and feedback used.

4) Classify different type of oscillators based on frequency range.

5) Give the two Barkhausen conditions required for sinusoidal oscillations to be sustained.

6) Prove that oscillations will not be sustained if, at the oscillator frequency the magnitude of the product of the transfer gain and feedback factor are less than unity.

7) State the condition of (1+A) which a feedback amplifier must satisfy in order to the stable.

8) Derive an expression for frequency of oscillation of Hartley oscillator using transistors.

9) Discuss and explain the basic of an LC oscillator and derive the conditions for the oscillations.

10) Derive the expression for frequency of oscillation in transistor colpitts oscillator.

11) What is piezoelectric effect? Explain the working crystal oscillator.

12) Draw the circuit diagram of a crystal oscillator. What are the advantages of a crystal oscillator over the other oscillators?

13) What is the range of frequency over which a crystal oscillator may be normally used and why?

14) What are the advantages and limitations of a crystal oscillator?

15) Explain the principle of operation of a Wien bridge oscillator with the help of a neat diagram obtain an expression for its frequency of oscillations.

16) What is the type of feedback incorporated in the Wien-bridge oscillator circuit? Explain its working.

17) Show that the gain of Wien bridge oscillator using BJT amplifier must be at least 3 for the oscillations to occur.

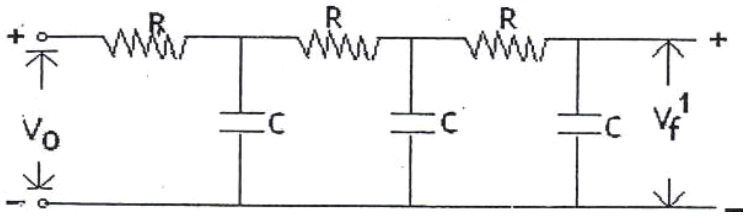
18) List the advantages of Wien bridge oscillator.

19) Explain how to stabilize the amplitude against variation, due to fluctuations occasioned in Wein bridge oscillator.

20) Draw the circuit diagram of a RC phase shift oscillator using BJT.

21) Derive the expression for frequency of oscillator RC – phase shift oscillator using BJT.

22) For the feedback network shown in fig. find the transfer function and the input impendence. If this network is used in a phase shift oscillator, find the frequency of oscillation and the minimum amplifier voltage gain. Assume that the network does not load down the amplifier.



23) Sketch the circuit of a phase shift oscillators using a BJT and explain its operation.

24) What are the factors that affect the frequency stability of an oscillator? How frequency stability can be improved in oscillators.

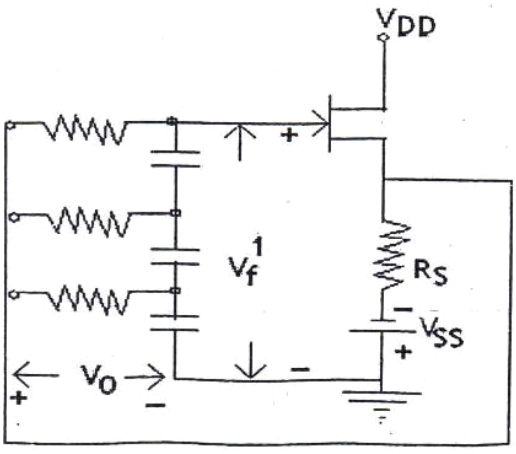
25) Explain briefly about frequency and amplified stability of oscillators.

26) Why the LC oscillator are not suitable for low frequency applications. Explain the principle of working of basic LC oscillators.

27) Derive the expression for frequency of oscillators. Why RC oscillators are not suitable for high frequency applications.

28) Why RC oscillators are not suitable for high frequency applications.

29) For the JFET oscillator shown in fig. find V_F/V_o, the frequency of oscillation and the minimum gain of the source follower required for oscillations.



30) Explain why in every practical oscillator the loop gain is slightly larger than unity?

31) Prove that amplitude of the oscillations is limited by the onset of Non-linearity.

32) State the NYQUIST CRITERION for stability.

UNIT-4:POWER AMPLIFIERS

1) Introduction to power amplifier

- A power amplifier is an amplifier, which is capable to providing a large amount of power to the load. Such as loud speaker or motor
- The power amplifier is used as a last stage in electronic system. A power amplifier is more commonly known as audio amplifier.
- The power amplifier does not actually amplify the power, it takes power the d.c power supply connected to the output circuit and converse it into useful a.c power. The power is fed to load.
- The small signal amplifier is called voltage amplifier and a large signal amplifier as a power amplifier.

2) Classification of power amplifiers

The quiescent point or operating point is fixed by selecting the d.c biasing conditions of transistors.

The position of the quiescent point on the load line decides the class of operation of the power amplifiers. The various classes of power amplifiers. Are

- CLASS A
- CLASS B
- CLASS C
- CLASS AB

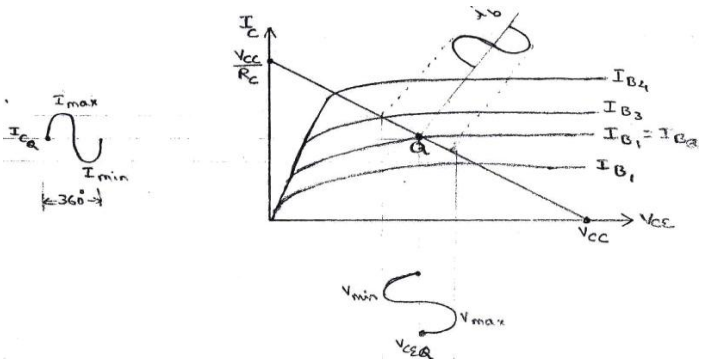
i) class A amplifier

a) the power amplifier is said to be class A amplifier if the Q point and the input signal are selected such that the output signal is obtained for a full input cycle.

b) For all values of input signal the transistor remain in the active region and never enters into cutoff saturation region.

c) From the fig. shown for full input cycle a full output is cycle is obtained. Here signal is faithfully reproduced, at the output without any distortion.

d) The efficiency of class A operation is very small.



i) class B amplifiers

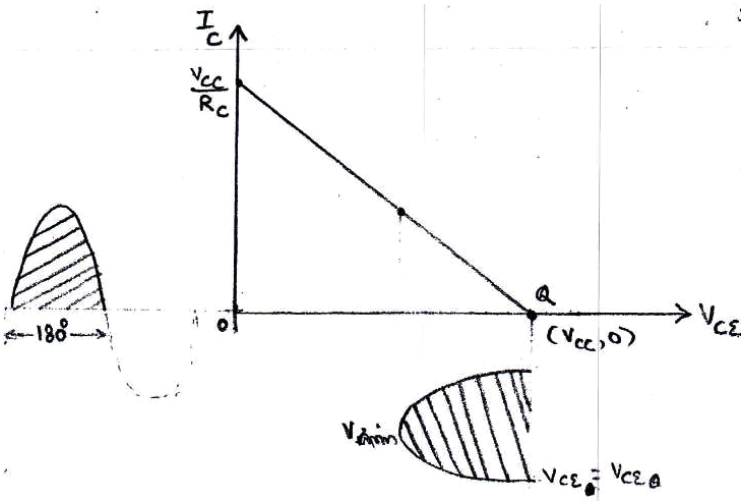
a) The power amplifier is said to be class B amplifier it the Q point and the input signal are selected, such that output signal is obtained only for one half cycle for a full input cycle. For this operation, the Q point is shifted on X-axis , transistor is biased to cutoff.

b) Due to the selection of 'Q' point on the X axis, the transistor remains in the active region only for positive half cycle is reproduced at the output. But in a negative half cycle of the input signal, the transistor enters in a cutoff region and no signal is produced at the output.

c) The collector current flows only for 180^0 (half cycle) of the input signal.

d) As only a half cycle is obtained at output for full input cycle, the output signal is distorted in this mode of operation.

e) The efficiency of class B operation is much higher than the class A operation.



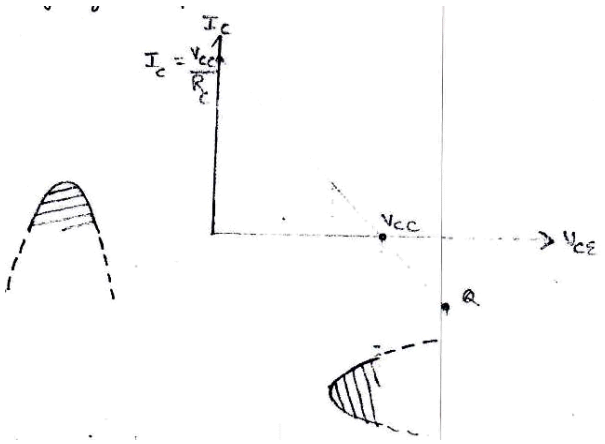
iii) Class 'C' amplifiers.

a) The power amplifier is said to be class C amplifier if the Q point and the input signal are selected such that the output signal is obtained for less than a half cycle, for a full input cycle. For this operation, the Q point is to be shifted below X –axis.

b) Due to selection of 'Q' point transistor remains active, for less than a half cycle. Hence only part of input appears at output.

c) In class C, the transistor is biased well beyond cutoff. As the collector current flows for less than 180^0 the output is much more distorted and hence 'C' is not used for A.F power amplifier.

d) The efficiency is very high compared to class A and class B and nearly 100%

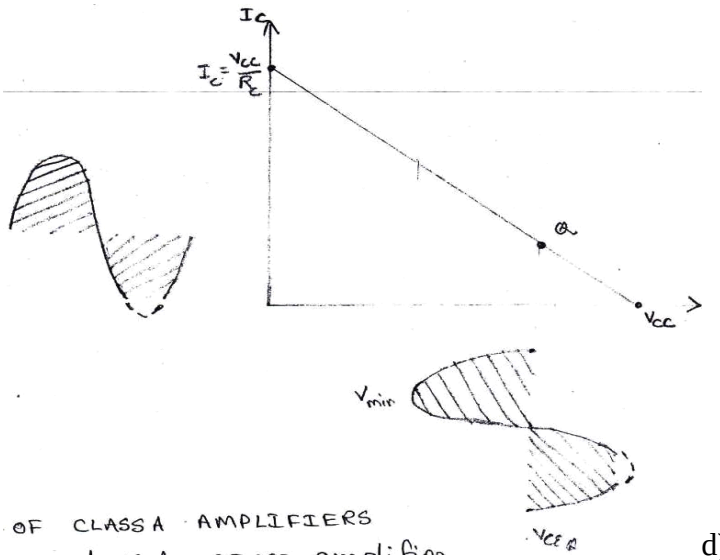


iv) Class AB amplifier

a) The power amplifier is said to be class AB amplifier it the Q point and the input signal are selected such that the output signal is obtained for more than 180^0 but less than 360^0 for a full input cycle.

b) The transistor remains active for more than one half cycle(180^0) and enters to cutoff region before (360^0) of completion of output signal. The Q point is slightly above X-axis and below the midpoint of load line.

c) The distortion exists in class AB also.



d) The efficiency is greater than A and less than class B. in class AB operation the cross over distortions is eliminated.

3) Analysis of class A amplifiers

Two types of class A power amplifier

- Directly coupled class A amplifier
- Transformer coupled class B amplifier.

1) Directly coupled class A amplifier

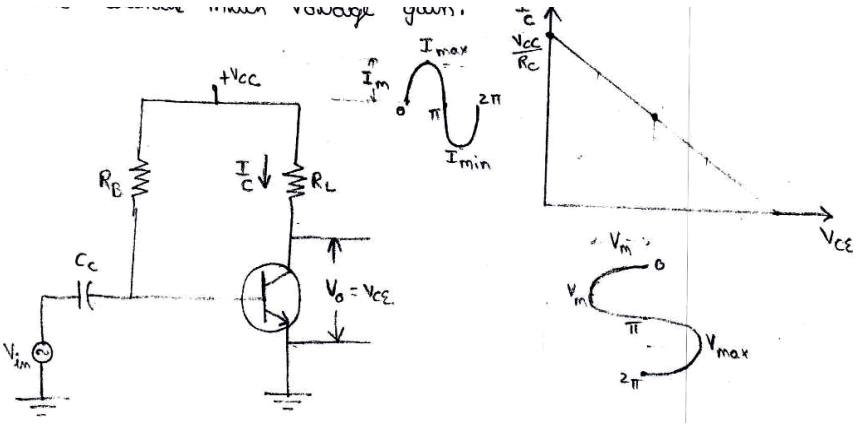
1) A simple fixed bias circuit can be used as a large signal class A amplifier as shown in figure (1).

2) The transistor used, is a power transistor. The value of R_B is selected such that Q point lie's at the centre of the d.c load line.

3) For all values of input signal the transistor remains in the active region and never enters into cutoff or saturation region. When an a.c input signal is applied the collector voltage varies sinusoid ally hence the collector current also varies sinusoid ally. The collector current flows for 360^0 (full cycle) of the input signal. The input and output wave forms are shown in fig 2.

4) The circuit represents the directly coupled class A amplifier as the load resistance is directly connected in the collector circuit. Generally value of R_L = 4 to 16 Ω and (B < 100) for transistor used.

5) The overall circuit handles large power in range few watts to 10 watts without much voltages gain.



6) D.C operation

The collector supply voltage V_{cc} and resistance R_B decides the d.c base = bias current I_{BQ}

The corresponding collector current is

The corresponding collector to emitter voltage

Hence the Q point (is determined

7) A.C operation

When an input a.c signal is applied the base current varies sinusoid ally. Assuming that the non linear distortion is absent the nature of the collector current and also vary sinusoid ally the varying output current and voltage deliver a.c power.

a.c power output

maximum instantaneous collector voltage

= minimum instantaneous collector voltage

= maximum instantaneous collector current

= minimum instantaneous collector current

= peak to peak value of a.c o/p current

→ Using r.m.s values $P_{a.c}$ =

Power delivered to load =

→ using peak to peak values $P_{a.c}$ =

Power delivered to load =

8) Efficiency

The ratio of output a.c power delivered to load to input d.c power gives the efficiency of amplifier.

→ Power dissipation

The power dissipation occurs in the form of heat

ii) Transformer coupled class A amplifier.

1) The basic circuit of transformer coupled amplifier is shown below.

2) The primary of transformer is connected to collector of the transistor the output is taken across load resistance connected to secondary of transformer.

3) As, the load is directly coupled to collector, power lass occurs due to d.c components, this disadvantage is eliminated by transformer coupled load.

4) Hence for a.c input signal given to base. Appears in amplified form at collector as primary of transformer is connected to it form at collector, as primary of transformer is connected to it, transfer's power to secondary of transformer and finally delivered to load resistance. (generally a load speaker)

5) D.C operation

There is no d.c voltage drop across the primary winding of the there no d.c bias voltage . Hence the d.c load line is a vertical straight line passing through a voltage point on the x-axis which is

→ D.C power input

6) A.C operation

For a.c analysis, a.c load line on the output characteristics must be obtained. The output current i.e collector current varies around its quiescent value when a.c input signal is applied to the amplifier. The corresponding output voltage also varies sinusoidally around its quiescent value which is in this case.

→ A.C output power: the a.c power developed is on the primary side of the transformer the a.c power delivered is on the secondary side of the transformer.

A.C power developed on the primary is

(pri) (pri)

load resistance interms of primer

A.C power delivered to load at secondary

→ The power delivered to secondary is some as power developed in primary (ideally) under practical conditions, it is slightly less than power in primary.

7) Efficiency:

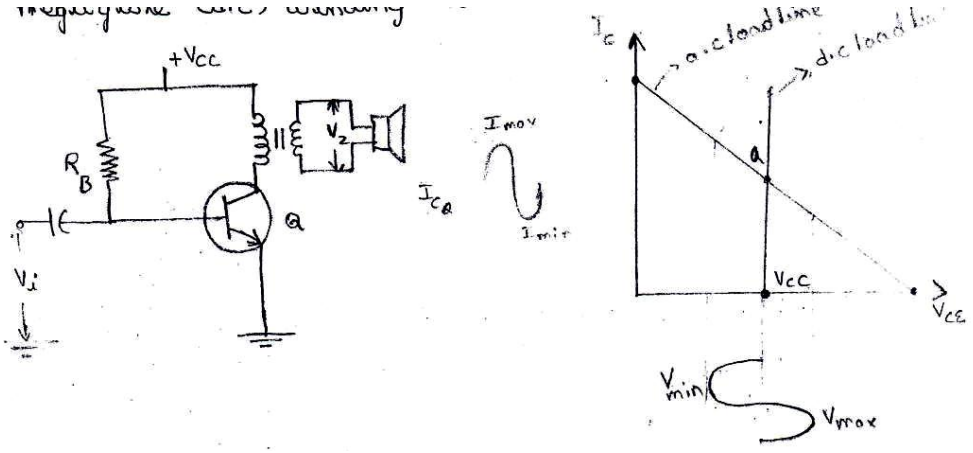
The efficiency is given by ratio of output a.c power to input d.c power

→ Maximum efficiency At maximum efficiency

Hence maximum efficiency is 50% ideally, but in practical conditions it is about 30 to 35%

8) Power dissipation

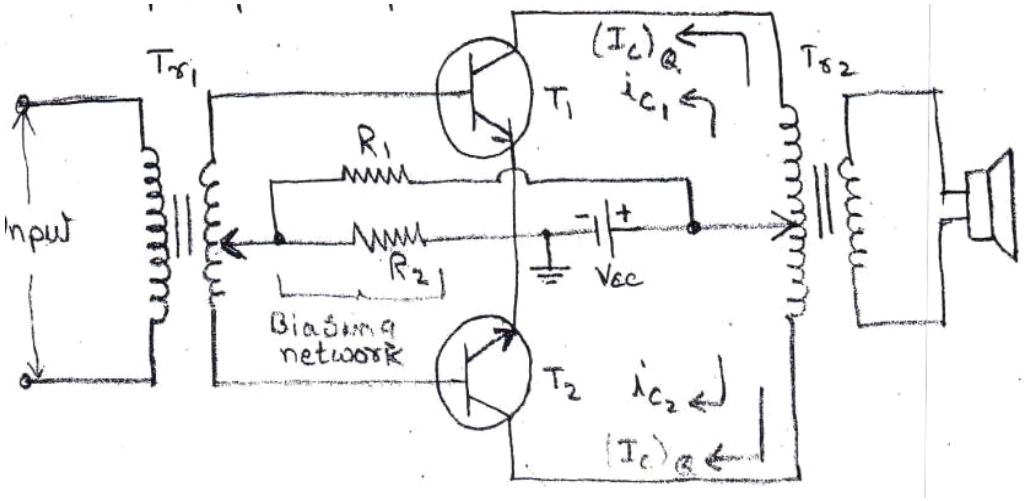
The power dissipated by the transformer is very small due to negligible (d.c) winding resistances and can be neglected.



Class A push pull power amplifier

The distortion introduced by non – linearity of the dynamical transfer characteristic using a single transistor as amplifier can be minimized by push-pull arrangement. The amplifier is then known as push pull amplifier

1) The class push pull amplifier is shown below.



2) In push pull arrangement two identical transistor T_1 and T_2 are used. The emitter terminals of the two transistors are connected together. The input signal is applied to the inputs of two transistors through centre tapped transformer, this transformer provides opposite polarity signals

to the two input transistor. The collectors of both the transistors are connected to the primary of output transformer.

The collector terminals of the two transistors are connected to the supply through the primary of output transformer. Resistors R_1 and R_2 provide the biasing. The load (loud speaker) is connected across the secondary of output transformer.

The transformer at output is chosen such that proper impendence matching is done such that maximum power is delivered.

3) Operation

a) The two transistors T_1 and T_2 carry d.c components of collector currents (. These currents are equal in magnitude and flow in opposite directions through the primary of transformer T_2. So there is practically no net d.c component of current through the primary of transformer T_2. This will increase the a.c power output which is obtained by a single transistor.

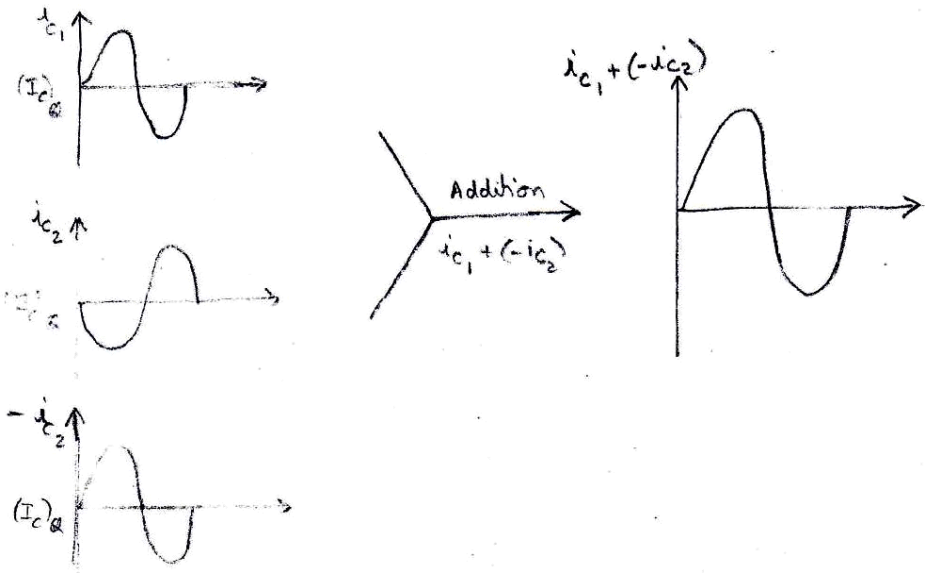
b) When an a.c signal is applied to the input. When the input signal voltage is positive, the base of transistor T_1 is more positive while of transistor T_1 increases. These currents flow in opposite direction in two halves of the primary of output transformer.

c) The flux produced by these currents will also be in opposite directions. As a result, the voltage across the load will be induced voltages whose magnitude will be proportional to the difference of collector currents i.e. (

d) For negative Half cycle, the collector current will be more than . In this case the voltage developed across the load will again be due to the difference (. As > the polarity of voltage induced across load will be reversed.

e) The overall operation results in an a.c voltage induced in secondary of output transformer and hence a.c power is delivered to the load. The difference of two collector currents is shown in fig.

f) If is obvious that during any given half cycle of input signal, one transistor is being driven (or pushed) deep into conduction while the other being non conduction (pushed out) hence the name push – pull amplifier.



Class B power Amplifier [push pull amplifier

- A class B pus pull amplifier is shown below
- The push pull circuit requires two transformers; one at the input circuit requires two transformers. One at ehe input called driver transformer and other at output called load. Both transformers are center tapped.
- Two transistors Q_1 and Q_2 are connected with emitter coupled as shown in circuit
- The drives transformer drives the input signal applied to primary and secondary is grounded at centre tap. The centre tap of primary of output transformer is connected to + $V_{CC.}$ The input signals applied to the base of the transistors Q_1 and Q_2 will be 180^0 out of phase.

- The transistor Q_1 conducts for th positive half cycle of the input producing positive half cycle at the load. While Q_2 conducts for the negative half cycle across the load. Thus, both the half cycles are obtained at the load i.e. full cycle is obtained.
- When point A is positive the transistor Q_1 gets driven into an active region whiles the transistor Q_2 is in cutoff region. While when point A is negative the point B is positive, hence the transistor Q_2 gets driven into the active region while the transistor Q_1 is in cut off region.
- The input and output wave forms are shown below

8. D.C operation

The d.c biasing point i.e Q point is adjusted on the x – axis such that and is zero. Hence Q point is (V_{CC} , O).

→ D.C power input: each transistor output is half rectified wave from

I_m = max. Value of output current by each transistor

d.c or average value is [half wave form]

Total d.c or average current drawn from supply is algebraic sum of the individual currents.

9. A.C operation

= max. value of current (o/p)

= max. value of o/p voltage

→ A.C power output

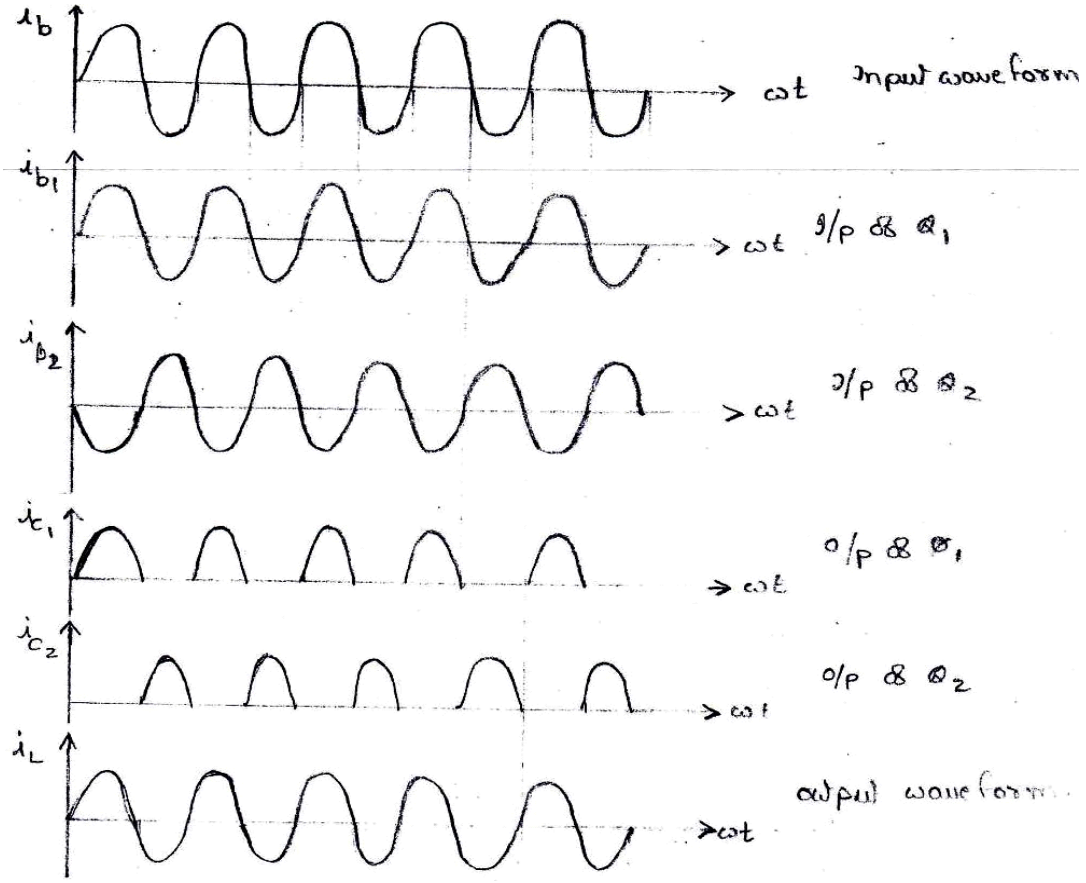
10) Efficiency

The efficiency is obtained by ratio of output power to input power

→ Maximum efficiency

Maximum efficiency occurs when $V_{mm} = V_{CC}$

= 78.5%


i_b
ωt
Input waveform
i_{b_1}
ωt
i_{b_2}
ωt
i_{C_1}
ωt
i_{C_2}
ωt
i_L
ωt

6) Complementary symmetry class B push pull amplifier

1) A Complementary symmetry class B push pull amplifier is shown below.

2) The circuit consists one npn an done $p_n p$, transistor instead of two npn transistors as in push pull amplifier. This circuit is transformer less circuit.

3) The matched pair of complementary transistors are used in common collector configuration. This is because C.C configuration has lowest output impedance and hence the impedance matching is possible.

4) The circuit is driven from a dual supply of V_{CC}. The transistor Q is npn while Q_2 is pnp type.

5) Operation:

a) In the positive half cycle of the input signal the transistor Q_1 gets driven into active region and starts conduction. The same signal is applied to the base of the Q_2 but as it is of complementary type it remains in off condition, during positive half cycle. Finally the output is taken at the load resistance $R_{L.}$

b) During negative half cycle of the signal the transistor Q_2 being PNP gets biased into conduction, while the transistor Q_1 gets driven into cutoff region. Hence only Q_2 conducts during negative half cycle of input, producing negative half cycle at the load R_L.

c) Thus for a complete cycle of input a complete cycle of output signal is developed across load R_L.

6) D.C power input

7) A.C power output

8) Efficiency

7) Distortion in amplifiers

1) The input signal applied to amplifiers is alternating in nature. The basic features of any alternating signal are amplitude, frequency and phase.

2) The amplifier output should be reproduced faith fully i.e there should be no no change or distortion in the amplitude, frequency and phase of the signal.

3) The possible distortions are in any amplifier are amplitude frequency distortion, phase distortion.

4) The amplification is faith full (i.e. distortion less) when the transistor is perfectly linear device i.e the dynamic characteristics of a transistor is a straight line over the operating rang [$i_c = Ki_b$]

5) Under practical conditions, dynamic characteristics is not perfectly linear. Due to such non linearity in the dynamic characteristics, the wave form of the output voltage differs from that of the input signal. Such a distortion is called as non linear distortion or amplitude distortion or hormone distortion.

a) Harmonic Distortion

1) The harmonic distortion means the presence of the frequency components in the output wave form, which are not present in the input signal.

2) Fundament frequency component

The component with frequency same as the input signal is called as fundamental frequency components.

3) The additional frequency components present in the output signal are having frequency components which are integral multiples of fundamental frequency component.

These components are called as harmonic components or harmonics.

Ex: Fundamental frequency FHz, harmonics are 2F,3F,4F……

Has the largest amplitude, with increase in order of harmonics amplitude decreases, so it is more important to study second harmonic distortion.

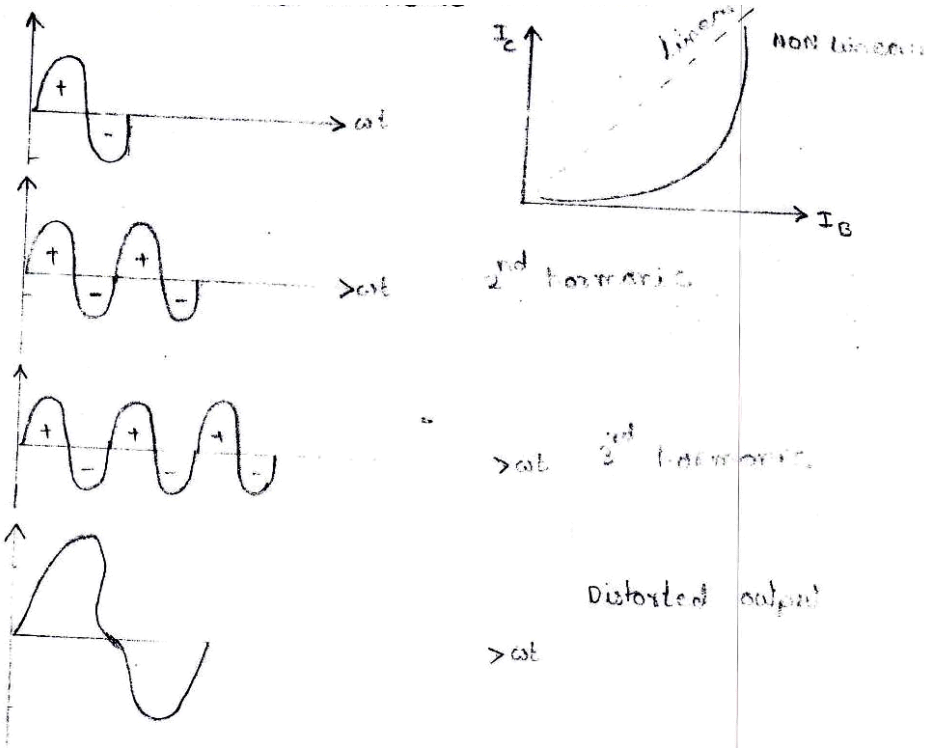
5)The percentage harmonic distortion due to each order (2^{nd} , 3^{rd} ….n^{th}) can be calculated by comparing the amplitude of each order of harmonic with the amplitude of the fundamental frequency component.

6) If the fundamental frequency component has an amplitude of B_1 and the n^{th} harmonic component has an amplitude of B_n then the % harmonic distortion due to n^{th} harmonic component is expressed as.

% n^{th} harmonic distortion

Total harmonic distortion is due to all the individual components

D = Total harmonic distortion.



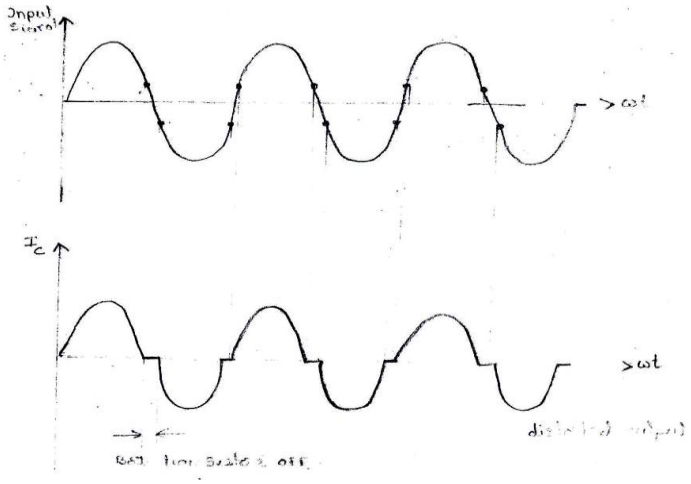
b) Cross over distortion

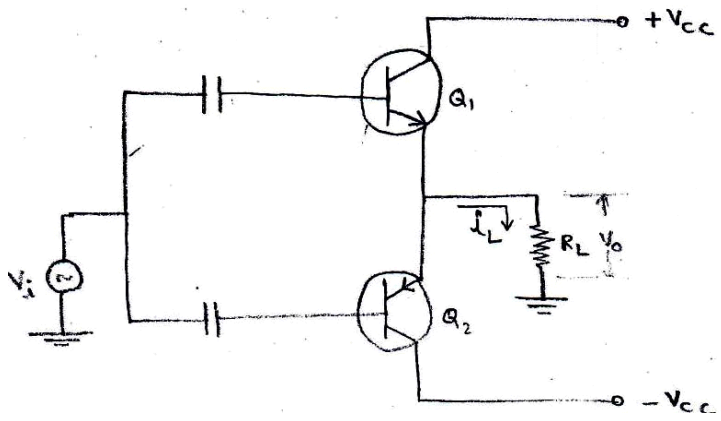
1) A transistor to be in active region the base emitter junction must be forward biased. The junction cannot be forward biased till the voltage applied becomes greater than cut in voltage (V_r) of the junction, which is generally 0.7 V for silicon and 0.2 V for germanium transistor.

2) Hence, as long as input signal is less than cut in voltage (V_r) of the base emitter junction, the collector current is zero and transistor remains in cutoff region.

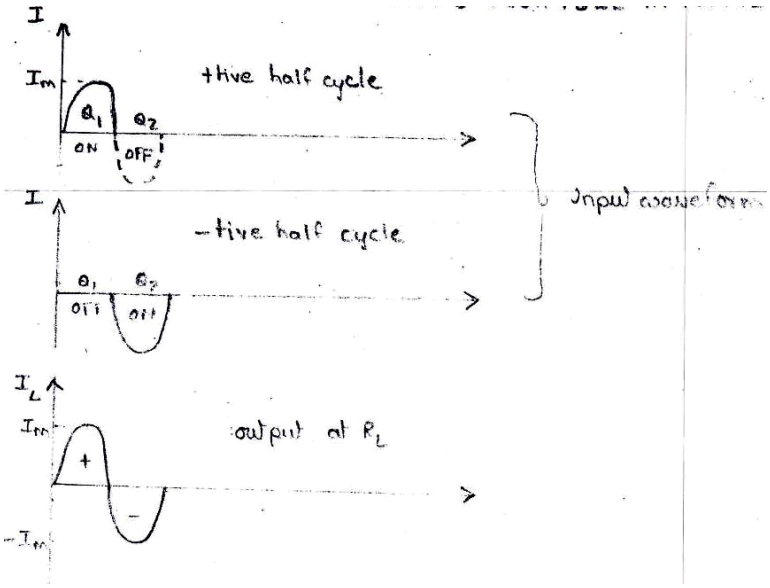
3) In class B amplifiers this cross over distortion is seen.

4) Hence there is a period between the crossing of the half cycles of the input signal, which none of the transistors is active and output is zero. Hence the nature of the output signal gets distorted and no longer remains same as that of input. This is called CROSS OVER DISTORION.





Complementary class B push pull amplifier



ASSIGNMENT – I

LARGE SIGNAL AMPLIFIER

1. Define power amplifier. How are power amplifiers classified?

2. Explain about class A series fed power amplifier? What is the efficiency?

3. Explain about transformer coupled class a power amplifier find its efficiency.

4. Compare series fed and transformer coupled class A amplifier.

5. Explain about class B push pull amplifier. Derive its efficiency.

6. With the help of a neat diagram explain the operation of a complementary symmetry configured class B power amplifier.

7. Compare and contrast push pull and complementary symmetry configurations for class B power amplifier.

8. Discuss in detail the origin and effect of cross – over distortion. How do you avoid the cross – over distortion in power amplifier circuit? Discus in detail

9. Discuss the origin of various distortions in transistor amplifier circuits.

10. Explain method of determinations of total harmonic distortion in push pull power amplifiers using 5 – point analysis.

11. What is thermal resistance? What is the unit of thermal resistance?

12. Explain the commonly available heat sinks.

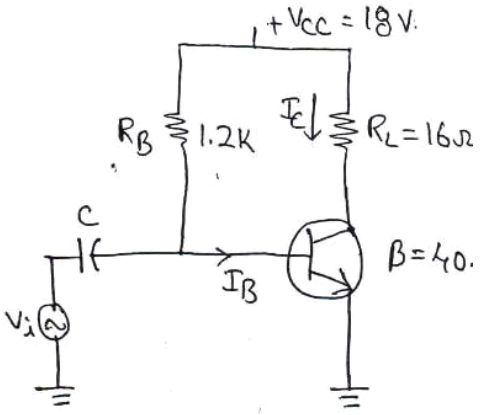
What is the necessary o f hear sinks for a power transistor?

ASSIGNMENT – 2

POWER AMPLIFIER

CLASS A

1) Calculate the input power output power and the efficiency of class A amplifier. Shown in fig. the input voltage causes a base current 5 mA r.m.s



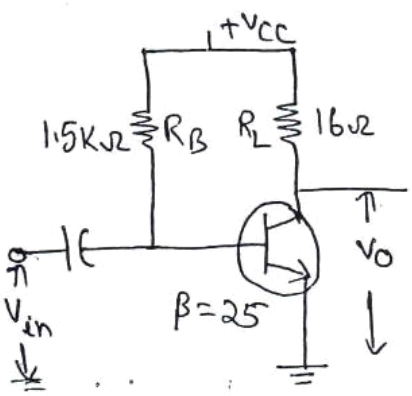
Ans: $P_{in} = P_{DC} = 10.38w$

$P_o = P_{a.c} = 640$ ml

2) A series fed class A amplifier uses a supply voltage of 20V. The a.c input voltage results in a bare current of 9 mA peak calculate.

1) Co – ordinates of the Q point, 2) D.C input power, 3) A.C output power

4) Efficiency, 5) Power dissipation, 6) maximum power dissipation.



Ans: 1) Q [14.85V, 321.67mA]

2) P_{dc} = 6.433w

3) $P_{a.c}$ = 404.95 mw

4) %

5) $P_d = P_{DC} - P_{ac}$

= 6.028w

6) Pd_{max} = 6.433w

CLASS B

3) A push pull class B A.F power amplifier uses the ideal transformer having a total of 160 turns on the primary an d40 turns on the secondary. It must be capable of delivering 40w power to the 8 Ω speaker, under maximum condition. How much should be the value of V_{CC}?

Ans: V_{CC} = 50.60V

4) For a class B amplifier using common collector configuration the supply voltage is 25V while the load resistance is 16Ω. If the input a.c signal of 20V peak is supplied, determine the input power, output power and the efficiency.

Ans: P_{dc} = 19.89w

$P_{a.c}$ = 12.5w

5) Calculate the efficiency of a complementary symmetry A.F power amplifier using Ideal emitter follower circuit and two d.c power supplies of +20V and -20V when driving an 8Ω load for a sinusoidal input voltage of i)V_{in} = 10 V(r.m.s) and ii) V_{in} = 5V(r.m.s) what value of V_{in} (r.m.s) yields maximum efficiency ?

Ans 2)

1)

DISTORTION

6) A single transistor amplifier with transformer coupled load produces harmonic amplitudes in the output as

B_o = 1.5 mA , B_1 = 120 mA , B_2 = 10 mA , B_3 = 4mA, B_4 = 2mA, B_5 = 1mA.

1) Determine the percentage total harmonic distortion

2) Assume a second identical transistor is used along will a suitable transformer provide push pull operation. Use the above harmonic amplitudes to determine the total harmonic distortion.

Ans : 1)% D = 9.1624%

2) % D = 3.4326%

7) A sinusoidal signal V_S= 1.75 sin (600t) is fed to a power amplifier the resulting output current is

I_0 = 15 sin 600t + 1.5 Sin 1200t + 1.2 Sin 1800t + 0.5 sin 2400t c

Calculate the percentage increase in the power due to distortion.

Ans: $P_{(a.c)D}$ = 0.0175

% $P_{increase}$ = 1.75 %

8) Prove that in class A amplifier if distortion is 10% power given to the load is increased by 1 %

Ans: -D = 10%

$P_{(a.c)D}$ = 1.01 P_{ac}

9) A Power amplifier supplies 3 w to a load of 6KΩ. the zero signl d.c collector current is 55 mA and the collector current with signal is 60mA. How much is the percentage second harmonic distortion?

Ans: % D_2 = 16.01%

10) A silicon power transistor is operated with a heat sin K with . The transistor is rated for 120 w at 25^0C and $Q_{jc} = 0.5^0$C/w. the mounting insulation has ^{0}C/w. what maximum power can be dissipated if the ambient temperature is 35^0C and $(T_j)_{max} = 200^0$C.

Ans: P_d = 68 .75 w

11) A silicon transistor has maximum allowable junction temperature of 175^0C. in ambient temperature of 25^0C , the transistor can dissipate 0.5w. if the transistor dissipates 0.3 w when an ambient temperature is changed to 35^0C. Find the junction temperature under this condition.

Ans: $T_j = 125^0$C

12) The operating junction temperature of a transistor is 125^0C. the total dissipation at a 25^0C case temperature is 0.5 w and at a 25^0C of ambient temperature, the total dissipation is 0.2 w. what is the value of thermal resistance

Ans:

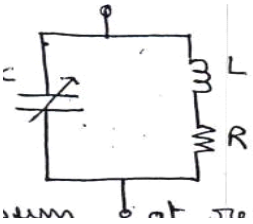
500^0C/w

300^0 C/w

UNIT--5

1) Tuned amplifiers

1) Tuned amplifier circuits are designed to amplify a signal over a narrow band of frequencies centered at fo. To achieve this, tuned amplifiers use a tuned or resonant circuit as load.



2) A tuned circuit is shown below, the amplifies employ a tuned parallel Lc circuit, ahich resonates at a resonant frequency.

f_r =

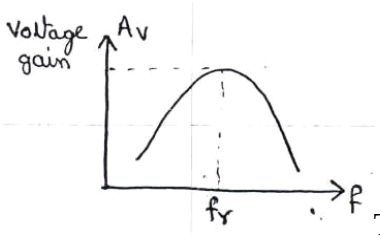
impedance z_r =

3) The response of tuned amplifier is maximum at resonant frequency and it falls sharply for frequencies below or above f_r.

4) Quality factor determines the 3dB bandwidth for the resonant circus the 3dB band width is given as B.w = , Q

2) Classification of tuned amplifiers.

For obtaining large gain, multi stage amplifiers are used.



They are classified as.

1) Single tuned amplifier

2) Double tuned amplifier

3) Stagger tuned amplifier.

These are further classified according to coupling used to cascade the stages of multi stage amplifier.

1) Capacitive coupled 2) inductive coupled 3) transformer coupled.

3) Single tuned amplifier

1) Single tuned multistage amplifier circuit uses one parallel tuned circuit as a load in each stage with tuned circuits in all stages. Tuned to the same frequency.

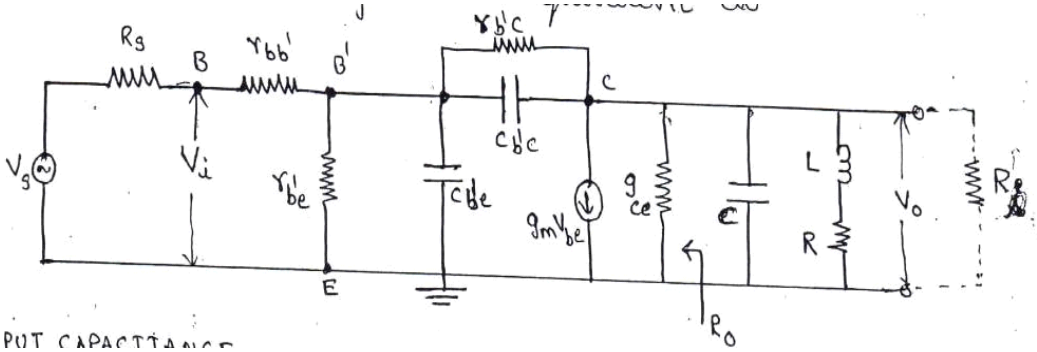
2) A single tuned amplifier (CE configuration) is shown below.

3) The tuned circuit by L and C acts as collector load and resonates at frequency of operation. The resistors R_1, R_2 and R_E along with capacitor C_E provides self bias for the circuit.

4) The equivalent circuit for single tuned amplifier using hybrid parameters.

R_i is input resistance of next stage and R_o is output resistance of current generator. g_m

The reactance of the bypass capacitor C_E and the coupling capacitors C_c are negligibly small at the operating frequency and hence these elements are neglected in equivalent ckt



Input capacitance

C_i = + (I –A), where A is the voltage gat of the amplifier

C_{eq} = (c – tuned circuit capacitance output capacitance

The output resistance of current general or g_m v_{be}

g_{ce} = = hoe - g_m h_{re} hoe =

5) Centre frequency

1) The centre frequency or resonant frequency is given as

, ceq = (+ C

$= C_0 + C$

2) Quality factor 'Q'

Effective quality factor Q =

\

=

3) Voltage gain (A_V)

A_V = = - g_m + – fractional

Variation in

Resonant freq.

A_V at resonance

g_m x R_t

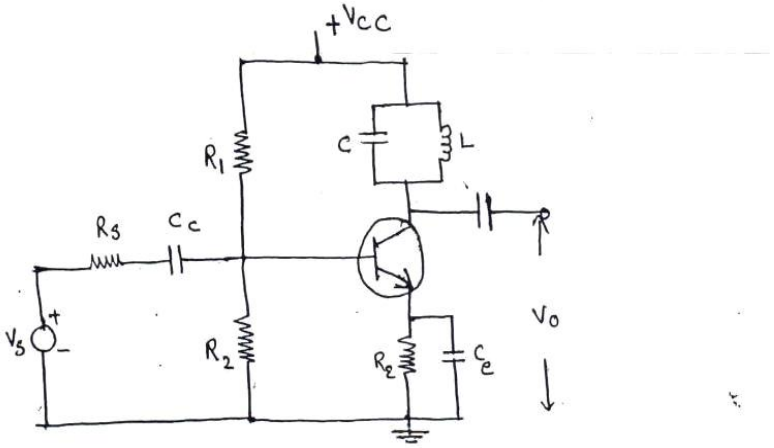
4) The 3xB band width is given as

f = =

The band width of n stage identical amplifier is given as

$(B.w)_n = f_2 – f_1 = B\ w_1$

Bw_1 is band width of single stage and Bwn is the bandwidth



Single tuned Capacitive Coupled transistor amplifier.

4) Double tuned amplifier

1) A double tuned amplifier in CE configuration is shown below.

2) The voltage developed actors tuned circuit is coupled inductively to another tuned circuit. Both tuned circuit are tuned to the semi frequency.

3) The coefficient of finical coupling is given as

K_c = Q_p = Quality factor for primary winding

Q_s = Quality factor for secondary winding

If K (coefficient of coupling)

1) K< Kc , circuit is linden coupled

2) K > Kc, circuit is over coupled

The frequently response is shown in figs for critical, under and over coupled circuits.

4) The bandwidth incase of double tuned amplifier over which the power amplification do not drop to less than one half, or – 3dB, of the power amplification al resonance, this makes voltage amplification dropping to 70.7% of if maximum value.

The 3dB bandwidth in a double tuned amplifier exceeds that un single tuned amplifier by factor

b = 1 for critical coupling

= , = 3d band width for double tuned

= 3dB bandwidth for single tuned.

6) Companied with a single tuned amplifier, the double tuned amplifier.

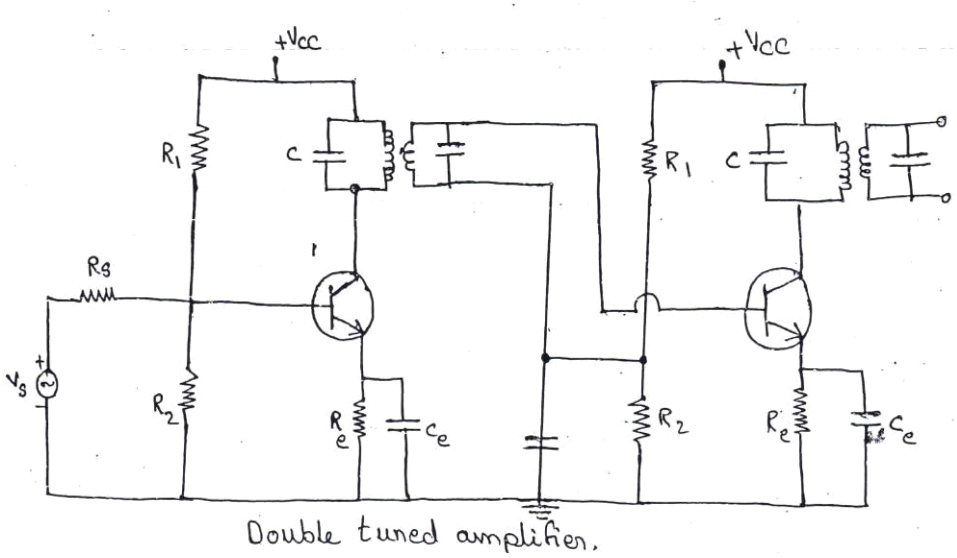
i) Posses a falter response lowing steeper sides

ii) Provides larger 2dB band width

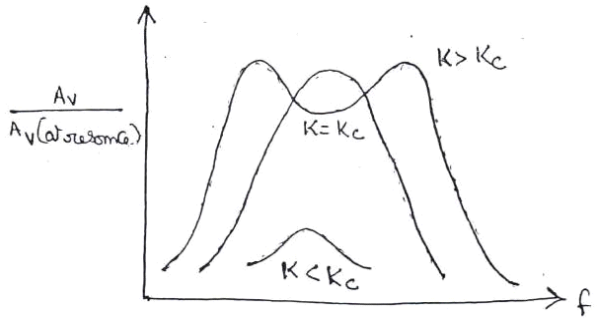
iii) Provides large gain bandwidth product

7) Efferent of cascading on band width for n stage. 3dB bandwidth = A_z (

= 2dB bandwidth for double tuned amplifier.



Double tuned amplifier.



5) Stagger tuned amplifier

1) The double tuned amplifier gives greater 2dB bandwidth loving stepper sides and flat top. But alignment of double tuned amplifier is difficult. To overcome this problem two single tuned cascaded amplifiers laving certain bandwidth are taken and their resonant frequencies are so adjusted that they are separated by an amount equal to bandwidth of each stage,

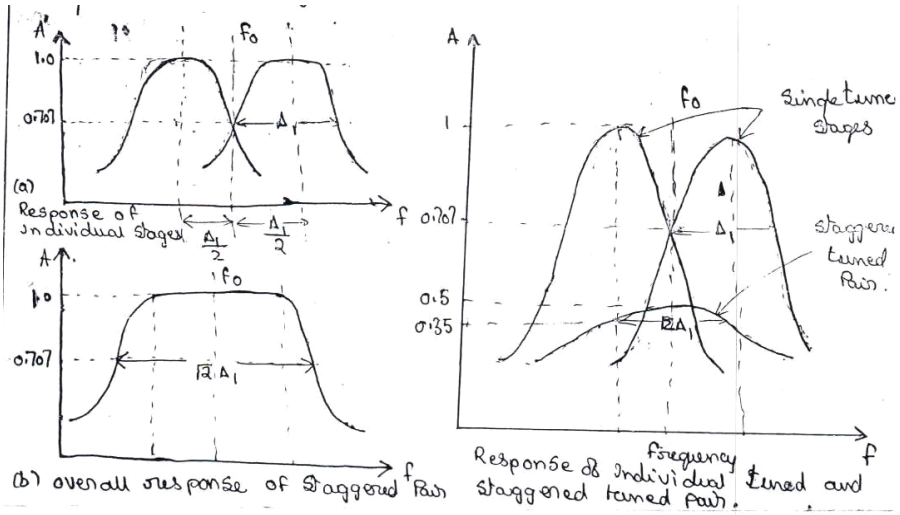
Since the resonant frequencies are displaced or staggered, they are known as stagger tuned amplifiers.

2) The advantage of staggered tuned amplifier is to have a better flat, wide band characteristics in contrast with a very sharp, rejective, narrow band char aclaisties of synchronous tuned circuits.

3) The overall response of the two stage stagger tuned pair is compared with individual stages in fig2.

4) The half power (3dB) band width of the staggered pair is times as great as the half power (3dB) band width of an individual single tuned slage.

5) The gain bandwidth product per stage of a stagger tuned pairs is 0,707. = 1 times that of individual single timed stages.

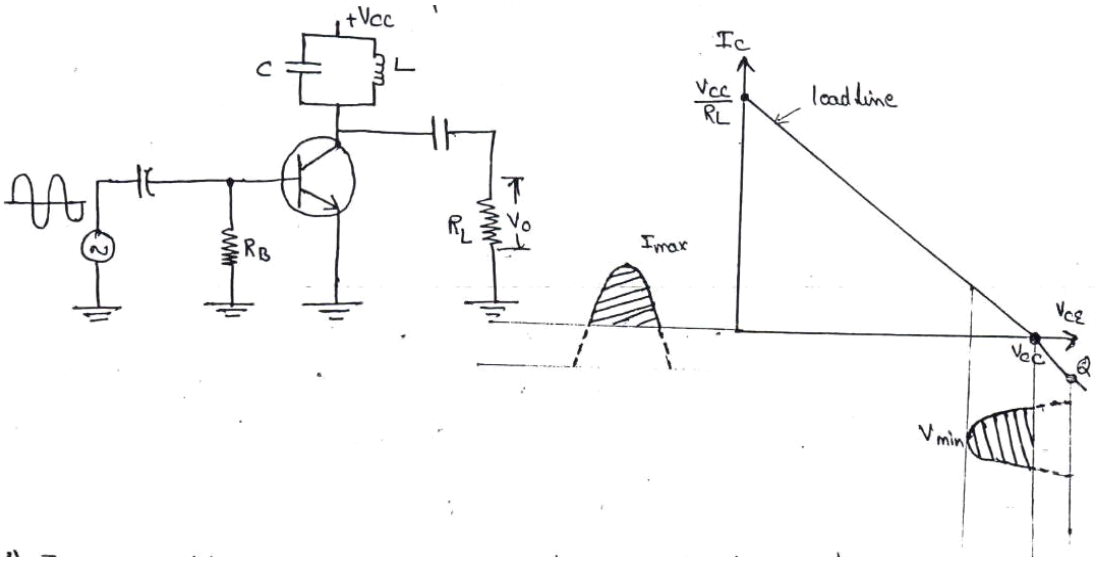


6) Class c tuned amplifier

1) The amplifier is said to be class c amplifier, if the Q point and the input signal are selector such that the output signal is obtained for less than a half cycle, for a full input cycle.

2) Due to such a selection of the Q point, transistor remains active, for less than a half cycle. Hence only that much part is reproduced at the output. For remaining cycle of the input cycle, the transistor remains cut off and no signal is produced at the output.

3) A class 'C' tuned amplifier is shown below



4) The parallel resonant circuit acts as a load impedance

5) As collector current flows for less than half a cycle, the collector current consists of a series of pulses with the harmonies of the input signal.

6) A parallel tuned circuit a eating as a load impedance is tuned to input frequency. Therefore, it filters the harmonic frequencies and prod ever a sine wave output vole age consorting of fundamental component of the input signal.

7) The output voltage is maximum at the resonant frequency the resonant frequency for parallel tuned circuit is given

F_r =

8) Rower gam G = =

9) Output power pout = = I^2oums R_L

= V_m =

10) Power dissipation

In class 'c' amplifier, the conduction angle is much less 180^0. The power dissipation of the transistor depends on the conduction angle. If increases when conduction angle increases.

The maximum power dissipation for class c amplifier can be given as

P_D max =

Under normal condition, conduction angle will be less than 180^0 and the transistor power dissipation will be less than.

But considering worst case condition, the transistor

Power rating must be greater than P_D max.

11) Efficiency

The efficiency of the amplifier is given as

100

100

The dc collector current depends on the conduction angle for a conduction angle of 180^0 ca half – wave signal), the average or dc collector current is (I_c) sat / for smaller conduction angle, the dc current is less than this.

In a class c amplifier, most of the dc input power is converted into ac load power because the transistor and ceil losses are small. When the conduction angle is 180^0, the efficiency is 78.5%. The efficiency increases when conduction angle decrease as said earlier class c amplifier has maximum efficiency of 100% approached at very small conduction angles.

12) Band width

The band width of resonant circuit is defined as B.w = $f_z - f_1$

The band width of class c tuned amplifier is given as B.w =

Where Q is the quality factor of the circuit.

Assignment -1 tuned amplifier.

1. What is a tuned amplifier and low do you classify tuned amplifier briefly explain.

2. Explain the significance of Q – factor.

3. Explain single tuned amplifier.

4. Briefly explain the capacitive coupled single tuned amplifier with its equivalent circuit.

5. With the help of a circuit diagram, explain tapped single tuned capacitance coupled amplifies.

6. Draw the circuit of double tuned amplifier [trams forms coupled]. Discuss the nature of responses of the amplifies for different values of kQ = 1, KQ > | and kQ < |.

7. Explain what do you mean by synchronous tuning of tuned amplifiers? Draw the frequency response of a synchronously tuned amplifies showing the response of individual stages and overall responses?

8. Explain about stagger funned amplifier draw the frequency response.

9. Compare stagger funned and synchronous funning

10. What is the effect of cascading in single funned amplifies.

11. What is the effect of cascading in double funned amplifies

12. Explain about class c tanned amplifier derive the efficiency.

1) A single tuned RF amplifier uses a transistor with an output resistance of 50k, output capacitance of 15PF. And input resistance of next stage is 20kΩ the tuned circuit consist of 47 inductance and 2Ω resistance calculate

i) Resonant frequency (ii) effective quality factor (iii) Band width of the circuit

Ans:- f_r = 20.2MHz

Q eff = 40. 5 2

B.w = 498.5kHz

2) A single tuned transistor amplifies is used to amplify modulated R.F carries of 600Hz and band width of 15Hz

The circuit has a total output resistance R_t = 20kΩ and output capacitance C_0 = 50PF. Calculate values of inductance and capacitance of the tuned circuit

Ans eff = 40, , c = 480.5PF

L = 132.6

3) An RF tuned voltage amplifier using FET with r_d = 100kΩ and g_m = 500us has tuned circuit, consisting of L = 2.4mH and c = 200 PF, as its load. At its resonant frequency the circuit offers an equivalent shun resistance of 100kg.

For the amplifier determine.

The resonant gain, Q eff 3) B.w

Ans :- Av = - 25,

Q eff = 14.147

B.w = 15. 904 kHZ

4) A tuned amplifies should have a gain of 50 for a centre frequency of 107. MHZ. and band width of 200KHZ .

A FET with gm = 5mt |v and r_d = 100k is to be used calculate the tank circuit parameters

Ans L = 3.288

C = 71.6PF

R = 3.98Ω

5) A simple tuned amplifier using FET has tank circuit components L = 100H, R = 5Ω, and c = 1000 PF. The FET used has r_d = 500kΩ, and g_m = 5m A/v. find

1) F_r 2) Tank circuit impedance at resonance 3) Voltage gain at resonance 4) Band width

Ans:- F_r = 503.29KHZ, R_p = 20k

A_v = B.w = 7.957KHZ

- 96,15

6) A tuned amplifier is required to have a voltage gain of 30 at 10.7MHZ with 200kHZ. B.w. ano FET with g_m = 5m A/v. and r_d = 100kΩ is available calculate of tank circuit eleventhS

C = 124.5PF R_p = 2.236Ω

L = 1.777

7. A three stage double tuned amplifies system is to have a half power B.w of 20KHZ centered on a centre frequency of 450 kHZ Assuming that all stages are identical, determine the half power band width of single stage. Assuming that each stage couple to get maximum fathers

$(B.w)_n$ = 28.01KHz

Where rage double tuned amplifies system is to have a half power B.w of 30 KHZ centered on a centre frequency of 400 kHZ. Assuming that all stages one identical determine the half power band width of single stage Assume that each stage couple to get maximum fatners

B.W = 42Khz

CLASS C

9) A class c tuned amplifier has inductance of 3H and capacitance of 470 PF. In the tank circuit calculates the resonal frequency.

$F_r = 4.238$ MHz.

10) for the circuit shown calculate resonant frequency a.c collector resistance quality factor and bandwidth $Q_L = 100$.

$F_r = 5.19$ MHZ

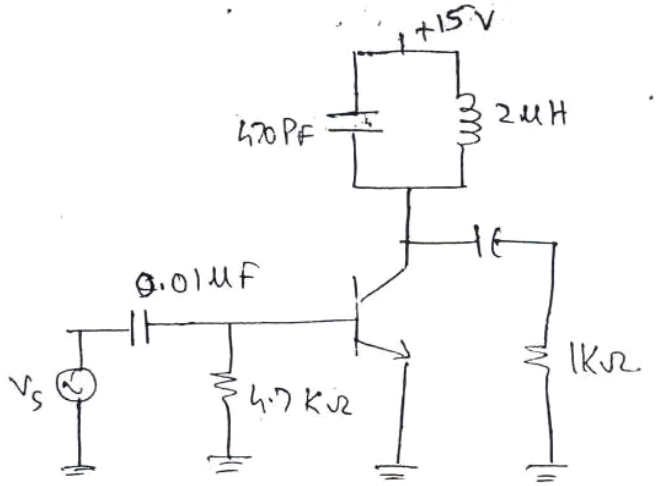
$R_C = 867\ \Omega$ Q= 13.29

B.W = 390.5 KHz

11) For the circuit show fig (1) what is the worst care power dissipation

Ans: $V_{pp} = 30V$

$P_{D\ max} = 26$ mw.



12. For circuit fig.1 calculate

1) P_6 when voltage output is 50 V_{pp}

2) $P_{ac(max)}$

3) $P_{id.c}$ if 0.4 mA and the output voltage is 30 V_{pp}

5) Band width of amplifier if Q = 125

6) Worst care transistor power dissipation.

Ans: P_{out} = 31.25 mw $P_{ac(max)}$ = 45 mw, P_{dc} = 15 mw

= 93.75% B.W = 85.84 KHZ, P_{Dmax} = 19.68mw.

3. If class c tuned amplifier has R_L = 6KΩ and required tank circuit Q = 80 calculate the values of L and C of the tank circuit. Assume V_{CC} = 20V, resonant frequency = 5MHz and worst care power dissipation = 20 mw.

Ans: P_{Dmax} = 2kΩ R_p = 3kΩ, L = 1.195 C = 851 PF)

4. Calculate the turns ration required to connect four parallel 16Ω speakers so that they appear as an 8kΩ effective load

Ans

Ratio 44.72 : 1