CONTENTS OF COURSE FILE

S.NO	TITLE	REMARKS
1	Vision & Mission statements of Institute / Department/PEOs	
2	Academic Calendar(JNTUH, College and Dept)	
3	Syllabus	
4	Text books & Reference books/ WEB/ Journals/ Topics Beyond the Syllabus/Gaps	
5	POs & PSOs	
6	Course Objectives, Course Outcomes, CO-PO Mapping	
7	Time Table	
8	Course schedule	
9	Course Plan	
10	Guest Lectures/Seminar / Field Visits	
11	Question bank (descriptive and objective)	
12	Previous question papers with at least one year External question paper solution/Answers	
13	Course material/Notes	
14	Tutorial Questions	
15	Assignment Questions (With Sample assignments of the Students)	
16	List of Weak students(As per previous semester Results, MID-I and MID-II Results)	
17	Schedule for Tutorial / Remedial / Special Classes	
18	Mid-I Question papers with key	
19	Mid –I Marks consolidation sheets with sample Answer scripts	
20	Mid-II Question papers with key	
21	Mid –II Marks consolidation sheets with sample Answer scripts	
22	CO attainment sheet	
23	Content Beyond the Syllabus and mapping with PO & PSO	
24	Course Review	
25	Course Completion Certificate	

ELECTRONIC DEVICES AND CIRCUITS



Department of Electronics and Communication Engineeri

Sreyas Institute of Engineering & Technology
Tattiannaram,
Hyderabad

2021-22

COURSE DESCRIPTION

Faculty Name	**Mrs. M PAVANI**
Designation	Assistant Professor
Department	ECE
Batch	2020-24
Academic Year	2021-22
Year & Semester	II-I
Section	A&B

Course title	**ELECTRONIC DEVICES AND CIRCUITS**			
Course code	EC301PC			
Regulation	R18			
Course Duration	16 weeks			
Course structure	Lectures	Tutorials	Practical	Credits
	4	1	0	4
Main Coordinator				
Team of instructors	Mrs. M. Pavani			

Prerequisites	Graduation Level	Credits	Periods/Week
1. Basic electronics	UG	4	4

Evaluation Scheme:				
S.No	Component		Duration	Marks
1	I - mid exam	Descriptive – answer any 2 of 4 – (10) Objective –answer all 20 Questions– (10)	80 Min	20
2	I - Assignment		-	05
3	II - Mid exam	Descriptive – answer any 2 of 4 – (10) Objective –answer all – (10)	80 Min	20
4	II - Assignment		-	5
5	External exam		3 Hours	75

Attainment Target for the academic semester:	CO1-T	CO2-T	CO3-T	CO4-T	CO5-T	CO6-T
	3	3	3	3	3	3

Institute Vision :

To be a centre of excellence in technical education to empower the young talent through quality education and innovative engineering for well being of the society.

Institute Mission :

1. Provide quality education with innovative methodology and Intellectual human capital.
2. Provide conducive environment for research and developmental activities.
3. Inculcate holistic approach towards nature, society and human ethics with lifelong learning attitude.

Department Vision :

To excel in Electronics & Communication Engineering education with the knowledge of innovation, research and ethics.

Department Mission:

1. To provide academic environment that promotes student centric learning through quality education and state of the art infrastructure.
2. To make the students aspire towards innovation and research to meet the technological needs of society.
3. To engage the students in activities which inculcate professional practices with social concern.

Programme Educational Objectives :

1. Graduate will be empowered with strong fundamental concepts, analytical capability, programming and problem solving skills.
2. Graduates will be employed, may pursue higher education or undertake research.
3. Graduates will embrace Professional Career Growth with Values & Ethics and urge for lifelong learning.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

ACADEMIC CALENDAR 2021-22

B. TECH./B.PHARM. II YEAR I & II SEMESTERS

I SEM

S. No	Description	Duration	
		From	To
1	Dussehra Recess	11.10.2021	16.10.2021 (1 Week)
2	Commencement of I Semester classwork	**18.10.2021**	
3	1st Spell of Instructions	18.10.2021	11.12.2021 (8 Weeks)
4	First Mid Term Examinations	13.12.2021	18.12.2021 (1 Week)
5	Submission of First Mid Term Exam Marks to the University on or before	24.12.2021	
6	2nd Spell of Instructions	20.12.2021	12.02.2022 (8 Weeks)
7	Second Mid Term Examinations	14.02.2022	19.02.2022 (1 Week)
8	Preparation Holidays and Practical Examinations	21.02.2022	26.02.2022 (1 Week)
9	Submission of Second Mid Term Exam Marks to the University on or before	26.02.2022	
10	End Semester Examinations	28.02.2022	12.03.2022 (2 Weeks)

II SEM

S. No	Description	Duration	
		From	To
1	Commencement of II Semester classwork	**14.03.2022**	
2	1st Spell of Instructions (including Summer Vacation)	14.03.2022	28.05.2022 (11Weeks)
3	Summer Vacation	09.05.2022	21.05.2022 (2 Weeks)
4	First Mid Term Examinations	30.05.2022	04.06.2022 (1 Week)
5	Submission of First Mid Term Exam Marks to the University on or before	11.06.2022	
6	2nd Spell of Instructions	06.06.2022	30.07.2022 (8 Weeks)
7	Second Mid Term Examinations	01.08.2022	06.08.2022 (1 Week)
8	Preparation Holidays and Practical Examinations	09.08.2022	16.08.2022 (1 Week)
9	Submission of Second Mid Term Exam Marks to the University on or before	16.08.2022	
10	End Semester Examinations	17.08.2022	30.08.2022 (2 Weeks)

REGISTRAR 11/10/21

EC301PC: ELECTRONIC DEVICES AND CIRCUITS

B.Tech. II Year I Sem.

L	T	P	C
3	1	0	4

UNIT-1

Diode and Applications: Diode - Static and Dynamic resistances, Equivalent circuit, Load line analysis, Diffusion and Transition Capacitances, Diode Applications: Switch-Switching times. Rectifier - Half Wave Rectifier, Full Wave Rectifier, Bridge Rectifier, Rectifiers with Capacitive andInductive Filters, Clippers-Clipping at two independent levels, Clamper-Clamping Circuit Theorem,Clamping Operation, Types of Clampers

UNIT-2

Bipolar Junction Transistor (BJT): Principle of Operation, Common Emitter, Common Base andCommon Collector Configurations, Transistor as a switch, switching times, Transistor Biasing andStabilization - Operating point, DC & AC load lines, Biasing - Fixed Bias, Self Bias, Bias Stability, BiasCompensation using Diodes.

UNIT-3

Junction Field Effect Transistor (FET): Construction, Principle of Operation, Pinch-Off Voltage, Volt-Ampere Characteristic, Comparison of BJT and FET, Biasing of FET, FET as Voltage Variable Resistor.

Special Purpose Devices: Zener Diode - Characteristics, Voltage Regulator. Principle of Operation -SCR, Tunnel diode, UJT, Varactor Diode.

UNIT-4

Analysis and Design of Small Signal Low Frequency BJT Amplifiers: Transistor Hybrid model, Determination of h-parameters from transistor characteristics, Typical values of h-parameters in CE, CB and CC configurations, Transistor amplifying action, Analysis of CE, CC, CB Amplifiers and CE Amplifier with emitter resistance, low frequency response of BJT Amplifiers, effect of coupling and bypass capacitors on CE Amplifier.

UNIT-5

FET Amplifiers: Small Signal Model, Analysis of JFET Amplifiers, Analysis of CS, CD, CG JFETAmplifiers. MOSFET Characteristics in Enhancement and Depletion mode, Basic Concepts of MOSAmplifiers.

S.No.	Text Books	Publication
1	Electronic Devices and Circuits Jacob Millman,	TMH, 4th Edition, 2001.
2	Electronic Devices and Circuits theory- Robert L. Boylestead, Louis Nashelsky	Pearson, 11th Edition,2009

S.No.	Ref Books	Publication
1	The Art of Electronics- Horowitz	Cambridge universitypress,3rd Edition
2	Electronic Devices and Circuits, David A. Bell	Oxford, 5th Edition,
3	Pulse, Digital and Switching Waveforms –J. Millman, H. Taub and Mothiki S. Prakash Rao	Anuradha Agencies, 2nd Edition, 2008

S.No.	Web Link
1	https://nptel.ac.in/courses/117/103/117103063/

S.No.	Journal

S.No.	Gaps in Curriculum
1	Introduction to PN Junction
2	Working of PN Junction diode
3	Fundamentals of semiconductors

S.No.	Topics Beyond Syllabus
1	
2	
3	

	Program Outcomes
PO 1	**Engineering Knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO 2	**Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO 3	**Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO 4	**Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO 5	**Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO 6	**The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO 7	**Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO 8	**Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO 9	**Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO 10	**Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions
PO 11	**Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO 12	**Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.
	Program specific outcomes
PSO1	Design, analyze and develop modules and systems for applications in advanced electronics and communication systems.
PSO2	Utilize modern tools for modeling and computational techniques in IC fabrication and RF technologies.

EC301PC	Course Objectives
A	To Gain the basic knowledge of basic electronic circuits by familiarizing students with basic principle operation of PN Junction Diode and its applications
B	To understand the principle of operation of Bipolar Junction Transistor and analyzing BJT under different modes of operation.
C	Understanding the principle of operation of Field Effect Transistor and its applications.
D	Introducing students to special purpose diodes such as Zener Diodes, Tunnel Diodes, UJT, SCR and Varactor diode, its characteristics and applications
E	Analyzing different models of BJT under small signal AC analysis as well understanding Transistor amplifying action
F	Analyzing small signal model of FET under different configuration and introduction of MOSFET characteristics and types along with a brief introduction to MOS Capacitor

EC301PC	Course Outcomes
1	Able to understand the fundamentals of electronic circuits such as diodes and its applications
2	Able to understand BJT and also the applications of BJT
3	Able to understand types of FET as well as principle of operations along with its characteristics curve
4	Able to understand applications of special purpose diodes along with its characteristics curve
5	Able to analyze BJT under different modes such as CB,CE and CC configurations and derive its parameters.
6	Able to analyze FET under different modes such as CS,CD,CG configurations and understand types of MOSFET's as well as MOS Capacitor.

COURSE OBJECTIVES						COs	PROGRAM OUTCOMES (POs)												PSOs	
A	B	C	D	E	F		1	2	3	4	5	6	7	8	9	10	11	12	I	II
3						CO1	2	1	1	1	0	0	0	1	1	0	0	0	1	1
	3					CO2	2	1	1	1	1	0	0	1	1	0	0	1	1	1
		3				CO3	2	1	1	1	1	0	0	1	1	0	0	1	1	1
			3			CO4	2	0	1	2	1	0	0	1	1	0	0	1	1	1
				3		CO5	2	3	2	1	1	0	0	1	1	0	0	1	1	1
					3	CO6	2	3	2	1	1	0	0	1	0	0	0	1	1	1

SEC-A	1	2	3	4	Break	5	6	7
MON			EDC					
TUE	EDC							
WED				EDC				
THU		EDC						
FRI		EDC						
SAT				EDC(T)				

SEC-B	1	2	3	4	Break	5	6	7
MON	EDC							
TUE				EDC				
WED			EDC					
THU				EDC(T)				
FRI				EDC				
SAT	EDC							

COURSE SCHEDULE

S.No	Unit No	Description	From	To	Total No. Periods
1	I	Diodes and its Applications	20|10|21	24|11|21	28
2	II	Bipolar Junction Transistor (BJT)	25|11|21	15|12|21	17
3	III	Junction Field Effect Transistor(FET)	16|12|21	5|1|21	14
4	IV	Analysis and Design of Small Signal Low Frequency BJT Amplifiers	7|1|21	27|1|21	10
5	V	FET Amplifiers	28|1|21	5|2|22	10

Unit	Topic(s) to be covered	Text Book/ Reference Book	Mode of Teaching	Planned Date	Actual Date of completion
UNIT 1: DIODE AND ITS APPLICATIONS	Introduction to the subject	JACOB MILLMAN & SALIVAHANA	OFFLINE	20-10-21	20/10/21
	Qualitative Theory of P-N Junction			21-10-21	21/10/21
	P-N Junction as a Diode			22-10-21	22/10/21
	Diode Equation			23-10-21	23/10/21
	Volt- Ampere Characteristics			26-10-21	26/10/21
	Ideal versus Practical – Resistance levels (Static and Dynamic)			27-10-21	27/10/21
	Transition and Diffusion Capacitances			28-10-21	28/10/21
	Diode Equivalent Circuits			29-10-21	29/10/21
	Load Line Analysis			30-10-21	2/11/21
	Diode switching times			02-11-21	3/11/21
	The P-N junction as a Rectifier, Half wave Rectifier			03-11-21	5/11/21
	Full wave Rectifier,			[illegible]	6/11/21
	Bridge Rectifier,			06-11-21	9/11/21
	Harmonic components in a Rectifier Circuit			09-11-21	10/11/21
	Inductor Filters			10-11-21	11/11/21
	Capacitor Filters			11-11-21	12/11/21
	Introduction to clippers			12-11-21	13/11/21
	Clipping at two independent levels			13-11-21	16/11/21
	Introduction to clampers			16-11-21	17/11/21
	Clamping operation & clamping circuit theorem			17-11-21	18/11/21
	Types of clampers			18-11-21	20/11/21
	Problems			19-11-21	23/11/21
	Problems			20-11-21	24/11/21

UNIT 2 : BIPOLAR JUNCTION TRANSISTOR(BJT)	Principle of operation	JACOB MILLMAN & SALIVAHANA	OFFLINE	23-11-21	25|11|21
	Transistor Current Components			24-11-21	26|11|21
	Transistor as an Amplifier			25-11-21	27|11|21
	Transistor Construction			26-11-21	30|11|21
	BJT Operation, BJT Symbol			27-11-21	1|12|21
	Common Base Configuration			30-11-21	2|12|21
	Common Emitter and Common Collector Configurations			01-12-21	3|12|21
	Transistor as switch			02-12-21	4|12|21
	Transistor biasing and stabilization			03-12-21	7|12|21
	Comparison of CB, CE, and CC Amplifier Configurations			04-12-21	8|12|21
	Need for Biasing, Fixed Bias			07-12-21	9|12|21
	Self bias			08-12-21	10|12|21
	Bias Stability, Stabilization Factors			09-12-21	11|12|21
	Thermal Runaway, Thermal Stability			10-12-21	14|12|21
	Problems			11-12-21	15|12|21
UNIT 3 : JUNCTION FIELD EFFECT TRANSISTOR(FET)	The Junction Field Effect Transistor: Construction	JACOB MILLMAN & SALIVAHANA	OFFLINE	21-12-21	16|12|21
	The Junction Field Effect Transistor: Principle of operation, symbol			22-12-21	17|12|21
	Pinch-off Voltage - Volt-Ampere characteristics			23-12-21	18|12|21
	Comparison of BJT and FET			24-12-21	21|12|21
	FET as voltage variable resistor			28-12-21	22|12|21
	Special purpose diodes: Zener diode and characteristics			29-12-21	24|12|21
	Zener diode as voltage regulator			30-12-21	28|12|21
	SCR			31-12-21	29|12|21
	Tunnel diode			04-01-22	30|12|21
	UJT			05-01-22	31|12|21
	Varactor diode			06-01-22	4|1|22
	Problems			07-01-22	5|1|22

UNIT 4 : ANALYSIS & DESIGN OF SMALL SIGNAL LOW FREQUENCY BJT AMPLIFIERS	Transistor hybrid model	JACOB MILLMAN &SALIVAHANA	OFFLINE	08-01-22	7/1/22
	Determination of h-parameters from transistor characteristics			11-01-22	18/1/22
	Typical values of h- parameters in CE,CB and CC configurations			12-01-22	19/1/22
	Transistor amplifying action			18-01-22	20/1/22
	Analysis of CE,CC and CB amplifiers and CE amplifier with emitter resistance			19-01-22	21/1/22
	Low frequency of BJT amplifiers			20-01-22	22/1/22
	Effect of coupling and bypass capacitors on CE amplifiers			21-01-22	25/1/22
	Problems			22-01-22	27/1/22
UNIT 5 : FET AMPLIFIERS	The JFET Small Signal Model	JACOB MILLMAN & SALIVAHANA	OFFLINE	25-01-22	28/1/22
	FET Amplifiers: FET Common Source Amplifier			27-01-22	29/1/22
	Common Drain Amplifier			28-01-22	31/1/22
	Common Gate Amplifier			29-01-22	1/2/22
	JFET Amplifiers			01-02-22	1/2/22
	MOSFET -- Construction			02-02-22	2/2/22
	MOSFET -- principle of operation, symbol			03-02-22	3/2/22
	Characteristics in Depletion mode			04-02-22	4/2/22
	Problems			05-02-22	5/2/22
REVISION	UNIT 1			08-02-22	8/2/22
	UNIT 2			09-02-22	9/2/22
	UNIT 3			10-02-22	10/2/22
	UNIT 4			11-02-22	11/2/22
	UNIT 5			12-02-22	12/2/22

12/2/22

Head of the Department
Electronics & Communication Engineering
Sreyas Institute of Engineering and Technology
Beside Indu Aranya, Nagole, Hyderabad-500068.

Guest Lectures

Date	Resource person	Organization	Topic	No. of Students Attended

Seminars

Date	Resource person	Organization	Topic	No. of Students Attended

Industry /Field Visits

Date	Organization / field	Place of visit	Coordinator	No. of Students Attended

QUESTION BANK (DESCRIPTIVE AND OBJECTIVE)

UNIT-1:

Short answers:

1. What is PN Junction?
2. Define Static and Dynamic Resistance
3. Define Transition and diffusion capacitances
4. What is doping.
5. Differentiate the types of semiconductors.

Long Answers:

1. Explain the switching times of diode.
2. Explain the forward biasing of a PN junction diode
3. Draw and explain the V-I characteristics of a PN junction diode.
4. State the diode current equation and explain the meaning of each term in it.
5. With a neat circuit diagram explain the working of full wave rectifier.

Multiple Choice Questions:

1. If the positive terminal of the battery is connected to the anode of the diode, then it is known as:

a.Forward biased b. Reverse biased c. Equilibrium d. Unbiased

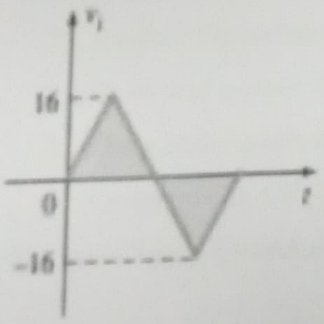
2.What is the SI unit of conductivity?

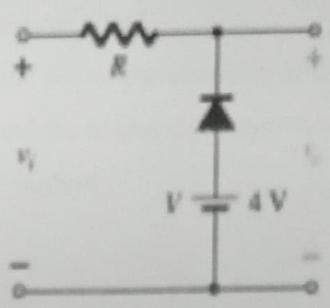
a. (Ωm)-1 b. Ωm c. Ω d. m

3. The cut-in voltage for silicon diode is approximately

a. 0.2 V b. 0.7 V c.1.1V d.1.4V

4. For the given input waveform to the given circuit, what is the peak value of the output waveform?





a. 16 V b.0V c.12V d.10V

5. Which of the following is not a necessary component in a clamper circuit?

a. Diodeb. Capacitorc. Resistord. Independent DC Supply

6.The change in collector emitter voltage from 6V to 9V causes increase in collector current from 6 mA to 6.3 mA. Determine the dynamic output resistance.

a. 10kΩ b.20kΩ c.50kΩ d.6 0kΩ

Fill in the Blanks:

1.For a germanium diode the cut-in voltage is V

2. The output of a half wave or full wave rectifier is .....

3. The maximum efficiency of full wave rectification is .....

4. The basic purpose of filter is to.....

5. A clamping circuit is also called as a .....

UNIT-2:

Short answers:

1. What is a transistor. Classify its types.
2. Why BJT is called as a bipolar junction transistor.
3. Why BJT is called as a current controlled device.
4. Sketch the symbols of NPN and PNP transistor.
5. State the operating regions of BJT.

Long Answers:

1. Explain the working principle of a NPN transistor
2. Explain the current components of a BJT.
3. Draw and explain the input and the output characteristics of a CB configuration.
4. Draw and explain the input and the output characteristics of a CE configuration.
5. Compare CB, CE, CC Configuration.

Multiple Choice Questions:

1.Which of the following is not a part of a BJT?

a. Base b. Collector c. Emitter d.None of the mentioned

2.The number of PN junctions in a BJT is/are:

a. 1 b. 2 c. 3 d. 4

3. In which of the following modes can a BJT be used as an amplifier?

a. Active b. Cut-off c. Saturation d. All of the mentioned

4.If a BJT is to be used as a switch, it must operate in:

a. Active b. Cut-off c. Saturation d. Both b and c.

Fill in the Blanks:

1. In Zener diode, the Zener breakdown takes place when the reverse breakdown voltage (Vz) is V

2. Zener breakdown can occur in .....

3. In breakdown region Zener diode behaves as a .....

4. In BJT ..... region is lightly doped and ..... region is heavily doped.

5. For a transistor to function as an amplifier the EB junction is ..... and CB junction is .....

UNIT-3:

Short answers:

1.What is FET. Classify its types.

2. List the important features of a FET.

3. Why BJT is called as a voltage-controlled device.

4. Why the input impedance of FET is higher than BJT.

5. Draw the symbol of N-Channel FET.

Long Answers:

1. Explain with neat sketch the construction and working of a N-Channel FET.
2. Explain the drain characteristics of a FET.
3. Explain the transfer characteristics of a P-Channel FET.
4. Compare BJT and FET.
5. List the applications of FET.

Multiple Choice Questions:

1. A FET _____

a. Is a voltage controlled device
b. Is a current controlled device
c. Has a low input resistance
d. Has a very large voltage gain

2 The gate controls _____

a. The width of the channel
b. The drain currents
c. The proportional pinch off voltage
d. All the above

3. The pinch off voltage has the same magnitude as the _____.

a. Gate voltage
b. Drain-source voltage
c. Gate-source voltage
d. Gate-source cutoff voltage

4. Transconductance is measured in _____ .

a. A/V
b. A
c. $Ohms^{-1}$
d. watts

5. Which internally connected region is heavily doped with an impurity by forming double PN junctions in JFET.

a. Source
b. Drain
c. Gate
d. Channel

6.In a degenerate semiconductor,the majority carriers are controlled by _____

a.Femi-Dirac statistics

b.Maxwell-Boltzmann statistics

c.Bose-Einstein statistics

d.Pauli's exclusion principle

7. In _____ configurations there is phase shift of 0 degree between input and output.

a. CE
b. CB

c. CC
d. CB or CC

8. In _____ configurations there is phase shift of 180 degree between input and output.

a. CE
b. CB
c. CC
d. CB or CC

9. The _____ amplifier can be used as voltage buffer.

a. CB
b. CE
c. CC
d. CB or CE

10. A emitter follower has a voltage gain of _____.

a. 0
b. 1
c. 0.5
d. 0.75

Fill in the Blanks:

1. For a JET, the value of Vds at which Id becomes essentially constant is the _____.
2. The value of Vgs that makes Id approximately zero is the _____ .
3. Transconductance is measured in _____ .
4. Determine the value of transconductance for n-channel JFET with Idss = 9 mA, Vp= -2V, Vgs= -1V_____.
5. JFET biasing at DC Level can be undertaken by _____.

UNIT-4:

Short answers:

1. Define hybrid parameters.
2. List the h-parameters of a CB, CC, CE configuration.
3. Write a short note on the mid-band gain of the amplifier.
4. Explain the use of coupling capacitors in a CE amplifier.
5. State the benefits of h-parameters.

Long Answers:

1. Explain the use of bypass capacitors in detail.
2. Explain the need of C_1, C_2 and C_E in detail.
3. Draw and explain the operation of a CE transistor circuit in detail.
4. Draw the h-parameter equivalent circuit of a CB, CC and CE transistor.
5. Give the typical values of h-parameters for CB, CC and CE configurations. Also give conversion formula between them.

Multiple Choice Questions:

1. The ideal voltage amplifier must have _____ input resistance.

   a. Low
   b. High
   c. Infinite
   d. zero

2. The ideal value of Ro is _____.

   a. Zero
   b. Infinity
   c. Very low
   d. High

3. Ideally the bandwidth of an amplifier should be _____.

   a. Infinity
   b. Low
   c. As high as possible
   d. Zero

4. The frequency of Vo of an amplifier is _____.

   a. Less than that of Vin
   b. Same as that of Vin
   c. Greater than that of Vin
   d. Twice that of Vin

5. Ideally voltage gain of an amplifier should be _____.

   a. Zero
   b. High
   c. Infinity
   d. Low

6.The _____ amplifier can be used as buffer.

a. CB
b. CE
c. CC
d. CB or CE

7. In _____ configurations there is phase shift of 180 degree between input and output.

a. CE
b. CB
c. CC
d. CB or CC

8. The phase difference between the input and output voltage in a common base arrangement is _____.

a. 90
b. 180
c. 0
d. None of the above

Fill in the Blanks:

1. The transistor acts as an amplifier in the _____ region.

2. In _____ configuration there is phase shift of 180 between input and output.

3. The output voltage of an amplifier is 5 V when an input voltage is 50 mV.Its voltage gain is _____.

4. The current gain of _____ amplifier is always less than unity.

5. The voltage gain of _____ amplifier is always less than unity.

6. A common emitter transistor amplifier has a current gain of 50.If the load resistance is 4 k ohms and input resistance is 500 ohms, the voltage gain in amplifier is _____.

7. A common emitter amplifier is designed with npn transistor with a= 0.99. the input impedance is 1 kilo ohms and load is 10 kilo ohms.The voltage gain will be _____.

UNIT-5:

Short answers:

1. List the important parameters of a JFET.
2. What is the input resistance of a JFET.
3. What is DC drain resistance.
4. What is AC /dynamic resistance.
5. What is JFET forward transconductance.

QUESTION BANK (DESCRIPTIVE AND OBJECTIVE)

Long Answers:

1. Draw and explain the JFET low frequency ac equivalent circuit.
2. Draw and explain the CS amplifier circuit and derive the expressions for Zi, Zo and Av.
3. Draw and explain the common source amplifier circuit with self-bias (un-bypassed Rs) and derive the expressions for Zi, Zo and Av.
4. Draw and explain the common drain amplifier circuit and derive the expressions for Zi, Zo and Av.
5. Draw and explain the common gate amplifier circuit and derive the expressions for Zi, Zo and Av.

Multiple Choice Questions:

1.The approximate AC equivalent circuit of a JFET contains _____.

a. A current source in series with a resistance
b. A current source between drain and source terminals
c. A current source between gate and source terminals
d. A resistance between drain and source terminals

2. Which kind of small signal JFET parameter is also a well-known form of 'dynamic drain resistance' across the drain and source terminals especially when the operation of JFET is in pinch off region.

a. AC drain resistance
b. DC drain resistance
c. Ohmic resistance
d. Transconductance

3. Determine the value of transconductance for N-channel JFET with I_{DSS} = 9mA, V_p = -2V, V_{gs} = -1V.

a. 7.5 mS
b. 6.5 mS
c. 4.5 mS
d. 5.5 mS

. The value of current source in AC equivalent circuit dependent on the _____.

a. Transconductance and gate-to-source voltage
b. DC supply voltage
c. External drain resistance
d. Answers (b) and (c)

If the source bypass capacitor is removed in the CS amplifier, _____.

a. The voltage gain will increase
b. The transconductance will increase
c. The voltage gain will decrease

6. If the external load resistance in CS amplifier is removed, the output voltage will _____.

a. Remains constant
b. Decrease
c. Increase
d. Be zero

7. The voltage gain of CD JFET amplifier is always _____.

a. Equal to 1
b. Less than 1
c. Greater than 1
d. Not equal to 1

8. Choose the correct statement.

a. MOSFET is an uncontrolled device
b. MOSFET is a voltage-controlled device
c. MOSFET is a current controlled device
d. MOSFET is a temperature-controlled device

9. In MOSFET devices the N-channel type is better the P-channel type in the following respects

a. It has better noise immunity
b. It is faster
c. It is TTL compatible
d. It has better drive capability

Fill in the Blanks:

1. In a common source amplifier, V_{ds}= 4.2 V_{rms} and V_{gs} = 140mv rms. The voltage gain is _____.

2. In a CS amplifier, R_D = 2.2 K, Rs = 330 ohms, V_{dd} = 10 V, and gm = 4500 micro second. If the source resistor is completely bypassed, the voltage gain is _____.

3. A CD amplifier with Rs = 1.2 K ohms has a gm of 6000 micro seconds. The voltage gain is _____.

4. A CS amplifier has a voltage gain of _____.

5. A source follower has a voltage gain of _____.

6.Which is the most significant current generating parameter in common drain JFET amplifier _____.

6. If the external load resistance in CS amplifier is removed, the output voltage will _____.

a. Remains constant
b. Decrease
c. Increase
d. Be zero

7. The voltage gain of CD JFET amplifier is always _____.

a. Equal to 1
b. Less than 1
c. Greater than 1
d. Not equal to 1

8. Choose the correct statement.

a. MOSFET is an uncontrolled device
b. MOSFET is a voltage-controlled device
c. MOSFET is a current controlled device
d. MOSFET is a temperature-controlled device

9. In MOSFET devices the N-channel type is better the P-channel type in the following respects

a. It has better noise immunity
b. It is faster
c. It is TTL compatible
d. It has better drive capability

Fill in the Blanks:

1. In a common source amplifier, V_{ds}= 4.2 V_{rms} and V_{gs} = 140mv rms. The voltage gain is _____.

2. In a CS amplifier, R_D = 2.2 K, Rs = 330 ohms, V_{dd} = 10 V, and gm = 4500 micro second. If the source resistor is completely bypassed, the voltage gain is _____.

3. A CD amplifier with Rs = 1.2 K ohms has a gm of 6000 micro seconds. The voltage gain is _____.

4. A CS amplifier has a voltage gain of _____.

5. A source follower has a voltage gain of _____.

6.Which is the most significant current generating parameter in common drain JFET amplifier _____.

Code No: 153AT

R18

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, October - 2020
ELECTRONIC DEVICES AND CIRCUITS
(Common to ECE, EIE, MCT)

Time: 2 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
- - -

1.a) Explain the operation of Full Wave Rectifier with necessary graphs.
b) Derive the expression for transition capacitance of a diode. [8+7]

2.a) Derive the expression for Ripple factor for Full Wave Rectifier with L-section filter.
b) Explain the working of p-n diode in forward and reverse bias conditions. [8+7]

3.a) Derive the operating point using AC and DC load lines.
b) Explain about Punch through and Base width modulation. [8+7]

4.a) Draw and explain the CE characteristics of a transistor.
b) The reverse leakage current of the transistor when in CB configuration is 0.3μA while it is 16μA when the same transistor is connected in CE configuration. Determine α, β and γ. [9+6]

5.a) With the help of neat diagram explain the voltage divider biasing method for FET.
b) Explain the construction and emitter characteristics of UJT. [8+7]

6.a) Why we call FET as a Voltage Controlled Device.
b) Draw the circuit diagram of SCR and explain its operation along with its characteristics. [7+8]

7.a) Draw and Explain BJT small signal model, compare the performance of CE, CB, CC amplifier.
b) Given I_E= 2.5mA, h_{fe}= 140, h_{oe}= 20μs and h_{ob}= 0.5μs. Determine the common-emitter hybrid equivalent circuit. [8+7]

8.a) Explain the working of MOSFET amplifier and discuss the gain and frequency response characteristics?
b) An n-channel JFET has I_{DSS} =10mA and V_P = - 2V. Determine the drain source resistance r_{ds} for (i) V_{GS} =0V. (ii) V_{GS} = - 0.5V. [8+7]

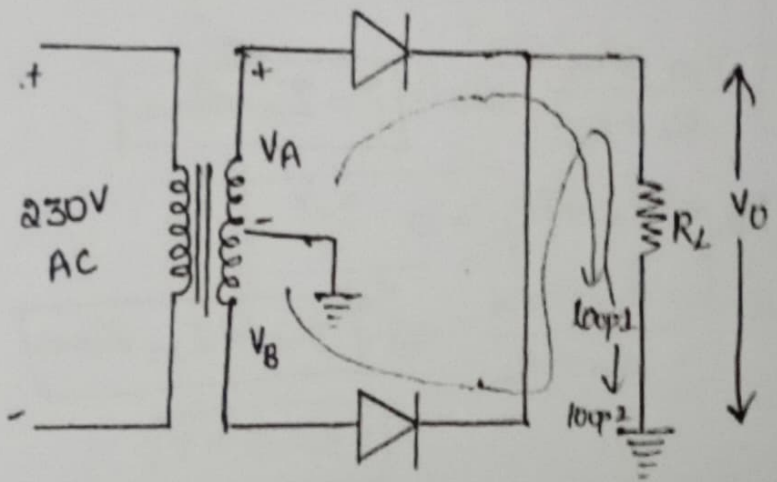
---ooOoo---

JNTUH USED NO-11-2020 AN

1a) Explain the operation of Full Wave Rectifier with necessary graphs.

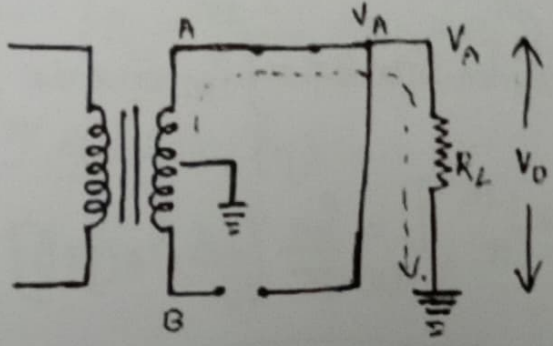
Full wave Rectifier

In this method we use 2 diodes i.e, full wave rectifier is the combination of two half wave rectifiers



case-1: $0 < \alpha < \pi$

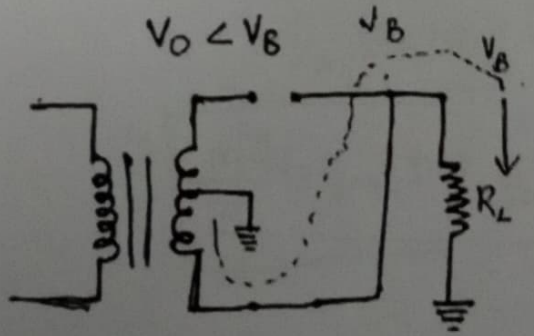
D_1 - ON D_2 - OFF

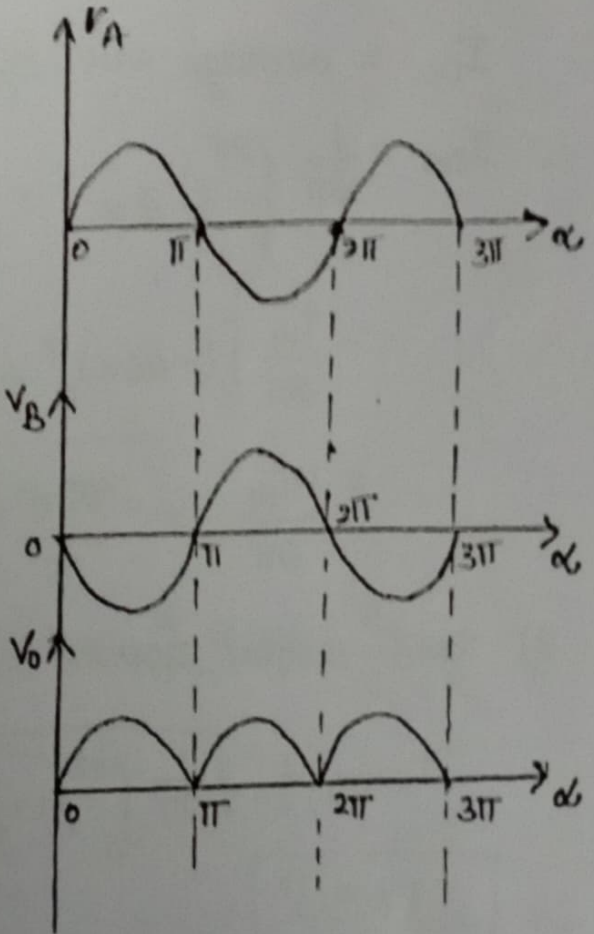


$V_o = V_A$

case-2: $\pi < \alpha < 2\pi$

$V_o < V_B$





Analysis

1) Instantneous output current (or) load current (i)

$i = i_m \sin\alpha$, $0 < \alpha < \pi$

$= -i_m \sin\alpha$, $\pi < \alpha < 2\pi$

for $0 < \alpha < \pi$, $-V_A + iR_F + iR_L = 0$

$$i = \frac{V_A}{R_F + R_L} = \frac{V_m \sin\alpha}{R_F + R_L} \Rightarrow \boxed{i = I_m \sin\alpha}$$

for $\pi < \alpha < 2\pi$, $-V_B + iR_F + iR_L = 0$

$$i = \frac{V_B}{R_F + R_L} = \frac{-V_m \sin\alpha}{R_F + R_L} \Rightarrow \boxed{i = -I_m \sin\alpha}$$

2) DC output current (I_{DC})

I_{DC} = average value of instantneous current (i)

$$I_{DC} = \frac{1}{2\pi}\int_0^{2\pi} i \cdot d\alpha = \frac{1}{2\pi}\left[\int_0^{\pi} i_m \sin\alpha \, d\alpha - \int_{\pi}^{2\pi} i_m \sin\alpha \, d\alpha\right]$$

$$= \frac{i_m}{2\pi}\left[(-\cos\alpha)_0^{\pi} + (\cos\alpha)_{\pi}^{2\pi}\right] = \frac{i_m}{2\pi}\left[(1+1)+(1+1)\right]$$

$$= \frac{4i_m}{2\pi} = \frac{2i_m}{\pi}$$

$$\boxed{I_{DC} = \frac{2I_m}{\pi}}$$

3) RMS output current (I_{RMS})

$$I_{RMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i^2 \cdot d\alpha} \Rightarrow \boxed{I_{RMS} = \frac{I_m}{\sqrt{2}}}$$

4) RMS value of AC component (I'_{RMS})

$$I'_{RMS} = \sqrt{I_{RMS}^2 - I_{DC}^2}$$

5) Ripple factor (γ)

$$\gamma = \frac{I'_{RMS}}{I_{DC}} = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - 1} = \sqrt{\frac{(I_m/\sqrt{2})^2}{(2I_m/\pi)^2} - 1}$$

$$= \sqrt{\frac{\frac{I_m^2}{2}}{\frac{4I_m^2}{\pi^2}} - 1} = \sqrt{\frac{\pi^2}{8} - 1} = 0.483$$

$$\gamma = 0.483$$

6) Input power (P_i)

$$P_i = I_{rms}^2 (R_F + R_L)$$

7) Efficiency (η)

$$\eta = \frac{P_{DC}}{P_i} \times 100 = \frac{I_{DC}^2 \cdot R_L}{I_{RMS}^2 (R_F + R_L)}$$

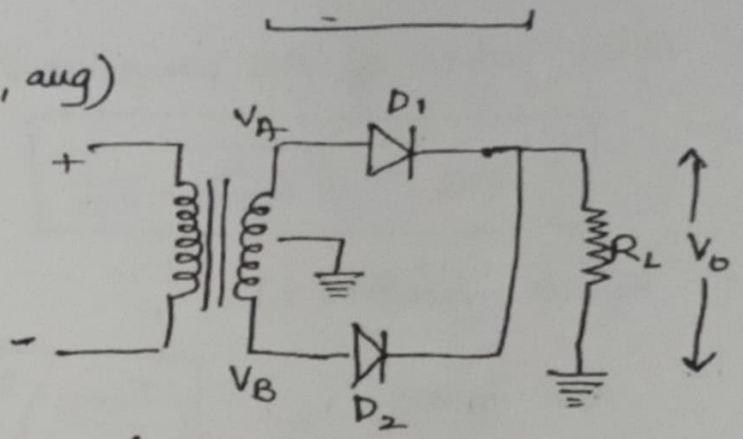
$$\eta = \frac{\frac{4I_m^2}{\pi^2} \cdot R_L}{\frac{I_m^2}{2}(R_F + R_L)} \times 100 = \frac{8}{\pi^2} \times 100 \cdot \frac{R_L}{R_F + R_L}$$

$$\eta = 81 \frac{R_L}{R_F + R_L}$$

$R_F \approx 0$

$$\eta = 81\%$$

8) Average diode Voltage ($V_{d,avg}$)



For $0 < \alpha < \pi$

$V_{diode} = 0$

for $\pi < \alpha < 2\pi$ $\quad V_A - V_B$

$= V_m \sin\alpha - (-V_m \sin\alpha)$

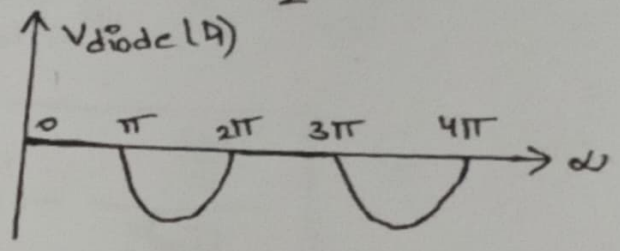
$= 2V_m \sin\alpha$

$D_1 \rightarrow V_{diode} = 0 \Rightarrow 0 < \alpha < \pi$

$2V_m \sin\alpha, \Rightarrow \pi < \alpha < 2\pi$

$D_2 \rightarrow V_{diode} = -2V_m \sin\alpha \quad 0 < \alpha < \pi$

$= 0 \quad \pi < \alpha < 2\pi$



$$V_{d,avg} = \frac{1}{2\pi}\int_0^{2\pi} V_{diode} \cdot d\alpha$$

$$\boxed{V_{d,avg} = -\frac{2V_m}{\pi}}$$

9) Peak Inverse voltage (PIV)

$$PIV = |V_{diode}| = |2V_m \sin\alpha|_{max} = 2V_m$$

$$\boxed{PIV = 2V_m}$$

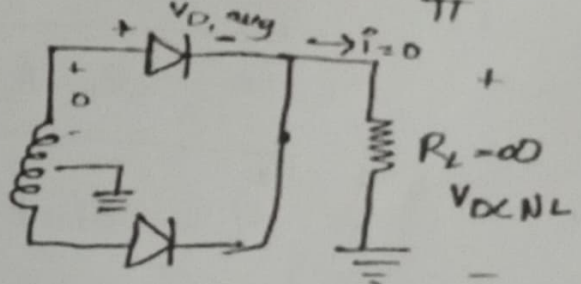
10) No load DC O/P voltage (V_{DCNL}):

$V_{DCNL} = V_{DC} \,|\, i = 0$ or $R_L = \infty$

$0 + V_{D,avg} + V_{DCNL} = 0$

$$V_{DCNL} = -V_{D,avg} = \frac{2V_m}{\pi}$$

$$\boxed{V_{DCNL} = \frac{2V_m}{\pi}}$$



11) Full load DC O/P voltage (V_{DCFL})

$V_{DCFL} = V_{DC} \,|\, i \neq 0.$

$V_{DCFL} = V_{DC} \mid i \neq 0.$

$$\boxed{V_{DCFL} = I_{DC} \cdot R_L}$$

$$\boxed{V_{DCFL} = \frac{2V_m}{\pi} - I_{DC} \cdot R} \qquad R = R_F + \frac{R_S}{2}$$

12) Regulation factor:

$$\text{reg } \% = \frac{V_{DCNL} - V_{DCFL}}{V_{DCFL}} \times 100$$

$$\boxed{\%\ \text{regulation} = \frac{R}{R_L} \times 100\ \%} \qquad R = R_F + \frac{P_{SW}}{Q}$$

13) Form factor (F):

$$F = \frac{I_{RMS}}{I_{DC}} = \frac{I_m/\sqrt{2}}{2I_m/\pi} = \frac{\pi}{2\sqrt{2}} = 1.11$$

$$\boxed{F = 1.11}$$

Bridge Rectifier

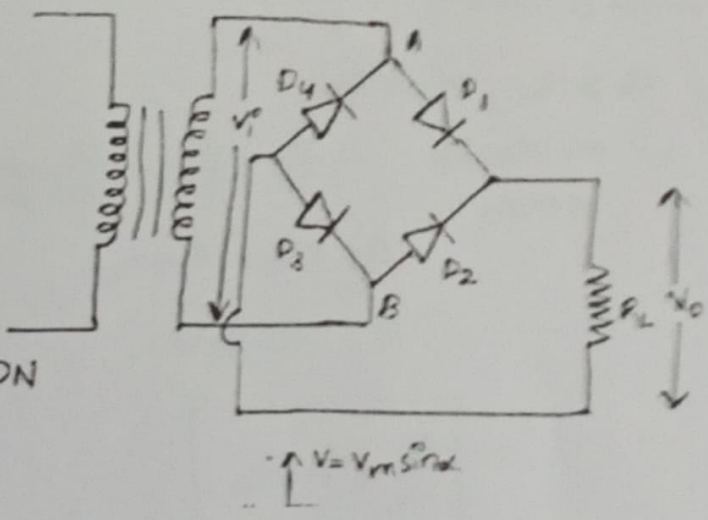
$V_i = V_m \sin\alpha$

for $0 < \alpha < \pi$

V_i is +ve, D_1, D_3 - F.B, ON

D_2, D_4 = R.B

$V_o = V_i$



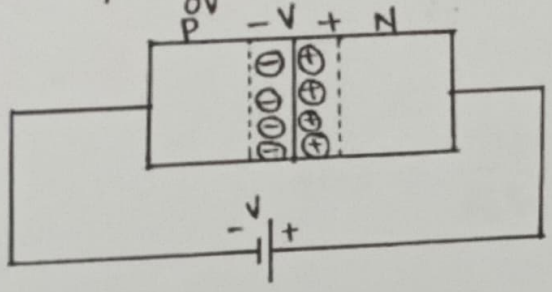
1b) Derive the expression for transition capacitance of a diode.

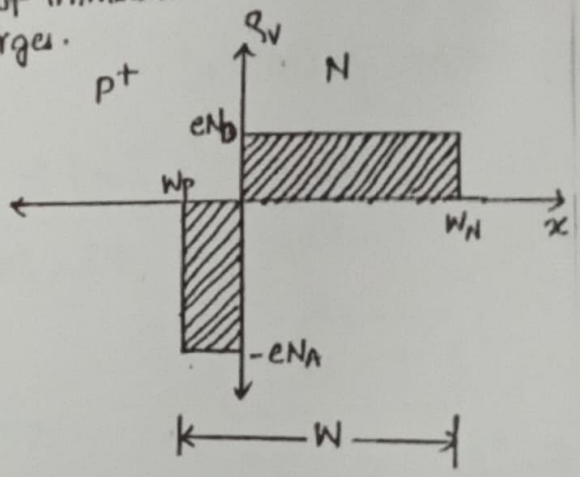
1> Transition capacitance

It appears when diode is in reverse bias. When the reverse voltage is increased depletion width increases and there by the amount of immobile charges present in depletion region also increases i.e, diode behaves as capacitor.

• The rate of change of immobile charge in the depletion region wrt the reverse voltage is known as transition capacitance. mathematically,

$C_T = \frac{\partial Q}{\partial V}$ where Q = Amount of immobile charges. V = reverse voltage





P^+N Junction:-

$N_A \gg N_D$, $W_P \ll W_N$

$W = W_N + W_P$

$W \approx W_N$

$C_T = \frac{\partial Q}{\partial V} = \frac{\partial Q}{\partial W} \times \frac{\partial W}{\partial V}$ ——— (1)

$Q = eN_D \times A \times W_N$

$Q \approx AeN_D W$

$\because \rho_V = \frac{Q}{V}$.

$Q = \rho_V \times V$

$Q = eN_D \times V$.

$$\boxed{\frac{\partial Q}{\partial W} = AeN_D}$$

From poisson's Equation

$$\frac{\partial^2 V}{\partial x^2} = -\frac{\rho_v}{\epsilon} \Rightarrow \int \frac{\partial^2 V}{\partial x^2} = \int -\frac{eN_D}{\epsilon}$$

$$\frac{\partial V}{\partial x} = \frac{-eN_D x}{\epsilon} + C_1 \text{ , At } x = W_N \text{ , } \frac{\partial V}{\partial x} = E = 0.$$

$$0 = \frac{-eN_D x}{\epsilon} + C_1 \Rightarrow C_1 = \frac{eN_D W_N}{\epsilon}$$

$$\int \frac{\partial V}{\partial x} = \int -\frac{eN_D x}{\epsilon} + \int \frac{eN_D W_N}{\epsilon}$$

$$V = -\frac{eN_D x^2}{2\epsilon} + \frac{eN_D W_N x}{\epsilon} + C_2$$

$C_2 = 0$, At $x = 0$, $V = 0$

Now, $V = -\frac{eN_D x^2}{2\epsilon} + \frac{eN_D W_N x}{\epsilon}$.

At N, $V = V_N$, $x = W_N$.

$$V_N = -\frac{eN_D W_N^2}{2\epsilon} + \frac{eN_D W_N^2}{\epsilon} = \frac{eN_D W_N^2}{2\epsilon}$$

$$\boxed{V_N = \frac{eN_D W_N^2}{2\epsilon}} \quad \text{IIIly} \quad \boxed{V_p = \frac{-eN_A W_p^2}{2\epsilon}}$$

$$V_B = V_N - V_p = \frac{eN_D W_N^2}{2\epsilon} + \frac{eN_A W_p^2}{2\epsilon}$$

$$V_B = \frac{e}{2\epsilon}\left[N_D \cdot W_N \cdot W_N + N_A \cdot W_p \cdot W_p\right]$$

$$V = \frac{e}{2\epsilon}\left[N_D W_N \left[W_N + W_p\right]\right].$$

$$V = \frac{e}{2\epsilon} N_D W^2 \quad \Big| \because W_N \approx W.$$

Where,

E = permitivity of S.C

A = area of cross section

W = width of depl reg.

$$\frac{\partial V}{\partial W} = \frac{\epsilon}{\epsilon} N_D \cdot W \quad , \quad \frac{\partial W}{\partial V} = \frac{\epsilon}{\epsilon N_D W}$$

$$C_T = A \epsilon N_D \times \frac{\epsilon}{\epsilon N_D \cdot W} \qquad \boxed{C_T = \frac{\epsilon A}{W}}$$

* Transition capacitance decreases with increases in the applied reverse voltage. Hence the diode in reverse bias can be used as voltage dependsardent capacitor.

* If a diode is used as a voltage dependent capacitor then it is called as varactor diode (or) variable capacitor diode.

2a) Derive the expression for Ripple factor for Full Wave Rectifier with L-section filter

An inductor is connected in series with load of the rectifier, it is also called as 'Choke filter'. The fundamental property of an inductor is that to "oppose any changes in the current passing through it". Thus an inductor presents high impedance to a.c (variations or ripples) and more to d.c. The inductor stores energy in it as magnetic field when the current is above its average value and delivers that energy to the circuit when the current tends to fall below the average level. Thus it reduces the pulsation of the rectifier output.

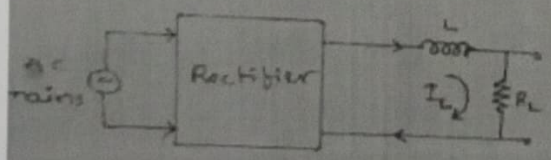


Figure: 2.8 (A)

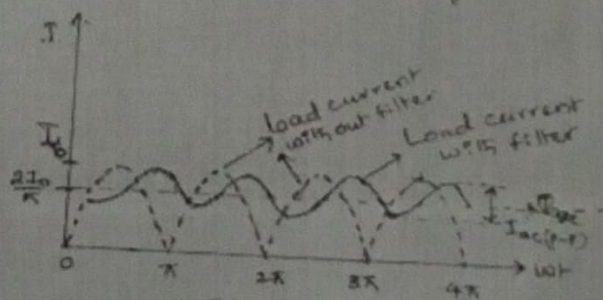


Figure: 2.8(B)

As shown in the figure 2.8(B) when output current tends to rise above the average value magnetic energy is stored in the inductor which has the effect of toning down or smoothening the sudden rise in current

However, when current tends to fall below the average value, this stores energy or returned to the circuit in an effort to prevent the current from falling down too much. In this way, current variations are reduced to the minimum. Thus the current through the load never drops to zero.

We know the load current for a full-wave rectifier is given by a Fourier series, i.e.

$$I = I_0\left[\frac{2}{\pi} - \frac{4}{3\pi}\cos 2\omega t - \frac{4}{15\pi}\cos 4\omega t \ldots\ldots\right]$$

The first term in the series represents the d.c while the rest represents a.c harmonics. The amplitudes of a.c terms beyond the [illegible] small compared with that of the first. Hence neglecting higher order the rectifier output is given by

$$I = I_0\left[\frac{2}{\pi} - \frac{4}{3\pi}\cos 2\omega t\right]$$

If R_{choke} is the resistance of the inductor (choke) and R_L the load. The d.c current and voltage across the load will be

$$I_{dc} = \frac{2V_0}{\pi(R_L + R_{choke})}$$ [Neglecting diode resistance which is very small]

If $R_{choke} << R_L$, $\boxed{I_{dc} = \frac{2V_0}{\pi R_L}}$

and $V_{dc} = I_{DC} R_L \Rightarrow V_{dc} = \frac{2V_0}{\pi(R_L + R_{choke})} R_L$

$$= \frac{2V_0}{\pi}\left[1 + \frac{R_{choke}}{R_L}\right]^{-1}$$

$$= \frac{2V_0}{\pi}\left[1 - \frac{R_{choke}}{R_L}\right]$$ [using binomial theorem]

$$= \frac{2V_0}{\pi} - \frac{2V_0}{\pi}\frac{R_{choke}}{R_L}$$

Output voltage $\boxed{V_{dc} = \frac{2V_0}{\pi} - I_{dc} \cdot R_{choke}}$

When no load is used ($I_{dc} = 0$) and hence

$$(V_{dc})_{NL} = \frac{2V_0}{\pi}$$

$$\therefore \text{Regulation} = \frac{\frac{2V_0}{\pi} - \left(\frac{2V_0}{\pi} - I_{dc} R_{choke}\right)}{\left(\frac{2V_0}{\pi} - I_{dc} R_{choke}\right)}$$

$$= \frac{I_{dc} R_{choke}}{\frac{2V_0}{\pi} - I_{dc} R_{choke}}$$

Since R_{choke} is generally too small, hence regulation factor is too much reduced. Therefore a better regulation is obtained.

The a.c component $I_0' = \frac{V_0}{Z}$

where $Z = R_L + j2X_L = \sqrt{R_L^2 + 4\omega^2 L^2}\ \angle\phi$ and $\phi = \tan^{-1}\frac{2\omega L}{R_L}$

Since inductor and load are in series, hence it serves as potential divider network.

$\therefore$ The peak value of the a.c voltage is $\frac{4V_0}{3\pi}$ [From the Fourier series Second term]

and r.m.s value of a.c component due to second harmonic is

$$I'_{rms} = \frac{1}{\sqrt{2}} \cdot \frac{4V_0}{3\pi \left[R_L^2 + 4\omega^2 L^2\right]^{1/2}}$$

$$\therefore \text{Ripple } \gamma = \frac{I'_{rms}}{I_{dc}} = \frac{4V_0/3\sqrt{2}\pi\,(R_L^2 + 4\omega^2 L^2)^{1/2}}{2V_0/\pi\,(R_L + R_{choke})}$$

$$= \frac{2}{3\sqrt{2}} \cdot \frac{(R_L + R_{choke})}{(R_L^2 + 4\omega^2 L^2)^{1/2}}$$

$$= \frac{2}{3\sqrt{2}} \cdot \frac{1}{\left[\frac{R_L^2}{(R_L + R_{choke})^2} + \frac{4\omega^2 L^2}{(R_L + R_{choke})^2}\right]^{1/2}}$$

If $R_L >> R_{choke}$, $\gamma = \frac{2}{3\sqrt{2}} \frac{1}{\left[1 + \left(\frac{2\omega L}{R_L}\right)^2\right]^{1/2}}$

neglecting 1 in comparision with $\left(\frac{2\omega L}{R_L}\right)^2$

$$r = \frac{2}{3\sqrt{2}} \cdot \frac{1}{\frac{2\omega L}{R_L}} = \frac{R_L}{3\sqrt{2}\,\omega L}$$

In case, the load is infinity i.e the out put is an open circuit, Then the ripple factor is $r = 0.471$. This is slightly less than the value of the full wave rectifier when no filter is used (i.e 0.482). It is clear that the inductor filter should only be used where R_L is considerably small. Hence the inductor filter is suitable for low load resistance. Because the ripple is inversely proportional to the value of the inductor.

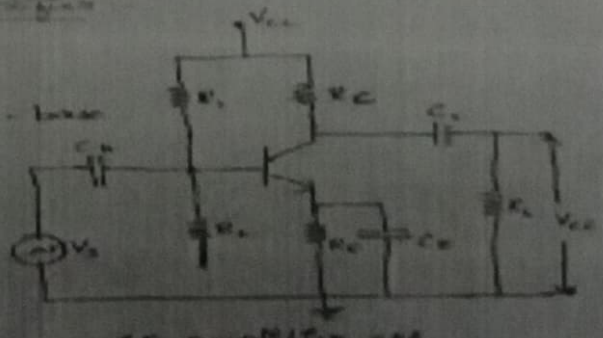
The disadvantage with this inductor filter is, for high load applications inductors are bulky, costlier and more power consuming.

NOTE: for $f = 50$ Hz, $r = \frac{R_L}{3\sqrt{2}\,\omega L} = 0.236\,\frac{R_L}{\omega L} = 0.236\,\frac{R_L}{2\pi f L}$

$$r = \frac{R_L}{1330\,L}$$

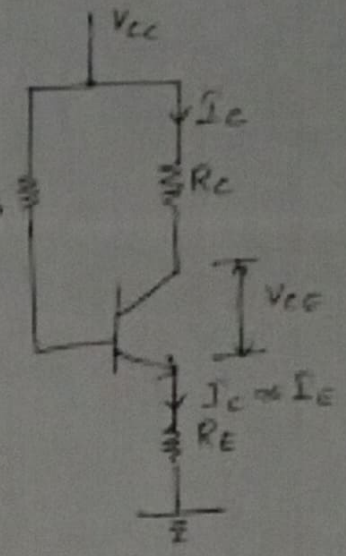
3a) Derive the operating point using AC and DC load lines.

- Operating point
- Biasing: In order to operate transistor in the desired region an external voltage has to be applied with correct polarity and magnitude to the two junctions of the transistor. This is known as biasing of the transistor.
- Because dc voltages are used to bias the transistor, biasing is known as dc biasing of the transistor.
- Operating point: When biasing is provided to a transistor, certain current and voltage conditions are established for the transistor.
- These conditions are known as operating point or operating conditions or quiescent point (it means quite, still, inactive)
- The operating point must be stable for proper operation of the transistor.
- The equivalent model of CE amplifier
- Transistor is biased with a common supply such that emitter base junction is forward biased & collector base junction is reverse biased, i.e. transistor is in active region.



CE amplifier ckt.

→ In the absence of AC signal, the capacitors provide very high impedance ie open circuit



DC equivalent ckt.

→ Applying KVL to the collector circuit we get,

$$V_{CC} = I_C R_C + V_{CE} + I_C R_E$$

$$V_{CC} = I_C (R_C + R_E) + V_{CE}$$

$$I_C (R_C + R_E) = V_{CC} - V_{CE}$$

$$\Rightarrow I_C = \left(\frac{-1}{R_C + R_E}\right) V_{CE} + \left(\frac{1}{R_C + R_E}\right) V_{CC}$$

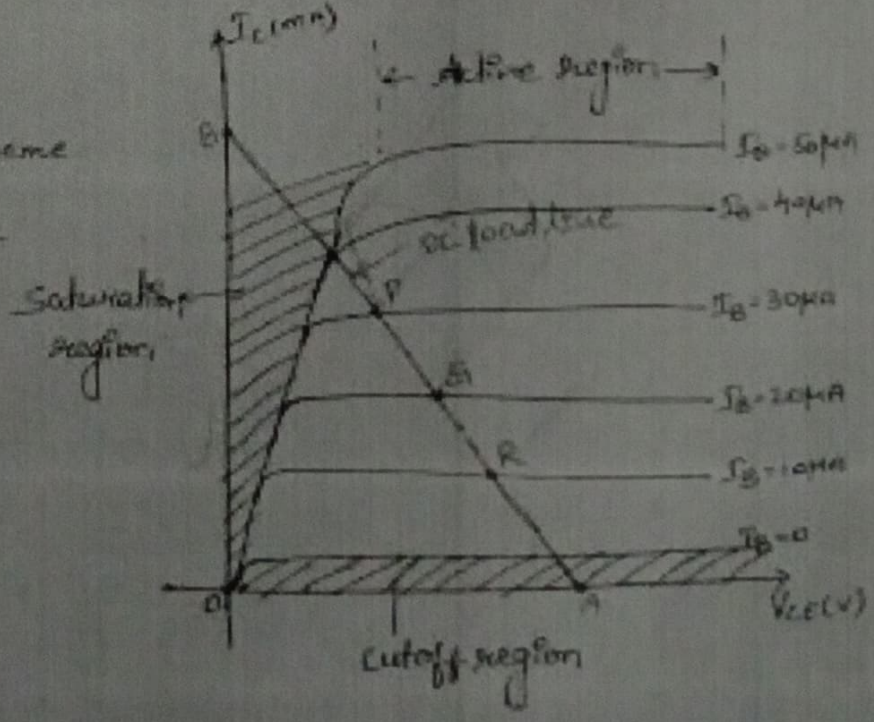
$$I_C = \left(\frac{-1}{R_{dc}}\right) V_{CE} + \frac{V_{CC}}{R_{dc}} \qquad R_{dc} = R_C + R_E$$

→ Compare this equation with $y = mx + C$.

→ I_C is a straight line on the graph of I_C vs V_{CE} which is having slope $\left(\frac{-1}{R_{dc}}\right)$.

→ To determine the 2 extreme points on the line, assume

(i) $V_{CE} = V_{CC}$ & (ii) $V_{CC} = 0$



i) When $V_{CE} = V_{CC}$

$\Rightarrow I_C = 0$, point A

ii) When $V_{CE} = 0$

$\Rightarrow I_C = \frac{V_{CC}}{R_{dc}}$, point B

→ The line drawn between the points A & B on the output characteristics is called <u>dc load line</u>

→ The 'dc' word indicates that only dc conditions are considered i.e. Input ac signal is assumed to be zero.

→ The intersection of the characteristic curve and dc load line is the operating point.

→ The point is fixed on the curve, so it is called as quiescent point or <u>Q point</u>

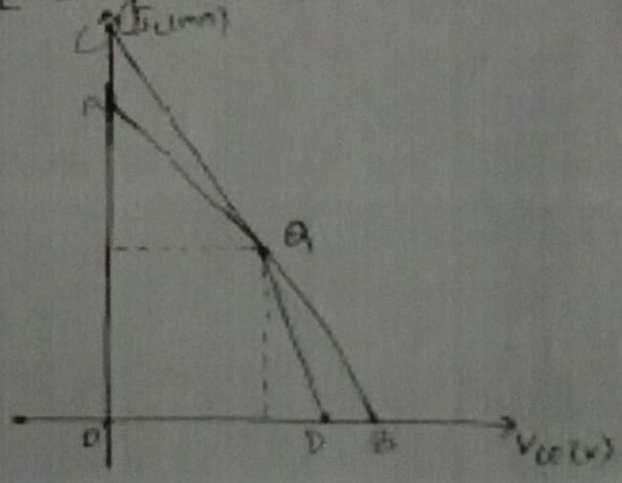
→ For different values of I_B, there will be different intersection points (P, Q, R in the fig)

→ After choosing the Q point at the center of the dc load line, <u>ac load line</u> is also drawn through the Q point.

→ The effective ac load resistance R_{ac} is given as

$$R_{ac} = R_c \| R_L$$

$$\text{Slope of } CQD = \left(\frac{-1}{R_{ac}}\right)$$



→ To draw ac load line, max V_{CE} & max I_C when the signal is applied are required

max $V_{CE} = V_{CEQ} + I_{CQ} R_{ac}$, point D

max $I_C = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$, point C

3b) Explain about Punch through and Base width modulation.

3.7.5 Early effect (Base-width modulation):- In the C-B configuration, as the collector voltage V_{CC} is made to increase the reverse bias, the space charge (depletion region) width between the collector and base tends to increase, with the result that the effective width of the base decreases. This dependency of base-width on collector-to-base voltage V_{CB} is known as the base-width modulation or Early effect. This decrease in the base width has three consequences:

(i) There is less chance for recombination with in the base region. Hence α increases with V_{CB}.

(ii) The charge gradient is increased with in the base, and consequently, the current of minority carriers injected across the emitter junction increases.

(iii) For extremely large voltages, the effective base-width may be reduced to zero, causing voltage breakdown in the transistor. This phenomenon is called the punch through effect.

4a) Draw and explain the CE characteristics of a transistor.

3.7.3.1 V-I characteristics of C-E configuration –

The characteristics of a pnp transistor connected in the common emitter configuration may be determined by the use of a circuit as shown in the figure 3.19

In this circuit the variable d.c source V_{BB} and provides forward bias to emitter junction. A voltmeter is connected across base(B) and emitter(E) to measure V_{BE}.

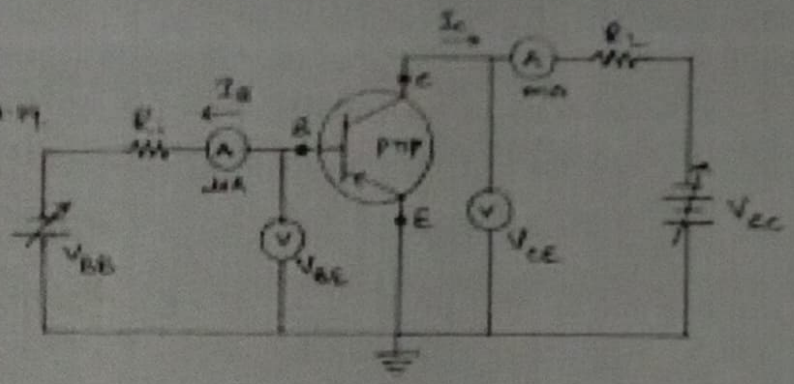


Figure: 3.19

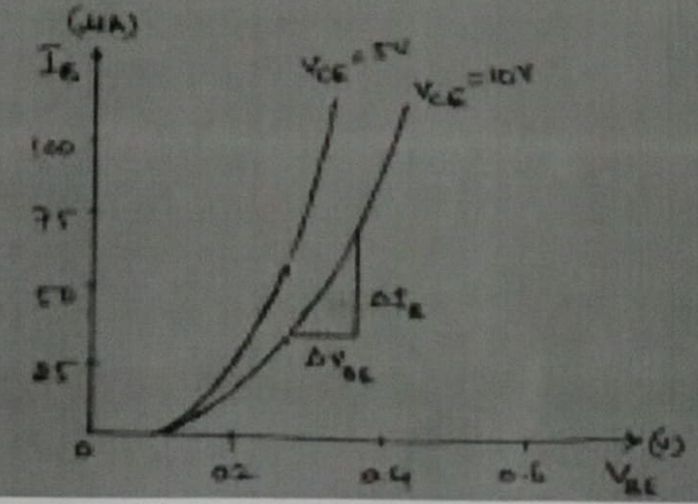
A micro-ammeter is connected in series with the base to measure I_B. Similarly a milliammeter is connected in the collector circuit to measure I_C. To measure V_{CE} another voltmeter is connected across collector(C) and emitter(E). A variable source V_{cc} is connected between C and E to vary V_{CE}.

3.7.3.2 Input characteristics:– The curves, showing the variation of the base current (I_B) with base-emitter voltage V_{BE} at constant collector-emitter voltage V_{CE}, are called the input characteristics of a C-E transistor.

For plotting the input characteristics, the collector-emitter voltage V_{CE} is kept fixed, the base-emitter voltage V_{BE} is varied with the help of variable d.c source V_{BB} and the base current I_B is noted for each value of V_{BE}. A graph of I_B against V_{BE} is then plotted. The procedure is repeated for other fixed values of V_{CE}. The curves so obtained is known as input characteristics of C-E transistor, as shown in the figure: 3.20

A study of these curves reveals the following facts:

(i) the characteristics resembles that of a forward-biased diode curves. This is expected because the base-emitter section of the transistor is a diode and it is forward biased.



(iii) In this case, I_B increases fast rapidly with V_{BE} as compared to C.B confi, which shows that the input resistance of C.E configuration is higher compared to that in C.B configuration.

$$R_{in} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE} = \text{constant}}$$

3.7.3.3 Output characteristics :- The curves, showing the variation of the collector current I_C with collector-emitter voltage V_{CE} at a constant base current I_B, are called the output characteristics of a common emitter transistor.

For plotting output characteristics, the base current I_B is kept fixed, with the help of variable d.c source V_{CC} the value of V_{CE} is varied in steps and the collector current I_C is noted for each value of V_{CE}. The procedure is repeated for other fixed values of I_B. A graph of I_C against V_{CE} is then plotted. The curves so obtained are known as output characteristics as shown in the figure: 3.21.

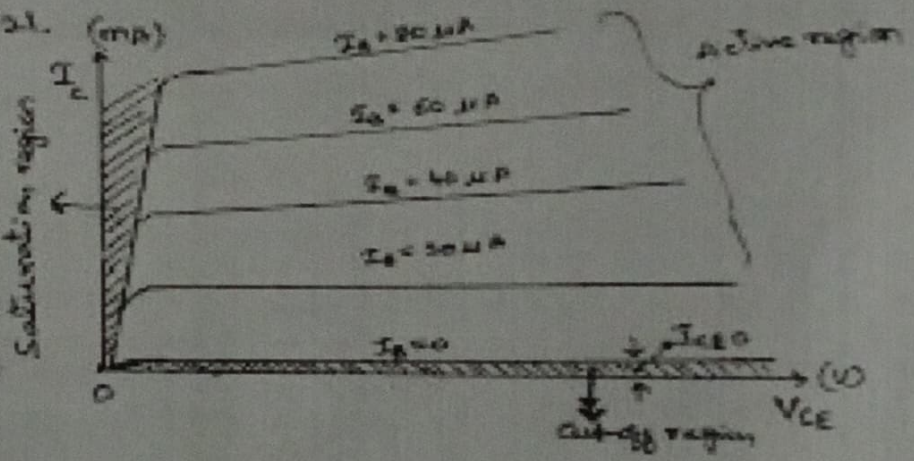


Figure : 3.21

A study of these curves reveals the following facts:

(i) The I_C varies rapidly with V_{CE} for very small voltages. After this I_C becomes almost constant and is decided entirely by base current I_B and becomes independent of V_{CE}.

(ii) The I_C is not zero when base current is zero, this is due to the inherent intrinsic conduction in semiconductors i.e due to minority carriers.

(iii) Since the base current I_B is in micro amperes and I_C is in milliamperes, the common emitter configuration exhibits a current amplification.

$$\beta = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE} = \text{constant}}$$

Just like C.B, the family of O/P curves is divided into three regions:

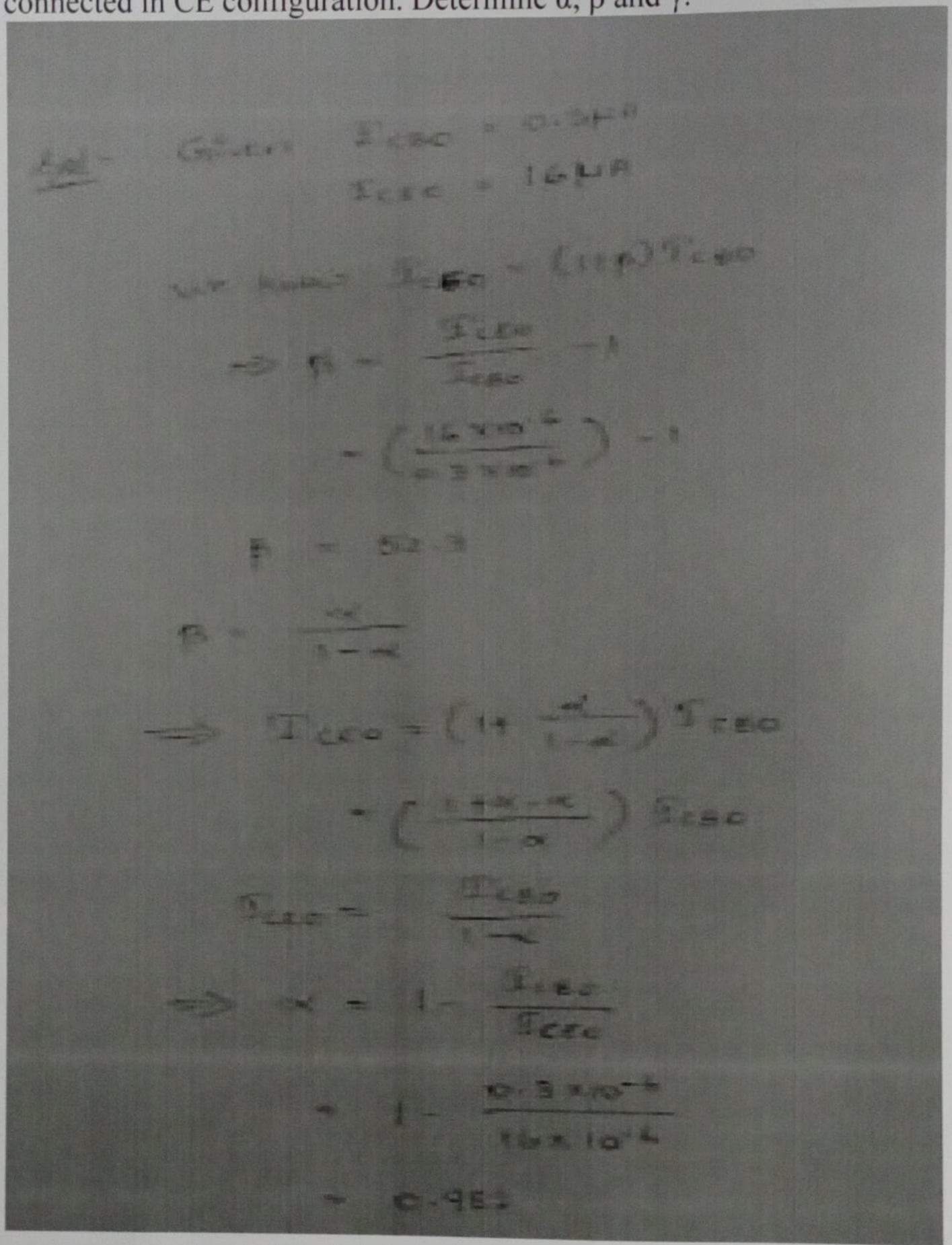
① Active region :- when emitter junction is forward biased and collector junction is reverse biased, the area above $I_B = 0$ and to the right side of ordinate, is known as active region.

for a given value of I_B, the emitter injects certain number of majority charge carriers into the base when collector-emitter voltage V_{CE} is small, the collector is unable to collect all charge carriers. Therefore, when V_{CE} is increased, collector current I_C first increases (as it collects maximum injected carriers) and then the rate of increase is quite small.

(ii) Saturation region: The region very close to the zero voltage axis where all the curves merge and fall rapidly towards origin, is known as Saturation region. In this region, the emitter junction as well as collector junction are forward biased.

(iii) Cut-off region: when both emitter junction and collector junction are reverse biased, the characteristic for $I_B = 0$ passes through origin but there is appreciable gap between the curve for $I_B = 0$ and x-axis. This small amount of current I_{CEO} is known as reverse leakage current and the area under the $I_B = 0$ and x-axis is known as the cut-off region.

4b) The reverse leakage current of the transistor when in CB configuration is 0.3μA while it is 16μA when the same transistor is connected in CE configuration. Determine α, β and γ.



6b) Draw the circuit diagram of SCR and explain its operation along with its characteristics

Silicon Controlled Rectifier (SCR)

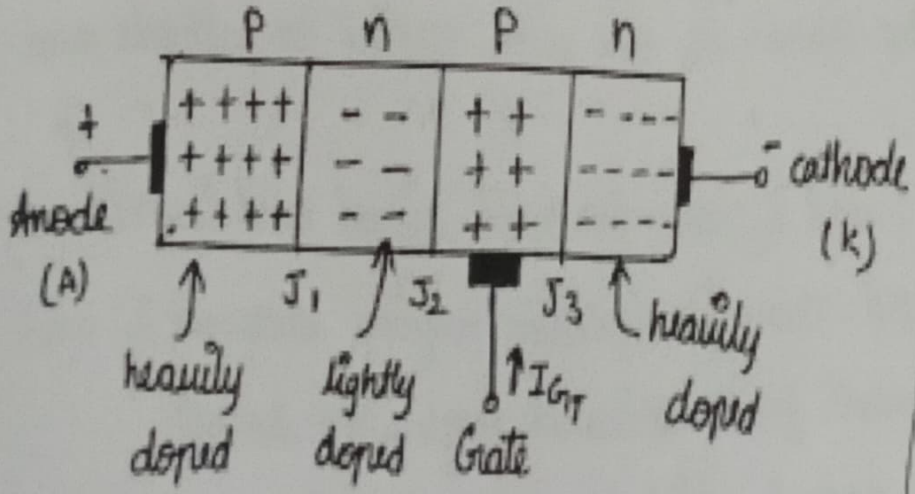
Construction:

→ The SCR is a four layer p-n-p-n device where p and n layers are alternately arranged. The outer layers are heavily doped while inner layers are lightly doped.

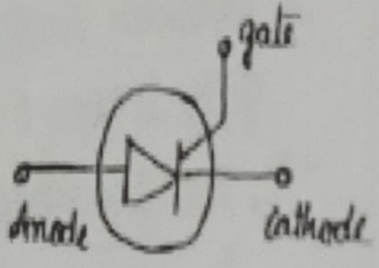
→ There are three p-n junctions called J_1, J_2 and J_3

→ The outer p layer is called anode while outer n layer is called cathode. Middle p layer is called gate

→ The three terminals are taken out respectively from these three layers, as shown in figure



Construction of SCR



Symbol of SCR

Anode must be positive with respect to cathode of forward bias the SCR

→ But this is not sufficient criterion to turn SCR ON. To make it ON, a current is to be passed through the gate terminal denoted as I_{GT}. Thus it is a current operated device

→ The I_{GT} is gate trigger current required to make the SCR ON

→ The basic material used for the SCR fabrication is silicon

Working principle Of SCR

The operation of SCR is divided into two categories,
i) when gate is open and ii) when gate is closed

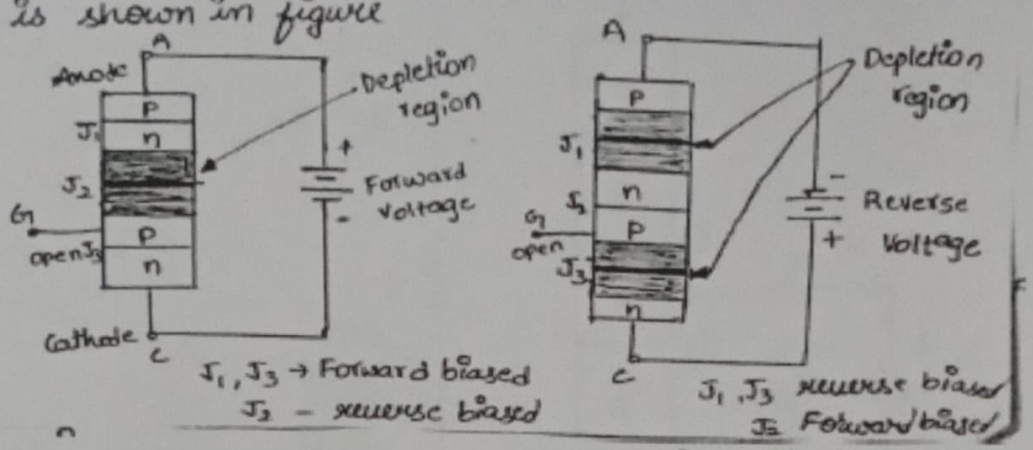
1) When gate is open:

→ Consider that the anode is +ve with respect to cathode and gate is open

→ The junctions J_1 and J_3 are forward biased and junction J_2 is reverse biased. There is depletion region around J_2 and only leakage current flows which is negligibly small

→ Practically the SCR is said to be OFF. This is called forward blocking state of SCR and voltage applied to anode and cathode with anode +ve is called forward voltage.

This is shown in figure



→ With gate open if cathode is made +ve with (16)
to anode, the junctions J_1, J_3 become reverse biased and J_2 forward biased. still the current flowing is leakage current, which can be neglected as it is very small

→ The voltage applied to make cathode +ve is called reverse voltage and SCR is said to be in reverse blocking state. This is shown in the figure

→ In forward blocking state, if the forward voltage is increased and made sufficiently large, the reverse biased junction J_2 breaks down and SCR conducts heavily

2) When gate is closed:

→ Consider that the voltage is applied between gate and cathode when the SCR is in forward blocking state

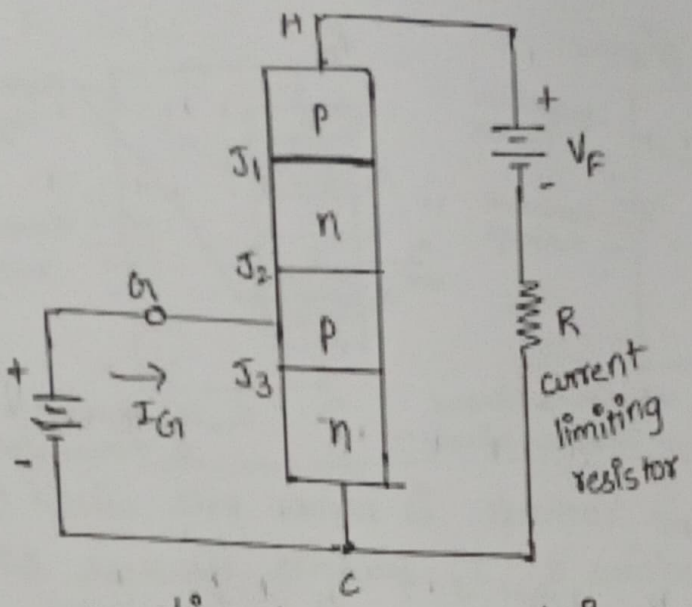
→ The gate is made positive with respect to the cathode.

→ The electrons from n-type cathode which are majority in number, cross the junction J3 to reach to positive of battery

→ While holes from P types move towards the negative of battery, this constitutes the gate current

→ This current increases the anode current as some of electrons cross junction J_2. As anode current increases, more electrons cross the junction J_2 and the anode current further increases

→ The resistance R is required to limit the current.



operation of SCR when gate is closed

→ once the SCR conducts, the gate loses its control

Characteristics of SCR:

1) Forward characteristics:

→ It shows a forward blocking region, when $I_G = 0$, It also shows that when forward voltage increases upto V_{BO}, the SCR turns ON and high current results. The drop across SCR reduces suddenly which is now the ohmic drop in the four layers. The current must be limited only by the external resistance in series with the device

→ It also shows that, if gate bias is used then as gate current increases, less voltage is required to turn ON the SCR.

→ If the forward current falls below the level of the holding current I_H, then depletion region begins to develop around J_2 and device goes into the forward blocking region

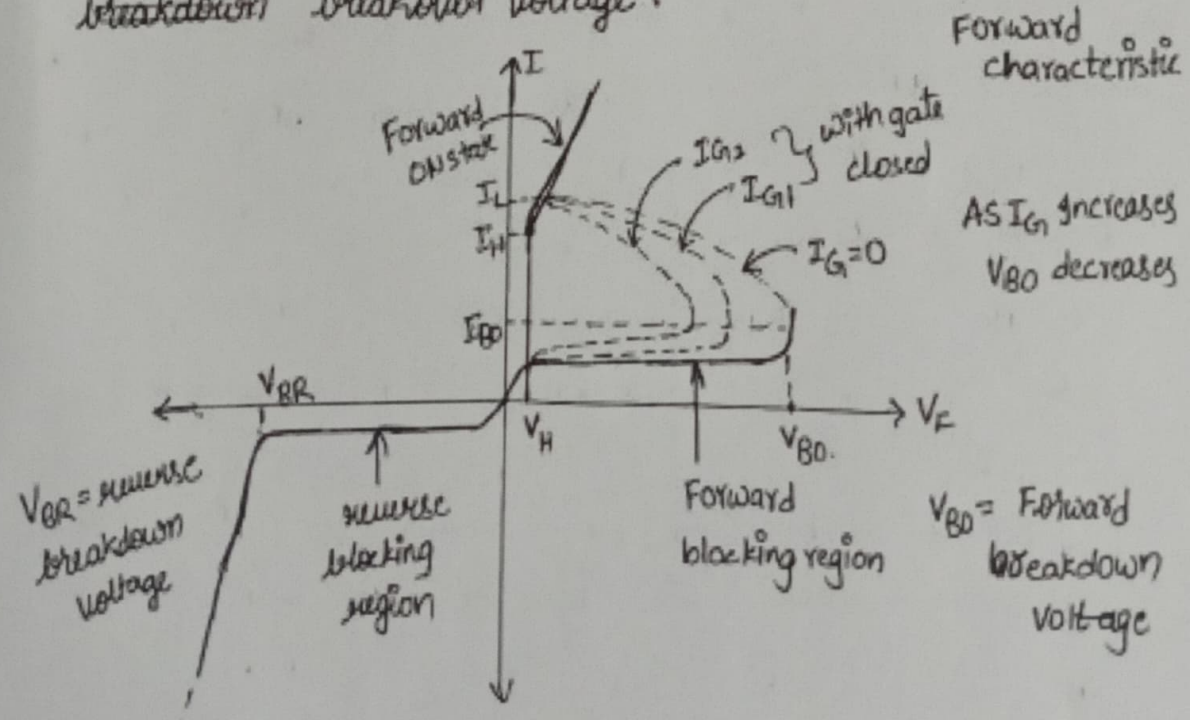
→ When SCR is turned ON from OFF state, the resulting forward current is called latching current I_L. The latching current is slightly higher than the holding current

Reverse Characteristics:

→ If the anode to cathode voltage is reversed, then the device enters into the reverse blocking region. The current is negligibly small and practically neglected.

→ If the reverse voltage is increased, similar to the diode, at a particular value avalanche breakdown occurs and a large current flows through the device. This is called reverse breakdown and the voltage at which this happens is called reverse breakdown voltage V_{BR}.

→ The forward breakover voltage is greater than reverse breakdown breakover voltage.



Characteristics of SCR

7a) Draw and Explain BJT small signal model, compare the performance of CE, CB, CC amplifier

BJT Hybrid model :—

The components of a small-signal low frequency equivalent circuit are called hybrid parameters or h-parameters, the equivalent circuit is called the hybrid model or h-parameter model. these parameters are denoted by h_i, h_r, h_f and h_o. From the two port network representation as shown in figure 5.1, for each port, there are two variables current and voltage (i.e I and V).

In general, transistor is a current controlled device, thus input current is an independent variable. The input voltage and output current are the functions of input current and output voltage, is given as

$$V_i = f_1(I_i, V_o) \quad \text{—— (3)}$$

$$I_o = f_2(I_i, V_o) \quad \text{—— (3)}$$

Thus, these four variables can be related by the following equation

$$V_i = h_{11} I_i + h_{12} V_o \quad \text{—— (4)}$$

$$I_o = h_{21} I_i + h_{22} V_o \quad \text{—— (5)}$$

where V_i = Input voltage, I_i = input current,

V_o = output voltage, I_o = output current.

The parameters, h_{11}, h_{12}, h_{21} & h_{22} which relating the four variables of the two port system are called h-parameters. From equations (4) & (5). h-parameters may be defined by first putting $V_o = 0$ (i.e output terminals are short circuited) and then $I_i = 0$ (i.e input terminals open circuited). Thus

(1) with output short circuited (i.e $V_o = 0$)

from equation (4) $V_i = h_{11} I_i \Rightarrow h_{11} = \frac{V_i}{I_i}$

and from (5) $I_o = h_{21} I_i \Rightarrow h_{21} = \frac{I_o}{I_i}$

$\therefore h_{11} = \left.\frac{V_i}{I_i}\right|_{V_o=0} = h_i$ = Input impedance (Ω)

and $h_{21} = \left.\frac{I_o}{I_i}\right|_{V_o=0} = h_f$ = Forward current transfer ratio or forward current gain (no units)

(ii) With input open circuited (i.e. $I_i = 0$)

from equation ④ $V_i = h_{12} V_o \Rightarrow h_{12} = \frac{V_i}{V_o}$

and from ⑤ $I_o = h_{22} V_o \Rightarrow h_{22} = \frac{I_o}{V_o}$

$\therefore h_{12} = \left.\frac{V_i}{V_o}\right|_{I_i=0} = h_r$ = Reverse voltage transfer ratio or Reverse voltage gain (no units)

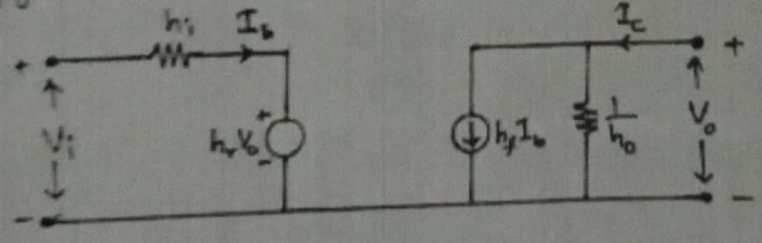
and $h_{22} = \left.\frac{I_o}{V_o}\right|_{I_i=0} = h_o$ = output admittance (Siemen)

It may seen that two of these h-parameters (h_{12}, h_{21} or h_r, h_f) are the ratios and hence they have no units. The other two h_{11}, h_{22} (or h_i, h_o) have dimensions of impedance (ohm) and admittance (Siemen) respectively. They are thus a mixture of different units and hence the name hybrid h-parameters. These h-parameters have the following advantages:

i) The h-parameters are real numbers at audio frequencies.
ii) They can be measured easily.
iii) They are particularly suitable for circuit analysis and design.
iv) They are specified by the transistor manufacturers.
v) They can be obtained from the transistor characteristics curves.

* h-parameter equivalent circuit for transistor :-

To analyse the performance of transistors, they are conveniently represented by h-parameter equivalent circuit. The h-parameter equivalent circuit can be drawn with the help of two equations ④ and ⑤, as shown in figure 5.6.



	C·E	C·B	C·C
Current gain	High	Low	High
Input impedance	Medium	Low	High
voltage gain	High	High	LOW
output impedance	Medium	High	Low

8a) Explain the working of MOSFET amplifier and discuss the gain and frequency response characteristics.

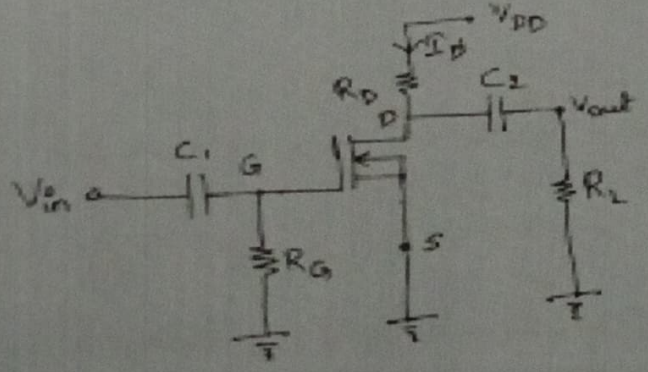
MOSFET Amplifiers

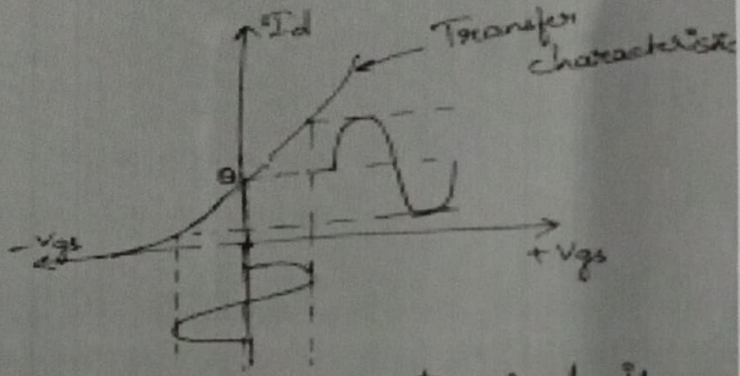
→ To produce linear amplification, MOSFET has to operate in its saturation region.

→ It needs to be biased around a centrally fixed Q-point.

Common-Source Depletion MOSFET Amplifier:

→ Source terminal is common for both input & output.





→ Gate is at approximately 0V dc & the source terminal is grounded, thus making $V_{gs} = 0V$.

→ When V_{in} is applied, V_{gs} swings above & below its zero value, producing a swing in drain current I_d.

→ During +ve half cycle of the signal, the +ve voltage on the gate increases & produces the enhancement mode. This increases the channel conductivity & hence the drain current I_d.

→ During -ve half cycle, the +ve voltage decreases & produces depletion mode. This decreases the conductivity & hence I_d.

→ A small change in gate voltage produces a large change in drain current I_d.

→ Large variation in I_d produces a large a.c o/p voltage across R_D

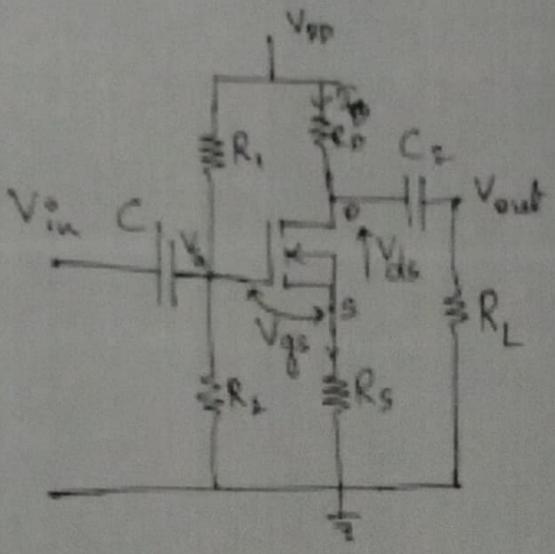
→ Voltage gain $A_V = g_m R_D$ or $A_V = g_m R_D'$ $(R_D' = R_D \| R_L)$

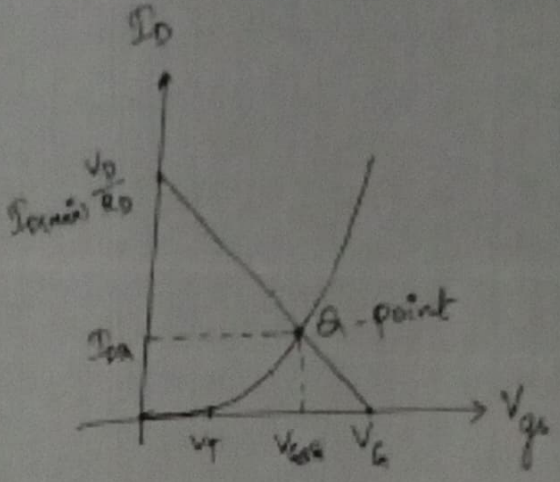
* Common-Source Enhancement MOSFET Amplifier:

→ The In E-MOSFET, current starts to conduct when there is a minimum V_{gs} called threshold voltage (V_T) is applied to the gate thus allowing the drain current to flow.

→ E-MOSFET doesnot conduct until the V_{gs} is less than V_T. If $V_{gs} \geq V_T$, E-MOSFET starts conducting.

→ If forward bias at the gate increases, I_d will also increase making the E-MOSFET ideal for use in MOSFET amplifier circuits.





$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

$$= I_D (R_D + R_S) + V_{DS}$$

$$\Rightarrow R_D + R_S = \frac{V_{DD} - V_{DS}}{I_D}$$

$$V_{GS} = V_G - I_S R_S$$

→ V_{GS} should be greater than V_T & $I_S = I_D$

$$V_{GS} = V_G - I_D R_S$$

$$\therefore V_G = V_{GS} + I_D R_S$$

$$(or) \quad V_G = V_{GS} + V_S$$

→ Since, no current flows into the gate terminal of a MOSFET

$$V_G = V_{DD}\left(\frac{R_2}{R_1 + R_2}\right)$$

8b) An n-channel JFET has IDSS =10mA and VP = - 2V. Determine the drain source resistance rds for (i) VGS =0V. (ii) VGS = - 0.5V

Sol:- Given $I_{DSS} = 10mA$

$V_p = -2V$

find r_{ds} when (i) $V_{GS} = 0V$ & (ii) $V_{GS} = -0.5V$

$$r_{ds} = \frac{V_p^2}{2 I_{DSS}(V_{GS} - V_p)}$$

(i) $V_{GS} = 0$

$$r_{ds} = \frac{(-2)^2}{2 \times 10 \times 10^{-3}(2)}$$

$$= 100\Omega$$

(ii) $V_{GS} = -0.5V$

$$r_{ds} = \frac{(-2)^2}{2 \times 10 \times 10^{-3}(-0.5+2)}$$

$$= 133.33\Omega$$

UNIT I

Diode and Applications

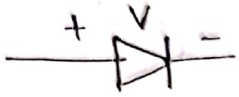
⇒ Static and Dynamic Resistance.

→ A diode has two types of resistors.

(i) Static or DC resistance (ii) Dynamic or AC resistances.

(i) **Static resistance:-** It is defined as the ratio of the voltage across the diode to the current passing through the diode.

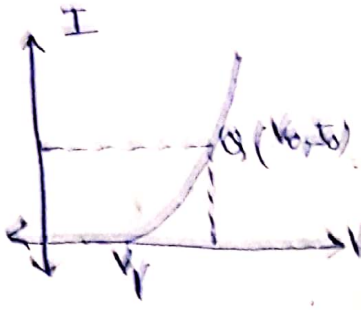
Mathematically, $\boxed{R = \frac{V}{I}}$



where V is the voltage across the diode, I is current passing through the diode.

(ii) **Dynamic resistance:-** It is defined as reciprocal of the slope of V-I characteristics of diode.

Mathematically, $\text{Slope} = \frac{\partial I}{\partial V}$ $r = \frac{1}{\text{slope}} = \frac{\partial V}{\partial I}$.



The current passing thgh diode,

$$I = I_0 \left[e^{V/\eta V_T} - 1 \right].$$

$$I = I_0 e^{V/\eta V_T} - I_0 \quad \text{---(1)}.$$

$$\frac{\partial I}{\partial V} = I_0 \cdot e^{V/\eta V_T} \frac{1}{\eta V_T}.$$

$$\frac{\partial I}{\partial V} = \frac{I + I_0}{\eta V_T}.$$

In forward bias $I \gg\gg I_0$, $\frac{\partial I}{\partial V} = \frac{I}{\eta V_T}$.

$$r = \frac{\partial V}{\partial I} \qquad \boxed{r \approx \frac{\eta V_T}{I}}$$

Scanned by CamScanner

(7) → If voltage across diode is V_D and current passing through diode is I_D, then (V_D, I_D) is the operating point of diode on VI characteristics.

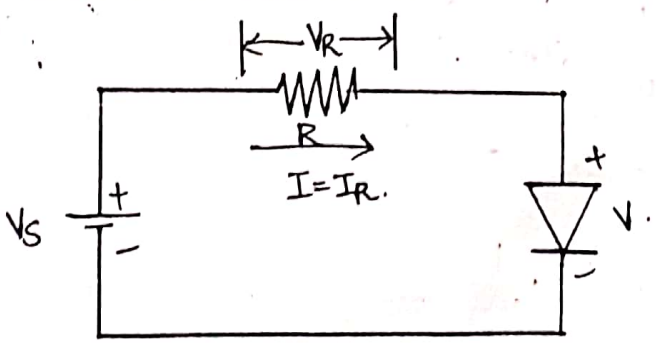
→ ~~If~~ diode is a non-linear element because the current varies non-linearly with respect to voltage.

→ If diode voltage is varied by a small amount. i.e, a few milli volts then diode current varies almost linearly with voltage. This is called a small signal operation of diode.

→ In small signal operation diode behaves as linear resistor.

→ The resistor offered by the diode in small signal operation is known as dynamic resistance or AC resistance or small signal resistance.

⇒ Diode equivalent circuit.



Simple diode circuit.

→ The PN junction diode is considered as a circuit element. The basic diode circuit shown above consists of a dc voltage V_s which is supplied across a resistor and a diode. In order to find the instaneous

Scanned by CamScanner

⑤ -diode voltage V and current I, the circuit can be analysed when the instantaneous source voltage is V_s. From KVL, the instantaneous diode voltage is

$$V_s = IR + V \quad \text{——(1)}$$

which can be expressed as $I = \frac{V_s}{R} - \frac{V}{R}$.

The ideal diode current equation relating the diode voltage V_D and current I_D is

$$I = I_0 \left[e^{(V/\eta V_T)} - 1 \right] \quad \text{——(2)}$$

where I_0 diode rev. Sat current at room temp. η is a constant (1 for Ge and 2 for Si) and V_T is thermal voltage i.e., $V_T = \frac{T}{11,600}$ in which T is the temperature of the diode junction (300K) or $V_T = 26$ mV at room temp.

Sub (2) in (1)

$$V_s = I_0 R \left[e^{(V/\eta V_T)} - 1 \right] + V.$$

As these equations contains both linear and exponential terms, it is difficult to solve by hand.

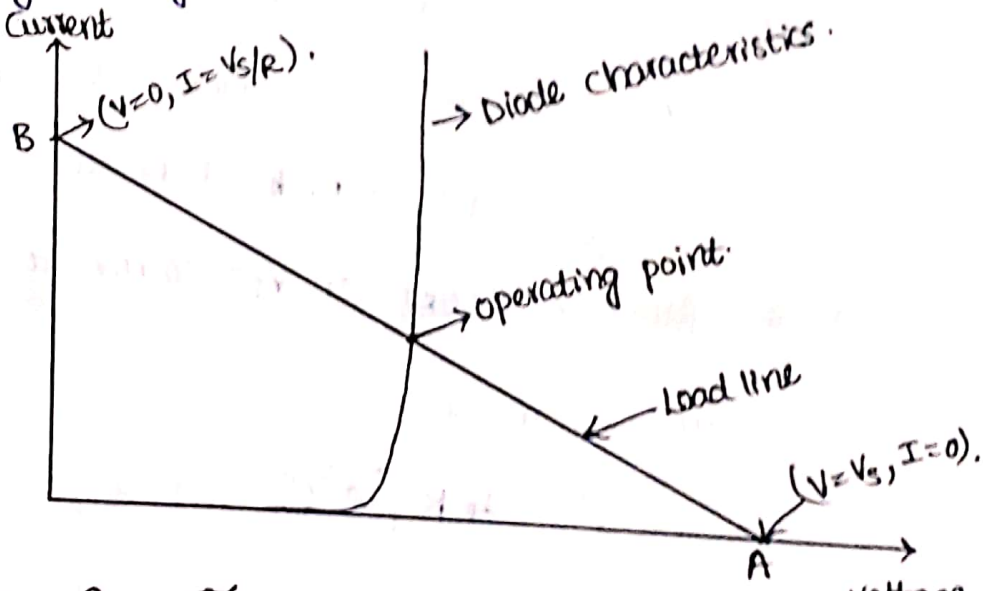
⇒ Load line Analysis:-

In the second method to draw the load line, I is determined when the device is short-circuited and V is determined when the device is open-circuited. So that the point B(V=0, $I = V_s/R$)

∵ on y-axis x coordinate is zero.
$V_s = IR + 0$.

Scanned by CamScanner

④ and A($V = V_s, I = 0$) lies somewhere on the y-axis and x-axis respectively of the diode characteristic curve as shown in figure. Thus a straight line drawn connecting the points A and B is called load line. This load line intersects the diode diode characteristics at some point which is chosen as operating point for the device. The operating point provides the diode voltage V_D appearing across the diode and the current I_D flowing through the diode.



Load line curve for Fixing the operating point.

✱ Diode Capacitances ✱

→ Diode has two types of capacitances.

1) ↳ Transition/ Junction/ Depletion/ Space charge capacitance.

2) ↳ Diffusion Capacitance.

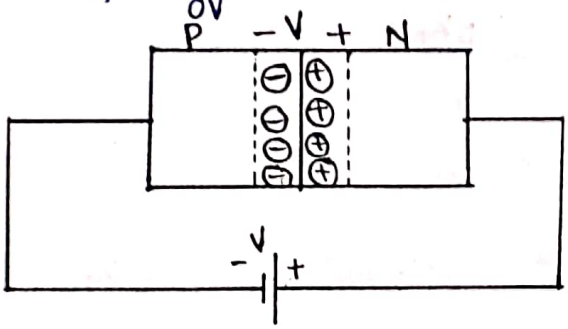
Scanned by CamScanner

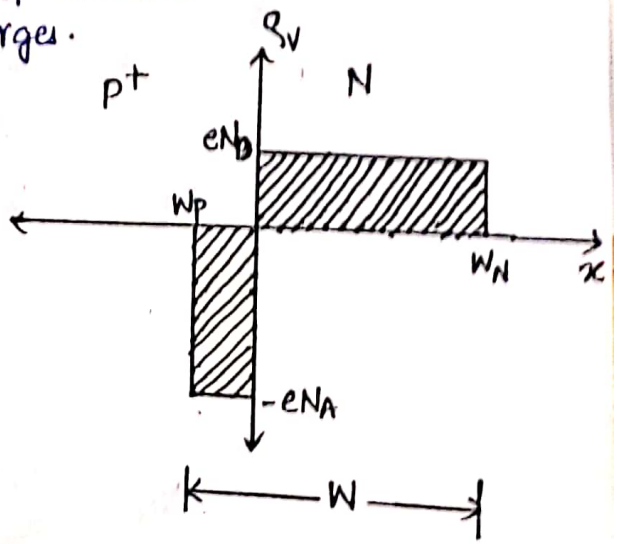
1> Transition Capacitance

It appears when diode is in reverse bias. When the reverse voltage is increased depletion width increases and there by the amount of immobile charges present in depletion region also increases i.e., diode behaves as capacitor.

• The rate of change of immobile charge in the depletion region wrt the reverse voltage is known as transition capacitance. mathematically,

$C_T = \frac{\partial Q}{\partial V}$ where Q = Amount of immobile charges. V = reverse voltage





P^+N Junction:-

$N_A \gg N_D$, $W_P \ll W_N$

$W = W_N + W_P$

$W \approx W_N$

$C_T = \frac{\partial Q}{\partial V} = \frac{\partial Q}{\partial W} \times \frac{\partial W}{\partial V}$ —— (1)

$Q = eN_D \times A \times W_N$

$Q \approx AeN_D W$

$\because \rho_V = \frac{Q}{V}$.

$Q = \rho_V \times V$

$Q = eN_D \times V$.

$$\boxed{\frac{\partial Q}{\partial W} = AeN_D}$$

Scanned by CamScanner

⑥ From poisson's Equation

$$\frac{\partial^2 V}{\partial x^2} = -\frac{\rho_v}{\epsilon} \Rightarrow \int \frac{\partial^2 V}{\partial x^2} = \int -\frac{eN_D}{\epsilon}$$

$$\frac{\partial V}{\partial x} = \frac{-eN_D x}{\epsilon} + C_1, \quad \text{At} \quad x = W_N, \quad \frac{\partial V}{\partial x} = E = 0.$$

$$0 = \frac{-eN_D x}{\epsilon} + C_1 \Rightarrow C_1 = \frac{eN_D W_N}{\epsilon}$$

$$\int \frac{\partial V}{\partial x} = \int -\frac{eN_D x}{\epsilon} + \int \frac{eN_D W_N}{\epsilon}$$

$$V = -\frac{eN_D x^2}{2\epsilon} + \frac{eN_D W_N x}{\epsilon} + C_2$$

$C_2 = 0$, At $x = 0$, $V = 0$

Now, $V = -\frac{eN_D x^2}{2\epsilon} + \frac{eN_D W_N x}{\epsilon}$.

At N, $V = V_N$, $x = W_N$.

$$V_N = -\frac{eN_D W_N^2}{2\epsilon} + \frac{eN_D W_N^2}{\epsilon} = \frac{eN_D W_N^2}{2\epsilon}$$

$$\boxed{V_N = \frac{eN_D W_N^2}{2\epsilon}} \quad \text{Illy} \quad \boxed{V_P = \frac{-eN_A W_P^2}{2\epsilon}}$$

$$V_B = V_N - V_P = \frac{eN_D W_N^2}{2\epsilon} + \frac{eN_A W_P^2}{2\epsilon}$$

$$V_B = \frac{e}{2\epsilon}\left[N_D \cdot W_N \cdot W_N + N_A \cdot W_P \cdot W_P\right]$$

$$V = \frac{e}{2\epsilon}\left[N_D W_N \left[W_N + W_P\right]\right].$$

$$V = \frac{e}{2\epsilon} N_D W^2 \quad \Big| \because W_N \approx W.$$

Where,

E = permitivity of S.C

A = area of cross section

W = width of depl reg.

Scanned by CamScanner

$$\frac{\partial V}{\partial W} = \frac{e}{\epsilon} N_D \cdot W \quad , \quad \frac{\partial W}{\partial V} = \frac{\epsilon}{e N_D \cdot W}$$

$$C_T = A e N_D \times \frac{\epsilon}{e N_D \cdot W} \qquad \boxed{C_T = \frac{\epsilon A}{W}}$$

* Transition capacitance decreases with increases in the applied reverse voltage. Hence the diode in reverse bias can be used as voltage dependent capacitor.

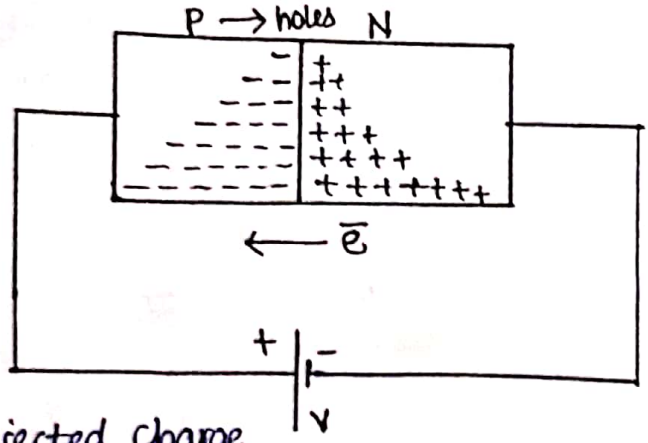
* If a diode is used as a voltage dependent capacitor then it is called as varactor diode (or) variable capacitor diode.

2> Diffusion Capacitance.

→ It occurs when the diode is operated in forward bias. When forward bias is occured the +ve charge i.e, holes injected into N-side and -ve charge i.e, free electoons inject into P-side. This injected carriers maximum near the junction and gradually decreases due to the recombination.

→ When forward voltage is increased the flow of holes from P to N and flow of ēs from N to P increases. Hence the injected charge carrier also increases.

→ The rate of change of injected charge wrt forward voltage is called diffusion capacitance.



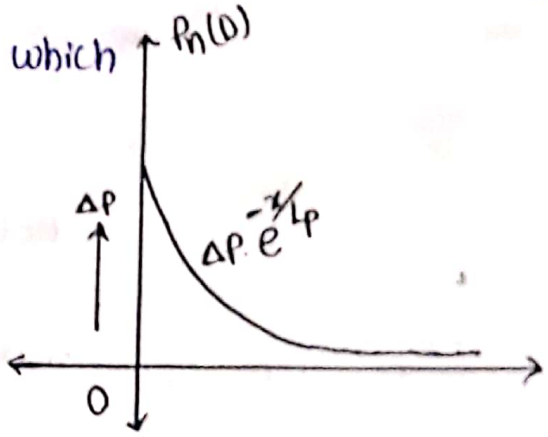
$$C_D = \frac{\partial Q}{\partial V}.$$ Where Q = injected charge

V = forward voltage.

Scanned by CamScanner

(8)

Consider a p^+N junction in F.B. in which current is dominantly due to holes.



The differential amount of injected charge on N-side is

$$\partial Q = \text{Injected hole density} \times \underbrace{e \times A \times dx}_{\text{differential volume.}}$$

$$\partial Q = eA \times \Delta P\, e^{-x/L_p} \times dx$$

Total charge is integration of above equation over length of n region

$$Q = eA \times \int_{x=0}^{x=x_N} \Delta P.\, e^{-x/L_p}\, dx \Rightarrow eA \times \Delta P \left[e^{-x/L_p}\right]_{x=0}^{x_N} \times \frac{1}{\left[1/-L_p\right]}.$$

$$Q = -eA\,\Delta P.\left[e^{-x_N/L_p} - e^{0}\right] \times L_p$$

But $x_N >>> L_p \Rightarrow e^{-x_N/L_p} \Rightarrow 0.$

$$Q = -AeL_p.\,\Delta P\left[0-1\right] = AeL_p\,\Delta P.$$

Differentiate wrt $V = \frac{\partial Q}{\partial V} = AeL_p \frac{\partial}{\partial V}(\Delta P)$. ——(1).

WRT, $I \cong I_{pn}(0) = Ae\frac{D_p}{L_p} \times \Delta P.$

Diff wrt V.

$$\frac{\partial I}{\partial V} = \frac{AeD_p}{L_p} \frac{\partial}{\partial V}(\Delta P).$$

$$\Rightarrow \frac{\partial}{\partial V}(\Delta P) = \frac{L_p}{AeD_p} \cdot \frac{\partial I}{\partial V} \quad —(2).$$

Sub (2) in (1).

$$\therefore \frac{\partial Q}{\partial V} = C_D = \cancel{A}\cancel{e}L_p \times \frac{L_p}{\cancel{A}\cancel{e}D_p} \cdot \frac{\partial I}{\partial V}$$

Scanned by CamScanner

$$C_D = \frac{L_p^2}{D_p} \times \frac{\partial I}{\partial V}$$

$$\boxed{C_D = \tau_p \times \frac{1}{r}}$$

$\because L_p = \sqrt{D_p \cdot \tau_p}$

$r = \frac{\partial V}{\partial I}$

$\tau_p = \frac{L_p^2}{D_p}$ = life time of holes. r = dynamic resistance.

$$C_D = \frac{\tau_p}{\frac{\eta V_T}{I}} = \boxed{\frac{\tau_p I}{\eta V_T} = C_D}$$

* $\boxed{C_D \propto \text{forward current } (I_F)}$

$C_D \propto e^{V/\eta V_T}$

i.e., C_D increases exponentially with voltage (forward voltage).

For PN Junction: $C_D = \frac{\tau_n}{r}$

NOTE:- For ordinary PN junction, $\boxed{C_D = \frac{\tau_p}{r} + \frac{\tau_n}{r}}$.

Diode Switching times:

→ Diode in forward bias ≡ ON switch

→ Diode in reverse bias ≡ OFF switch

Switching speed of a diode depends upon forward and reverse recovery times

Forward recovery time: It is the time taken by a diode to change from OFF state to ON state

Reverse recovery time: It is the time taken by a diode to change from ON to OFF state

For a diode $t_{rr} >> t_{fr}$.

t_{rr} = Reverse recovery time

t_{fr} = Forward recovery time

Scanned by CamScanner

(10)

→ Reverse recovery time is the sum of storage time and transition time.

Storage time (t_s): When diode is in ON condition, large amount of +ve charge is infected into N side in the form of holes and large amount of negative charge is injected into P side in the form of electrons

- When applied voltage changes to reverse bias, injected holes move back to P-side and injected electrons move back to n-side. During this reverse movement of carriers, recombinations occur and injected charge gradually reduces to zero
- The time taken by injected charge to become 0, is storage time

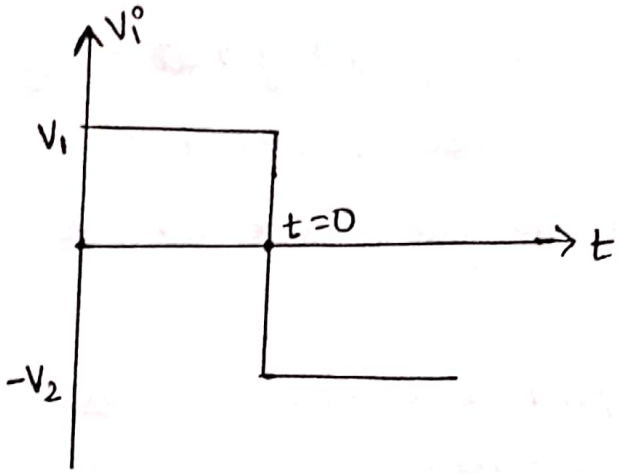
Transition time (t_t): When injected charge becomes zero, the transition capacitance of diode will start charging upto applied reverse voltage (capacitance voltage cannot change abruptly, it takes time to charge)

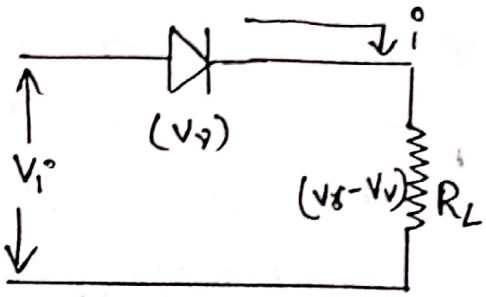
- The time taken by transition capacitance to charge upto applied reverse voltage is known as transition time

$$t_{rr} = t_s + t_t$$

i.e, Reverse recovery time is large due to two events taking place i.e, injected charge should be 0 & C_T should charge upto the R.B volt

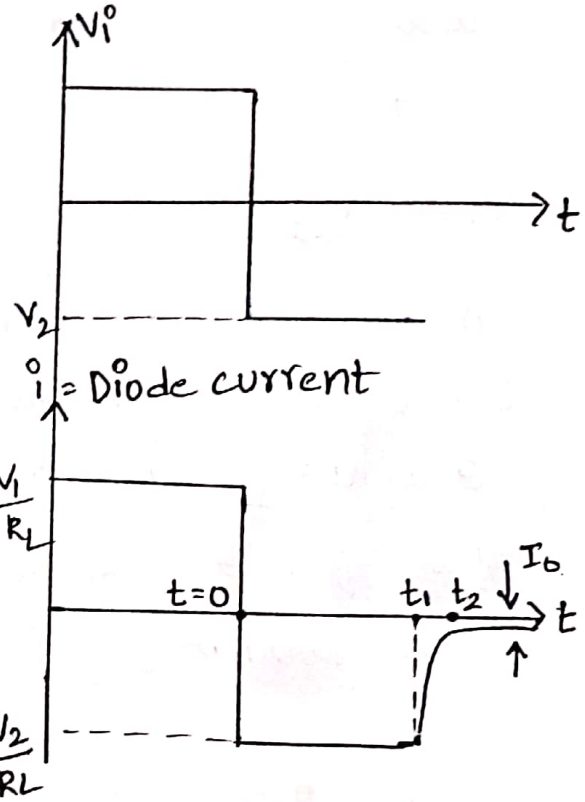
Scanned by CamScanner





For $t<0$: Diode is in forward bias (ON)

$$i = \frac{V_i - V_\gamma}{R_L} \simeq \frac{V_1}{R_L} \quad (\text{if } V_1 >> V_\gamma)$$



At $t=0$: V_i changes from $+V_1$ to $-V_2$ i.e from F.B to R.B

At $t=0$, current through the diode does not become 0, but current reverses its direction and a current equal to $\frac{V_2}{R_L}$ will flow through the diode from N side to P-side due to reverses its movement of injected carriers.

At $t=0$, when voltage changes abruptly (act as a S.C, and entire V_2 appears across R (diode acts as C)

This current flow continues till injected charge becomes 0 at $t=t_1$.

For $t>t_1$: The transition capacitance of diode starts charging & Hence voltage across diode keeps increasing and current through diode keeps decreasing (capacitive action)

Scanned by CamScanner

Transition capacitance gets fully charged at $t = t_2$ and diode current is I_0 (reverse current that flows when diode in OFF) Diode is fully recovered when current becomes I_0.

- To improve switching speed of a diode, reverse recovery time should, be reduced by decreasing storage time.

Rectifiers

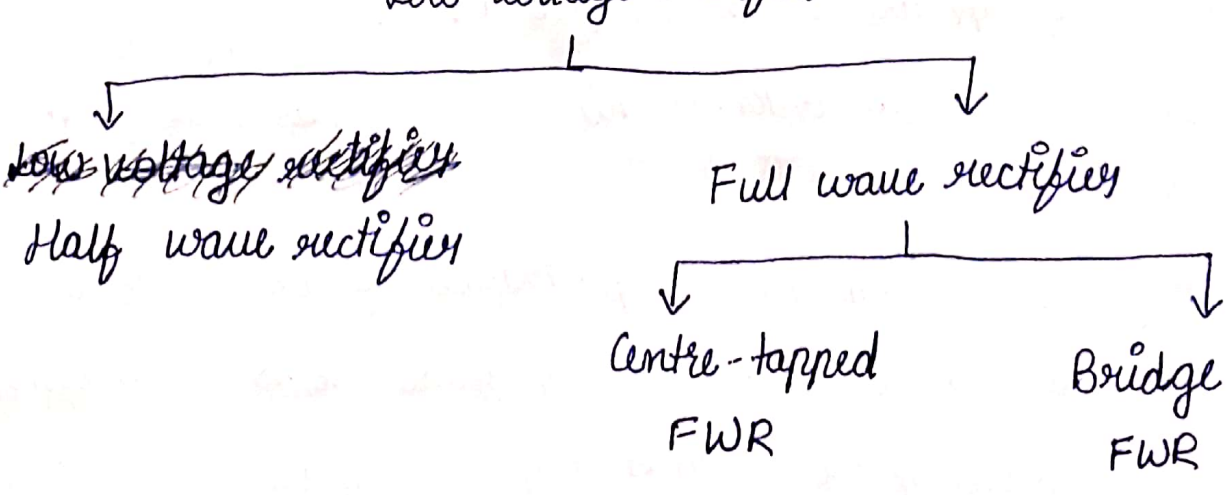
An electronic circuit which converts pure AC into pulsating DC (or) a circuit which converts bidirectional signal to unidirectional signal

It is of two types

i) Low voltage rectifier (produces low DC output voltage of few V to few 10's of volt)

ii) High voltage rectifier (produces DC output voltage of 100's of volt)

- Low voltage rectifier consists of normal diodes whereas high voltage rectifier consists of power diodes & SCR

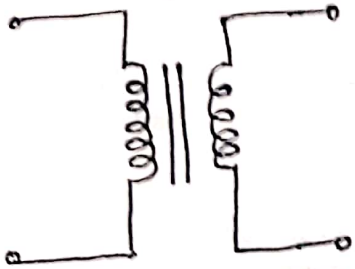


Scanned by CamScanner

(13) Step down transfer ⇒ to convert 220V AC to smaller AC or downsize AC voltages according to requirement before rectifying

- In low voltage rectifiers stepdown transformer is used to reduce the strength of AC voltage. (less no. of winding in secondary than primary)

$$\frac{V_1}{V_2} = \frac{N_1}{N_2}$$ Turns ratio

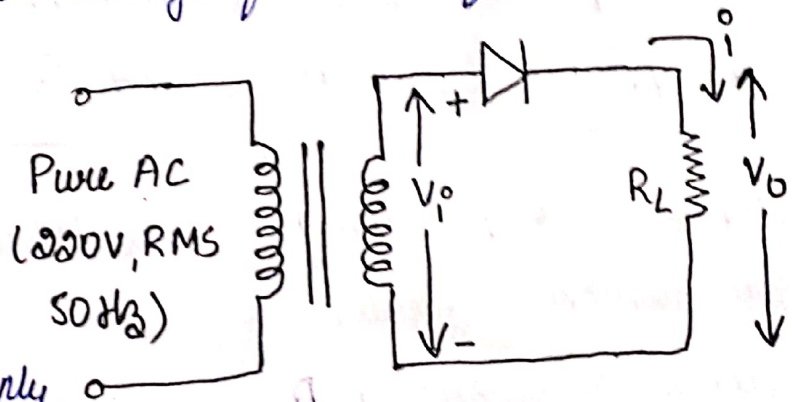


$N_1 : N_2$ $(N_1 > N_2)$

Ex: 220V $\xrightarrow{10:1}$ $\frac{220}{10}$ = 22V

- step down transformer is necessary to obtain low DC output voltage from rectifier

Half Wave rectifier



220V : line voltage

50Hz : line frequency or frequency of AC supply

V_i : Pure AC voltage having smaller RMS value

$V_i = V_m \sin \omega_0 t$ or $V_m \sin \alpha$ → mathematical representation of pure AC

V_m = peak value, $\frac{V_m}{\sqrt{2}}$ = RMS value, $2V_m$ = peak to peak value

$\omega_0 = 2\pi f_0$ = line frequency

$f_0 = 50Hz$, $\omega_0 = 2\pi \times 50 = 314$ rad/sec

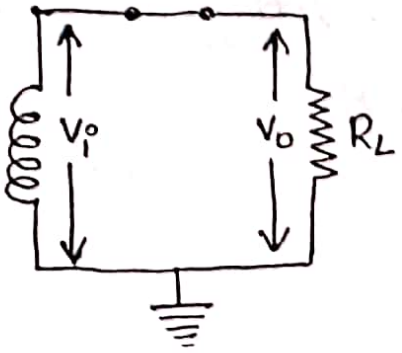
Scanned by CamScanner

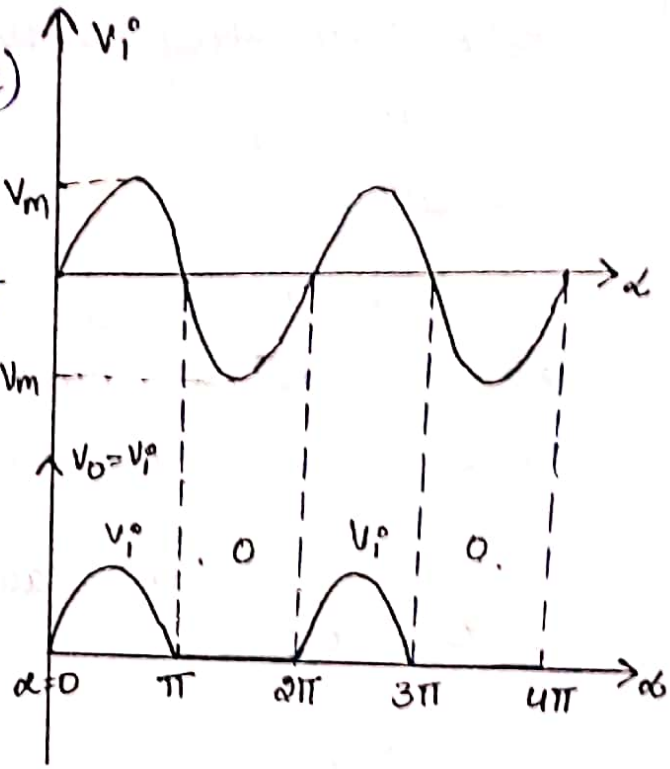
For $0 < \alpha < \pi$: (Diode in F.B → SC)

V_i = positive

∴ Diode operates in F.B equivalent to a short circuit

$V_o \cong V_i$



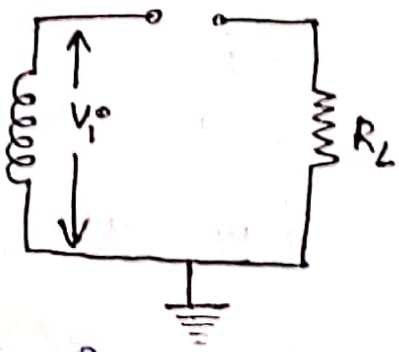


For $\pi < \alpha < 2\pi$:

V_i = Negative ⇒ input has negative cycle

∴ Diode operates in R.B equivalent to O.C

V_i appears fully across diode $V_o = 0$



- output is a pulsating DC waveform. It varies with time which indicates the presence of AC components. Hence, a pulsating DC signal has AC and DC component

Analysis of half-wave rectifier:

1) Instantaneous output current:

for $0 < \alpha < \pi$, R_F = Diode is F.B

R_F = Bulk resistance of internal resistance

Apply KVL in secondary loop.

$$-V_i + iR_F + iR_L = 0$$

$$i = \frac{V_i}{R_F + R_L} = \frac{V_m \sin\alpha}{R_F + R_L} = I_m \sin\alpha$$

where $I_m = \frac{V_m}{R_F + R_L}$

I_m = Peak O/P current

Scanned by CamScanner

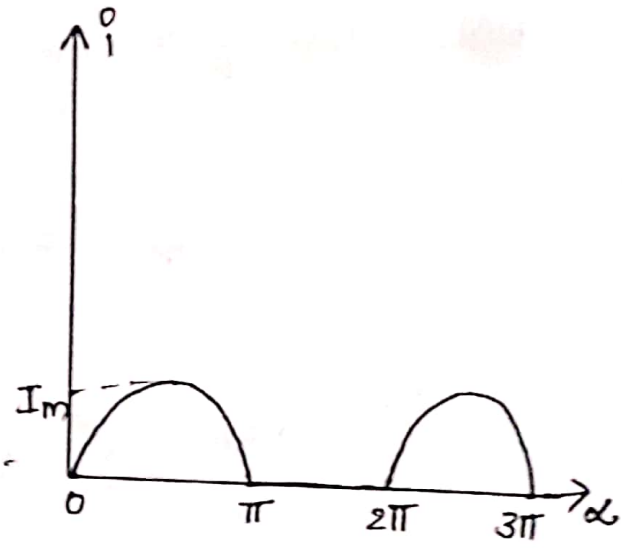
(15)

$\pi < \alpha < 2\pi$:

diode is in R.B

diode passes negligible current in reverse bias condition $\therefore i \cong 0$

$$\therefore \boxed{\begin{array}{ll} i = I_m \sin\alpha, & 0 < \alpha < \pi \\ 0, & \pi < \alpha < 2\pi \end{array}}$$



2) DC output current (I_{DC}):-

I_{DC} = Average value of the instantaneous current = $\frac{\text{Area}}{\text{Time Period}}$

$$I_{DC} = \frac{1}{2\pi}\int_0^{2\pi} i \cdot d\alpha = \frac{1}{2\pi} \times \int_0^{2\pi} I_m \sin\alpha = \frac{-I_m}{2\pi}\left[\cos\alpha\right]_0^{\pi} - 0\Big]_{\pi}^{2\pi}$$

$$I_{DC} = \frac{-I_m}{2\pi} - (1-1) = \frac{I_m}{\pi}, \quad \boxed{I_{DC} = \frac{I_m}{\pi}}$$

3) RMS output current (I_{RMS}):

$$I_{RMS} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} i^2 d\alpha} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} (I_m \sin\alpha)^2 \cdot 2\alpha}$$

$$= \sqrt{\frac{I_m^2}{2\pi}\int_0^{\pi} \sin^2\alpha \cdot 2\alpha} = \sqrt{\frac{I_m^2}{2\pi}\int_0^{\pi} \left(\frac{1-\cos 2\alpha}{2}\right) 2\alpha}$$

$$= \sqrt{\frac{I_m^2}{4\pi}\left[\alpha - \frac{\sin 2\alpha}{2}\right]_0^{\pi}} = \sqrt{\frac{I_m^2}{4\pi}\left[\pi - 0\right]}$$

$$= \sqrt{\frac{I_m^2}{4}} = \frac{I_m}{2} \qquad \boxed{I_{RMS} = \frac{I_m}{2}}$$

Scanned by CamScanner

(16) RMS value of the AC component (I'_{RMS}):

$i = AC + DC$

$i = I_{DC} + i' \Rightarrow \boxed{i' = i - I_{DC}}$

$$I'_{RMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i'^2 \, d\alpha}$$

$$I'_{RMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} (i - I_{DC})^2 \, d\alpha}$$

$$I'_{RMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} (i^2 + I_{DC}^2 - 2 \cdot i \cdot I_{DC}) \, d\alpha}$$

$$I'_{RMS} = \frac{1}{2\pi}\int_0^{2\pi} i^2 \cdot d\alpha + \frac{I_{DC}}{2\pi}\int_0^{2\pi} d\alpha - \frac{2I_{DC}}{2\pi}\int_0^{2\pi} i \, d\alpha$$

$$I'^2_{RMS} = I_{RMS} + I_{DC}^2 - 2I_{DC}^2$$

$$I'^2_{RMS} = I_{RMS} - I_{DC}^2 \qquad \boxed{I'_{RMS} = \sqrt{I_{RMS} - I_{DC}^2}}$$

5) Ripple factor:

It is defined as the amount of AC component present at the output of the rectifier

Mathematically, it is given as, $\gamma = \frac{\text{RMS value of AC components}}{\text{DC component}}$

$$\boxed{\gamma = \frac{I'_{RMS}}{I_{DC}}} \qquad \gamma = \frac{\sqrt{I_{RMS}^2 - I_{DC}^2}}{I_{DC}} = \sqrt{\frac{I_{RMS}^2 - I_{DC}^2}{I_{DC}^2}}$$

$$\boxed{\gamma = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - 1}} = \sqrt{\left(\frac{I_m/2}{I_m/\pi}\right)^2 - 1} = \sqrt{\frac{\pi^2}{4} - 1} \Rightarrow \boxed{\gamma = 1.21}$$

Scanned by CamScanner

(17) c) Input power (P_i):

It is average value of the product of instantneous voltage across the secondary winding and instantneous current through the secondary winding

Mathematically P_i = Avg value $(V_i \times i)$

$$P_i = \frac{1}{2\pi} \int_0^{2\pi} (V_i \times i)\, d\alpha$$

$$P_i = \frac{1}{2\pi} \int_0^{2\pi} i^2 (R_F + R_L)\, d\alpha$$

$$P_i = (R_F + R_L) \cdot \frac{1}{2\pi} \int_0^{2\pi} i^2 \cdot d\alpha$$

$$\boxed{P_i = I_{RMS}^2 (R_F + R_L)}$$

f) Efficiency (η): $\eta = \frac{P_{DC}}{P_i} = \frac{I_{DC}^2 R_L}{I_{RMS}^2 (R_F + R_L)}$

$$= \frac{\left(\frac{I_m}{\pi}\right)^2 \cdot R_L}{\left(\frac{I_m^2}{2}\right)(R_F + R_L)} = \frac{4}{\pi^2} \cdot \frac{R_L}{R_F + R_L} \times 100$$

$$\boxed{\%\eta = 40.5 \cdot \frac{R_L}{R_F + R_L} \%}$$

$R_F \approx 0$ $\quad \boxed{\eta = 40.5\ \%}$

Scanned by CamScanner

8) Average diode voltage ($V_{D,avg}$)

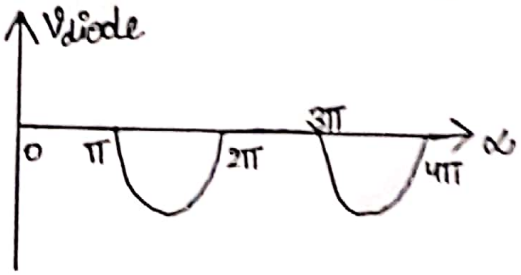
Let V_{diode} is the instantneous diode voltage

$0 < \alpha < \pi$: diode is in F.B $\quad V_{diode} = i.R_F \cong 0$

$\pi < \alpha < 2\pi$: diode is in R.B $\quad V_{diode} = V_i = V_m \sin\alpha$

$V_{diode} = 0 \quad 0 < \alpha < \pi$

$= V_m \sin\alpha \quad \pi < \alpha < 2\pi$ → Instantneous diode voltage



$$V_{D,avg} = \frac{1}{2\pi}\int_0^{2\pi} V_{diode}\cdot d\alpha$$

$$= \frac{1}{2\pi}\int_0^{\pi} 0\cdot d\alpha + \int_0^{2\pi} 1\cdot \sin\alpha\cdot d\alpha$$

$$= \frac{1}{2\pi}\int_0^{2\pi} V_m \sin\alpha\cdot d\alpha = \frac{V_m}{2\pi}\cdot[\cos\alpha]_{\pi}^{2\pi}$$

$$= \frac{-V_m}{2\pi}[1+1] = \frac{-V_m}{\pi}$$

$$\boxed{V_{D,avg} = \frac{-V_m}{\pi}}$$

~~9) Ripple factor:~~

9) Peak inverse voltage (PIV):

It is defined as the maximum voltage which appears across the diode in non-conducting state of a rectifier.

$$PIV = |V_{diode}|_{max}$$

$$= |V_m \sin\alpha|_{max}$$

$$\boxed{PIV = V_m}$$

Scanned by CamScanner

10) Transformer utilisation factor (TUF)

$$TUF = \frac{\text{DC power delivered to load}}{\text{AC rating of transformer secondary}}$$

$$TUF = \frac{P_{dc}}{P_{ac,\,rated}}$$

$$P_{ac,\,rated} = V \times I = \frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}}$$

$$= \frac{I_{dc}^2 R_L}{\frac{V_m I_m}{2\sqrt{2}}} = \frac{\frac{I_m^2}{\pi^2} \cdot R_L}{\frac{V_m \cdot I_m}{2\sqrt{2}}}$$

$$= \frac{\frac{V_m^2}{\pi^2} \cdot \frac{1}{R_L}}{\frac{V_m}{\sqrt{2}} \times \frac{V_m}{2R_L}} = \frac{2\sqrt{2}}{\pi^2} \Rightarrow \boxed{0.287 = TUF}$$

11) Form factor (F)

It is the measure of smoothness in wave form. Smaller 'F' indicates greater smoothness (or) less variation in output wave form

$$F = \frac{I_{rms}}{I_{DC}} = \frac{I_m/2}{I_m/\pi} = \frac{\pi}{2} = 1.57 \qquad \boxed{F = 1.57}$$

relation between ripple factor and form factor

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{DC}}\right)^2 - 1} \Rightarrow \boxed{\gamma = \sqrt{F^2 - 1}}$$

Scanned by CamScanner

12) Regulation factor

It is a measure of the change in the DC output voltage due to change in the load current.

Mathematically, $R = \frac{V_{DCNL} - V_{DCFL}}{V_{DCFL}} \times 100$

V_{DCNL} = No load DC output voltage

$V_{DCNL} = V_{DC} \mid \begin{matrix} C = 0 \\ R_L = \infty \end{matrix}$, $\boxed{V_{DCNL} = \frac{V_m}{\pi}}$

V_{DCFL} = full load DC output voltage

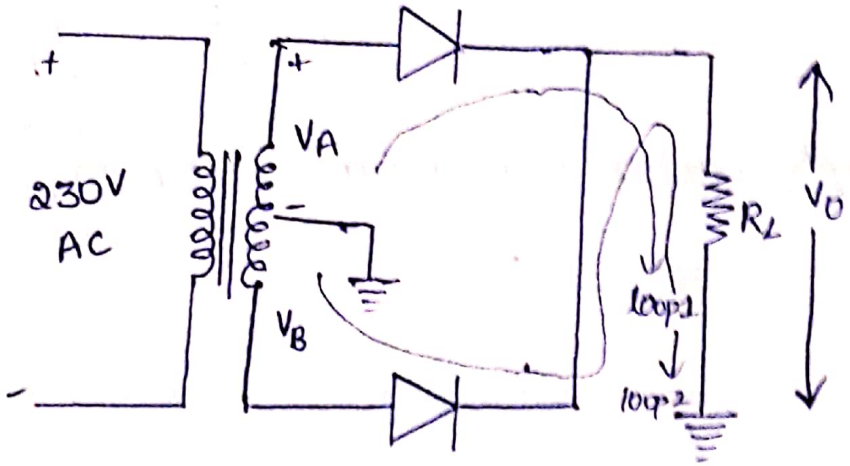
$V_{DCFL} = V_{DC} \mid i \neq 0$ $\boxed{V_{DCFL} = I_{DC} \times R_L}$

$\boxed{V_{DCFL} = \frac{V_m}{\pi} - I_{DC} \cdot R}$ $R = R_F + R_S$

$\boxed{R_{eq} = \frac{R}{R_L} \times 100\ \%}$

Full wave Rectifier

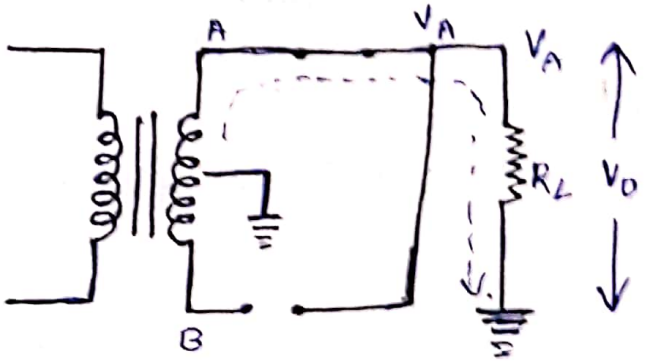
In this method we use 2 diodes i.e, full wave rectifier is the combination of two half wave rectifiers



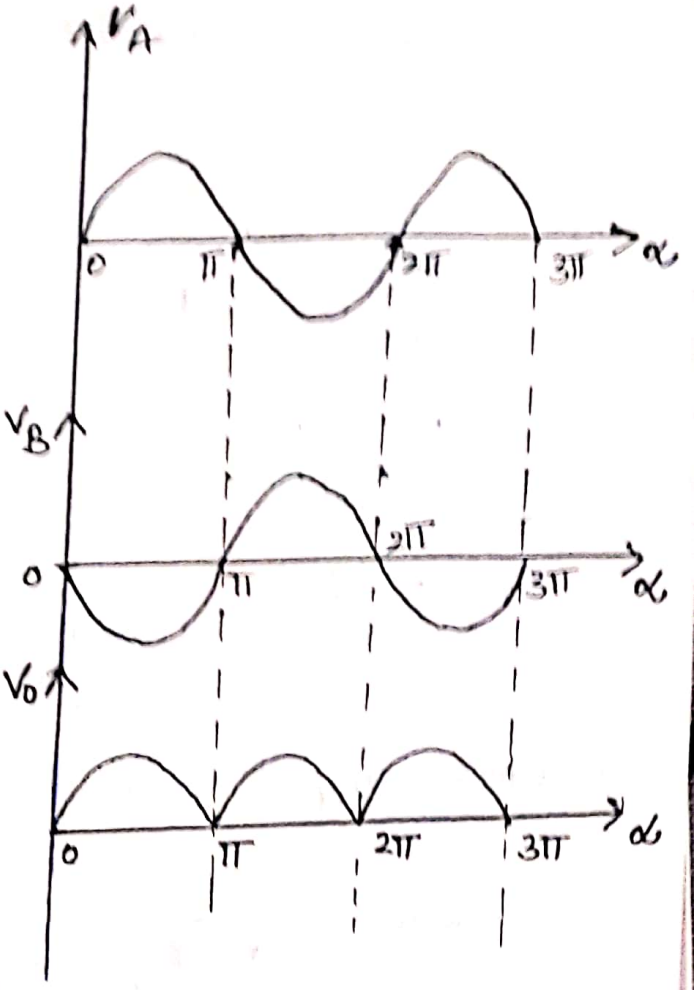
Scanned by CamScanner

case-1 : $0 < \alpha < \pi$

D_1 - ON D_2 - OFF

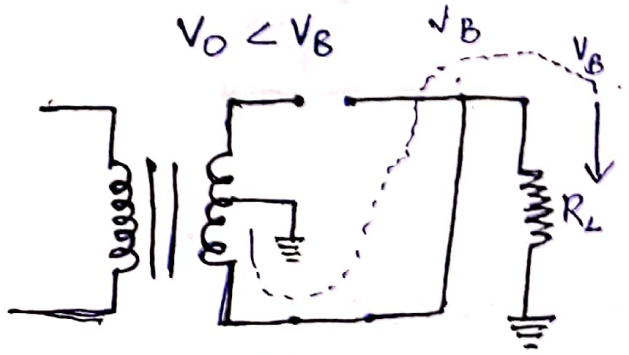


$V_o = V_A$



case-2 : $\pi < \alpha < 2\pi$

$V_o < V_B$



Analysis

1) Instantneous output current (or) load current (i)

$$i = i_m \sin\alpha \;, \quad 0 < \alpha < \pi$$

$$= -i_m \sin\alpha \;, \quad \pi < \alpha < 2\pi$$

for $0 < \alpha < \pi$, $-V_A + iR_F + iR_L = 0$

$$i = \frac{V_A}{R_F + R_L} = \frac{V_m \sin\alpha}{R_F + R_L} \Rightarrow \boxed{i = I_m \sin\alpha}$$

for $\pi < \alpha < 2\pi$, $-V_B + iR_F + iR_L = 0$

$$i = \frac{V_B}{R_F + R_L} = \frac{-V_m \sin\alpha}{R_F + R_L} \Rightarrow \boxed{i = -I_m \sin\alpha}$$

Scanned by CamScanner

2) DC output current (I_{DC})

I_{DC} = average value of instantaneous current (i)

$$I_{DC} = \frac{1}{2\pi}\int_{i}^{2\pi} i \cdot d\alpha = \frac{1}{2\pi}\left[\int_{i}^{\pi} i_m \sin\alpha \, d\alpha - \int_{\pi}^{2\pi} i_m \sin\alpha \, d\alpha\right]$$

$$= \frac{i_m}{2\pi}\left[(-\cos\alpha)_0^{\pi} + (\cos\alpha)_{\pi}^{2\pi}\right] = \frac{i_m}{2\pi}\left[(1+1)+(1+1)\right]$$

$$= \frac{4 i_m}{2\pi} = \frac{2 i_m}{\pi}$$

$$\boxed{I_{DC} = \frac{2I_m}{\pi}}$$

3) RMS output current (I_{RMS})

$$I_{RMS} = \sqrt{\frac{1}{2\pi}\int_{0}^{2\pi} i^2 \cdot d\alpha} \Rightarrow \boxed{I_{RMS} = \frac{I_m}{\sqrt{2}}}$$

4) RMS value of AC component (I'_{RMS})

$$\boxed{I'_{RMS} = \sqrt{I_{RMS}^2 - I_{DC}^2}}$$

5) Ripple factor (γ)

$$\gamma = \frac{I'_{RMS}}{I_{DC}} = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - 1} = \sqrt{\frac{(I_m/\sqrt{2})^2}{(2I_m/\pi)^2} - 1}$$

$$= \sqrt{\frac{\frac{I_m^2}{2}}{\frac{4I_m^2}{\pi^2}} - 1} = \sqrt{\frac{\pi^2}{8} - 1} = 0.483$$

$$\boxed{\gamma = 0.483}$$

Scanned by CamScanner

6) Input power (P_i)

$$P_i = I_{rms}^2 (R_F + R_L)$$

7) Efficiency (η)

$$\eta = \frac{P_{DC}}{P_i} \times 100 = \frac{I_{DC}^2 \cdot R_L}{I_{RMS}^2 (R_F + R_L)}$$

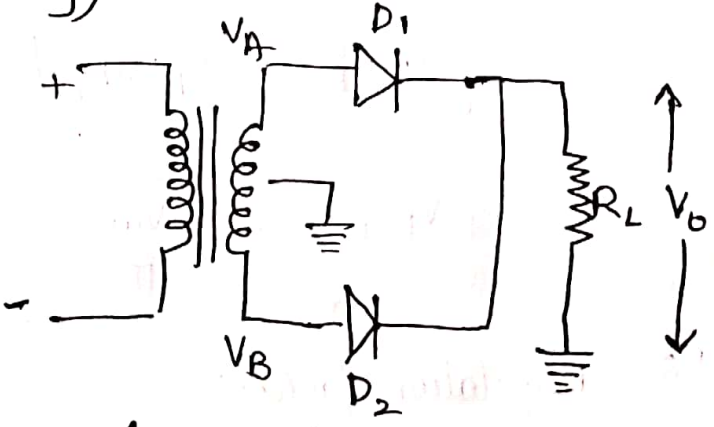
$$\eta = \frac{\frac{4I_m^2}{\pi^2} \cdot R_L}{\frac{I_m^2}{2}(R_F + R_L)} \times 100 = \frac{8}{\pi^2} \times 100 \cdot \frac{R_L}{R_F + R_L}$$

$$\eta = 81 \frac{R_L}{R_F + R_L}$$

$R_F \approx 0$

$$\eta = 81\%$$

8) Average diode Voltage ($V_{d,avg}$)



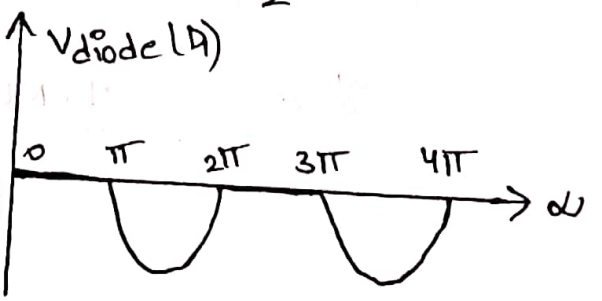
For $0 < \alpha < \pi$

$V_{diode} = 0$

for $\pi < \alpha < 2\pi$ $V_A - V_B$

$= V_m \sin\alpha - (-V_m \sin\alpha)$

$= 2V_m \sin\alpha$



$D_1 \rightarrow V_{diode} = 0 \Rightarrow 0 < \alpha < \pi$

$2V_m \sin\alpha, \Rightarrow \pi < \alpha < 2\pi$

$D_2 \rightarrow V_{diode} = -2V_m \sin\alpha \quad 0 < \alpha < \pi$

$= 0 \quad \pi < \alpha < 2\pi$

$$V_{d,avg} = \frac{1}{2\pi} \int_0^{2\pi} V_{diode} \cdot d\omega$$

$$V_{d,avg} = -\frac{2V_m}{\pi}$$

Scanned by CamScanner

9) Peak Inverse voltage (PIV)

$$PIV = |V_{diode}| = |\sqrt{2}V_m \sin\alpha|_{max} = \sqrt{2}V_m$$

$$\boxed{PIV = \sqrt{2}V_m}$$

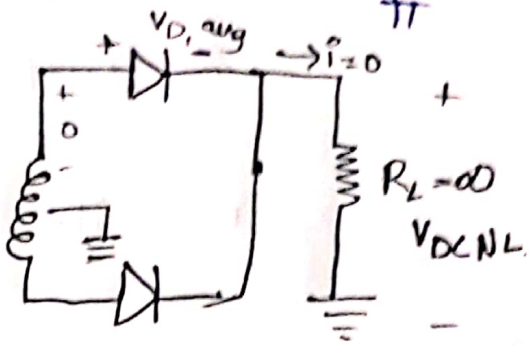
10) No load DC O/P voltage (V_{DCNL}):

$$V_{DCNL} = V_{DC} \,|\, i=0 \text{ or } R_L = \infty$$

$$0 + V_{D,avg} + V_{DCNL} = 0$$

$$V_{DCNL} = -V_{D,avg} = \frac{\sqrt{2}V_m}{\pi}$$

$$\boxed{V_{DCNL} = \frac{\sqrt{2}V_m}{\pi}}$$



11) Full load DC O/P voltage (V_{DCFL})

$$V_{DCFL} = V_{DC} \,|\, i \neq 0.$$

$$\boxed{V_{DCFL} = I_{DC} \cdot R_L}$$

$$\boxed{V_{DCFL} = \frac{\sqrt{2}V_m}{\pi} - I_{DC} \cdot R}$$

$$R = R_F + \frac{R_S}{2}$$

12) Regulation factor:

$$reg\,\% = \frac{V_{DCNL} - V_{DCFL}}{V_{DCFL}} \times 100$$

$$\boxed{\%\ regulation = \frac{R}{R_L} \times 100\,\%}$$

$$R = R_F + \frac{P_{SW}}{Q}$$

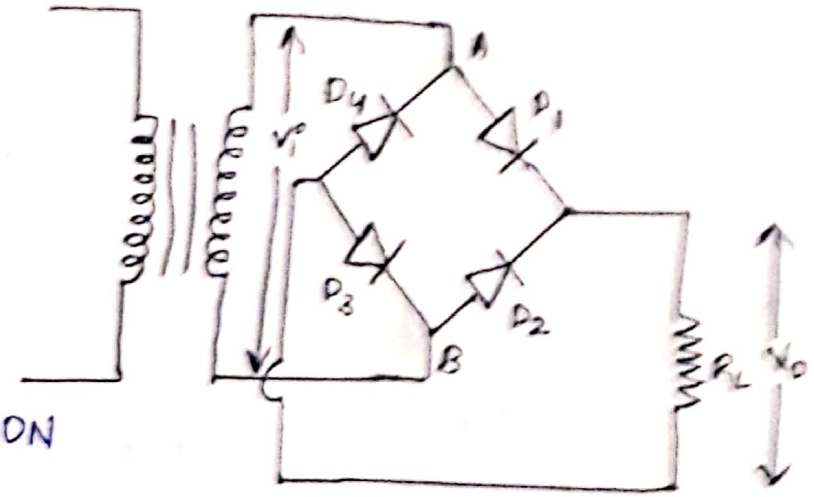
Scanned by CamScanner

13) Form factor (F).

$$F = \frac{I_{RMS}}{I_{DC}} = \frac{I_m/\sqrt{2}}{2I_m/\pi} = \frac{\pi}{2\sqrt{2}} = 1.11$$

$$\boxed{F = 1.11}$$

Bridge Rectifier



$V_i = V_m \sin\alpha$

for $0 < \alpha < \pi$

V_i is +ve, D_1, D_3 – F.B, ON

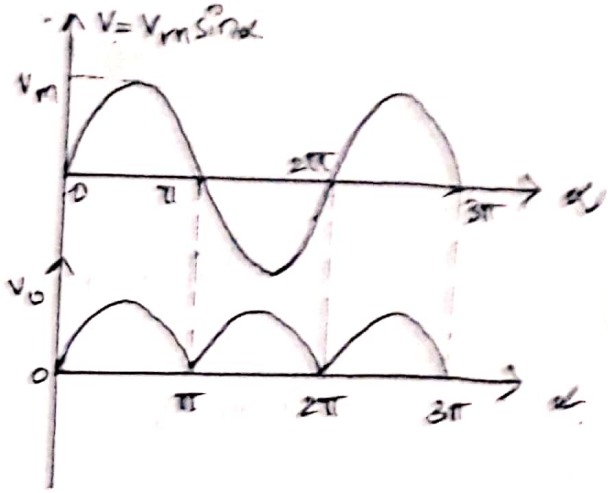
D_2, D_4 = R.B.

$V_o = V_i$

for $\pi < \alpha < 2\pi$

V_i is –ve, D_2, D_4 = F.B, ON.

$V_o = V_i$



Analysis

1) Instantaneous output current (i)

$$i = I_m \sin\alpha, \quad 0 < \alpha < \pi$$
$$= -I_m \sin\alpha, \quad \pi < \alpha < 2\pi$$

where $I_m = \frac{V_m}{2R_F + R_L}$

2) I_{DC}

$$I_{DC} = \frac{2I_m}{\pi}$$

3) I_{RMS}

$$I_{RMS} = \frac{I_m}{\sqrt{2}}$$

Scanned by CamScanner

4) I'_{RMS}

$$I'_{RMS} = \sqrt{I_{RMS}^2 - I_{DC}^2}$$

5) ripple factor

$$\gamma = 0.483$$

6) Input power

$$P_i = I_{RMS}^2 (2R_F + R_L)$$

7) Efficiency

$$\%\,\eta = 81 \times \frac{R_L}{2R_F + R_L} \%$$

8) Average diode voltage

consider D_1, $V_{diode} = 0$, $0 < \alpha < \pi$

$= V_m \sin\alpha$, $\pi < \alpha < 2\pi$

$$V_{D,avg} = \frac{-V_m}{\pi}$$

9) PIV

$|V_{diode}|_{max}$ in R.B, $PIV = |V_m \sin\alpha|_{max}$

$$PIV = V_m$$

10) V_{DCNL}

$$V_{DCNL} = \frac{2V_m}{\pi}$$

11) V_{DCFL}

$$V_{DCFL} = I_{DC} \cdot R_L$$

$$V_{DCFL} = \frac{2V_m}{\pi} - I_{DC} \cdot R$$

12) Regulation factor

$$\%\ reg = \frac{R}{R_L} \times 100\%$$

13) Form factor

$$F = 1.11$$

Scanned by CamScanner

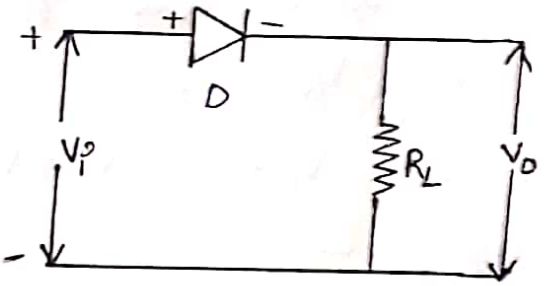
(27) # Clipper circuits

The circuits which are used to clip off unwanted portion of the waveform, without distorting the remaining part of the waveform are called clipper circuits or clippers when the diode is connected in series with the load, such circuit is called series clipper. when the diode is connected in a branch which is parallel to the load, it is called Parallel clipper

Series clippers

It is of two types

i) Series Negative clipper circuit



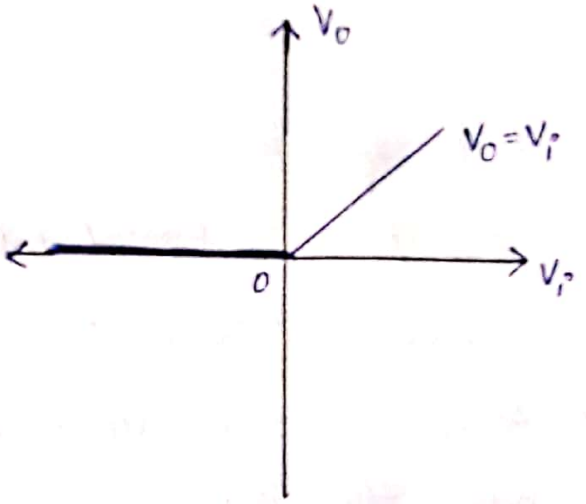
For a positive half cycle, the diode D is forward biased, Hence the voltage waveform across R_L looks like a +ve half cycle input voltage. while for negative half cycle, diode D is reverse biased and hence will not conduct at all. Hence there will not be any voltage available across resistance R_L. Hence the -ve half cycle of input voltage gets clipped off. As it clips off negative half cycle of the input is called series negative clipper

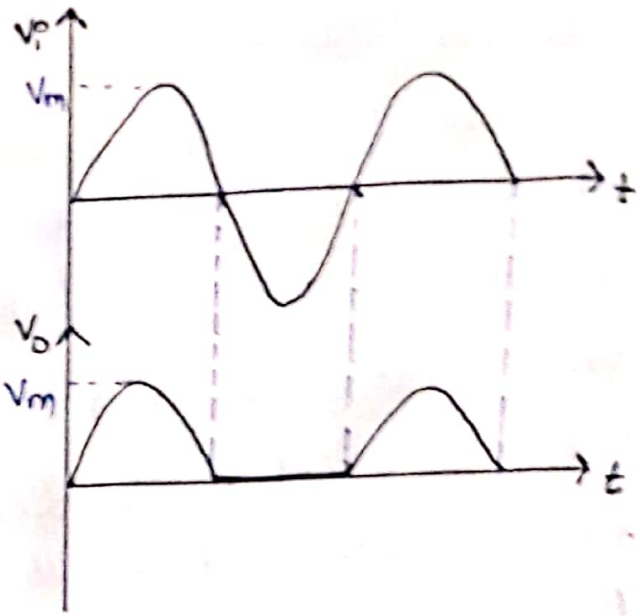
Case-1 : when the diode is ideal

$V_P = V_i$, $V_N = 0$

i) $V_P > V_N$, $V_i > 0$, $V_o = V_i$ ii) $V_P < V_N$, $V_i < 0$, $V_o = 0$.

Scanned by CamScanner

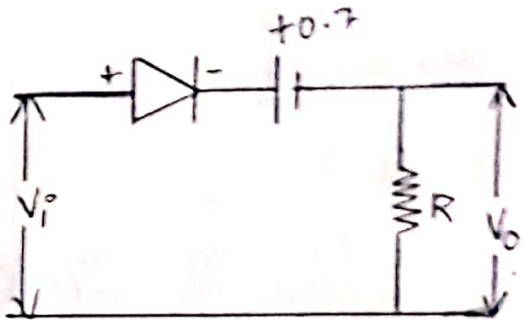




Tranfer characteristics with ideal diode

Case-II: considering V_r

Effect of cut-in voltage of diode

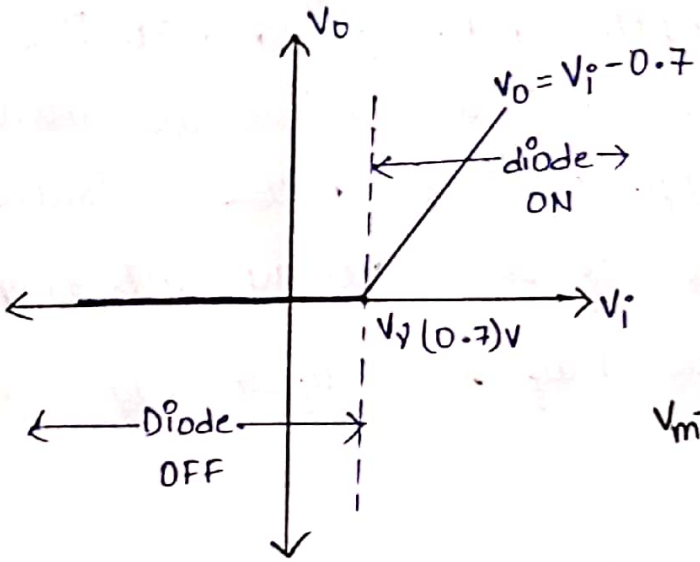


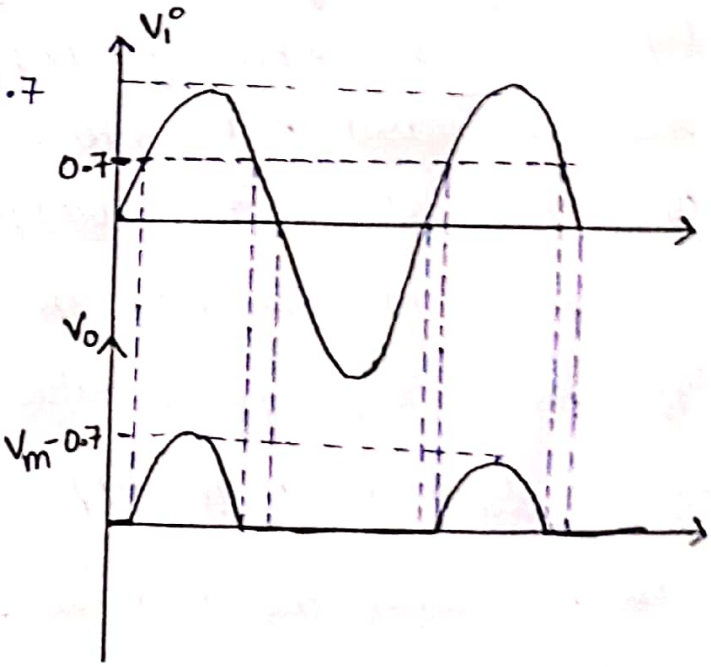
$V_P = V_i$, $V_N = 0.7$

i) $V_P > V_N$, $V_i > 0.7$, $V_o = V_i - 0.7V$

Diode is ON

ii) $V_P < V_N$, $V_i < 0.7$, $V_o = 0$ – Diode is OFF





Scanned by CamScanner

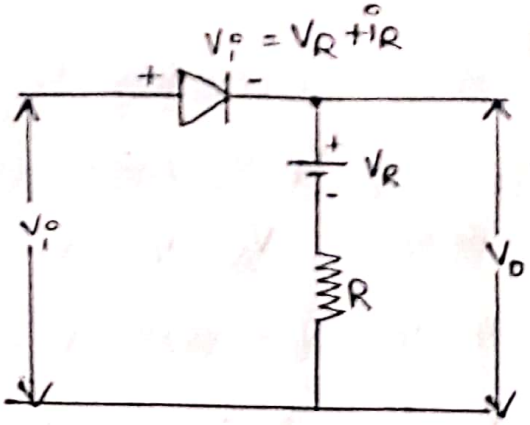
Case-III: Considering V_R

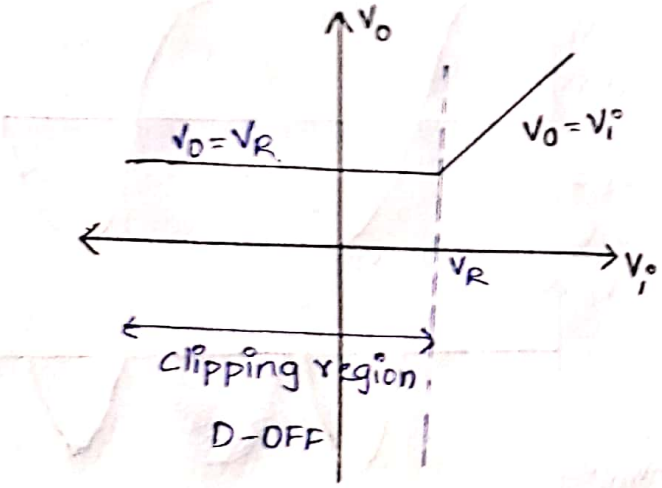
clipping above V_R below V_R

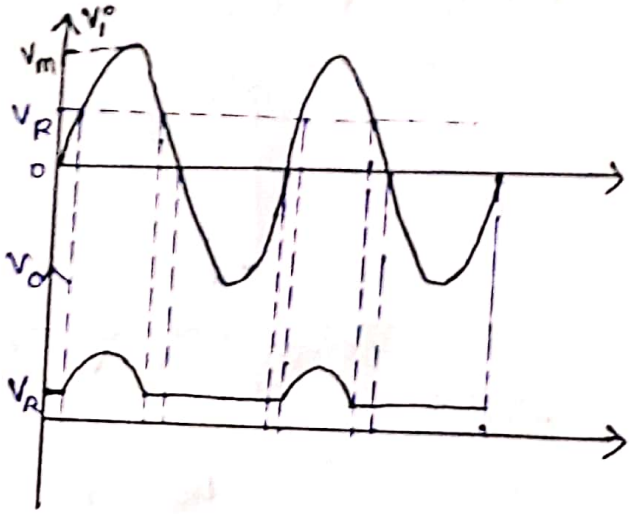
$V_P = V_i$, $V_N = V_R$

i) $V_P > V_N$, $V_i > V_R$, $V_o = V_i$ → Diode ON

ii) $V_P < V_N$, $V_i < V_R$, $V_o = V_R$ → Diode OFF







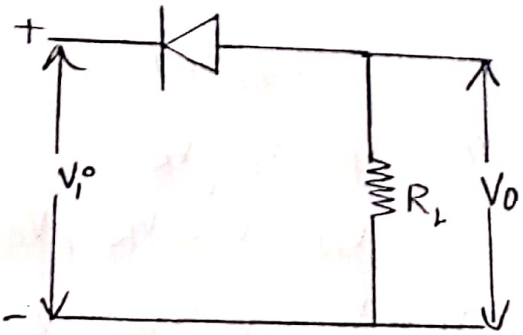
ii) Series Positive clipper circuit

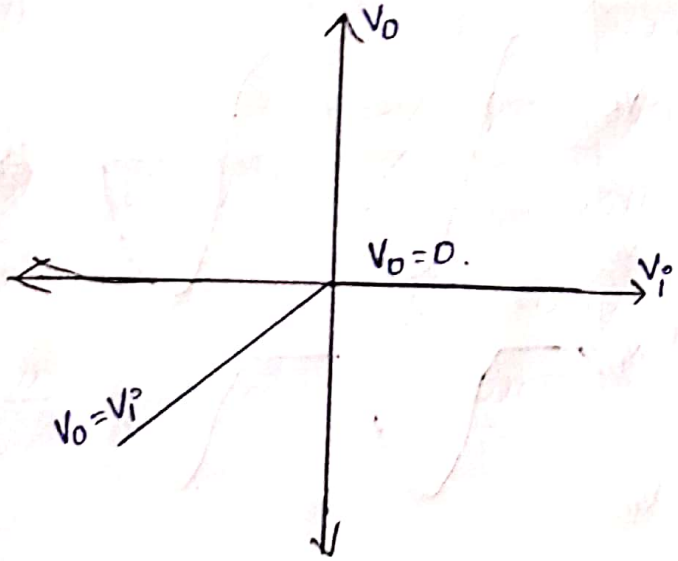
Case-1: Considering the diode is ideal

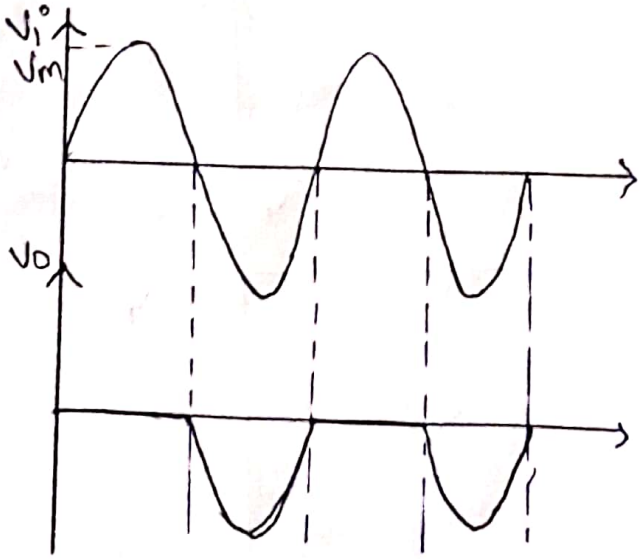
$V_N = V_i$, $V_P = 0$

i) $V_P > V_N$, $V_i < 0$, $V_o = V_i$ → Diode-ON

ii) $V_P < V_N$, $V_i > 0$, $V_o = 0$ → Diode-OFF



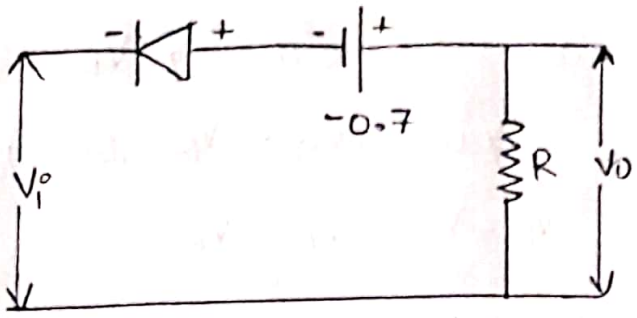




Scanned by CamScanner

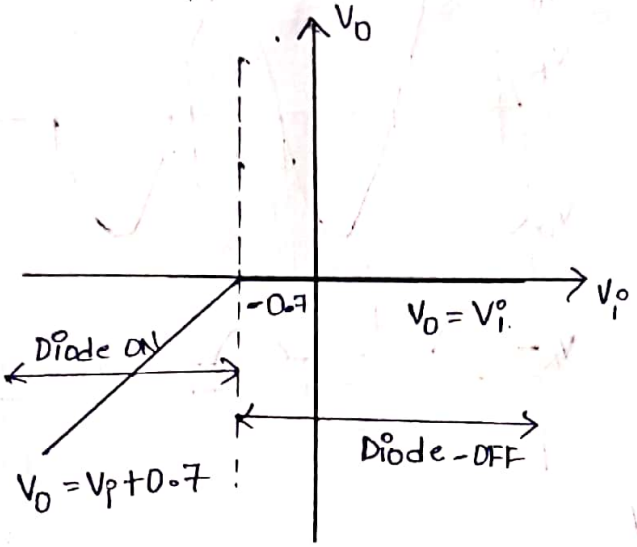
Case-II : Considering V_γ

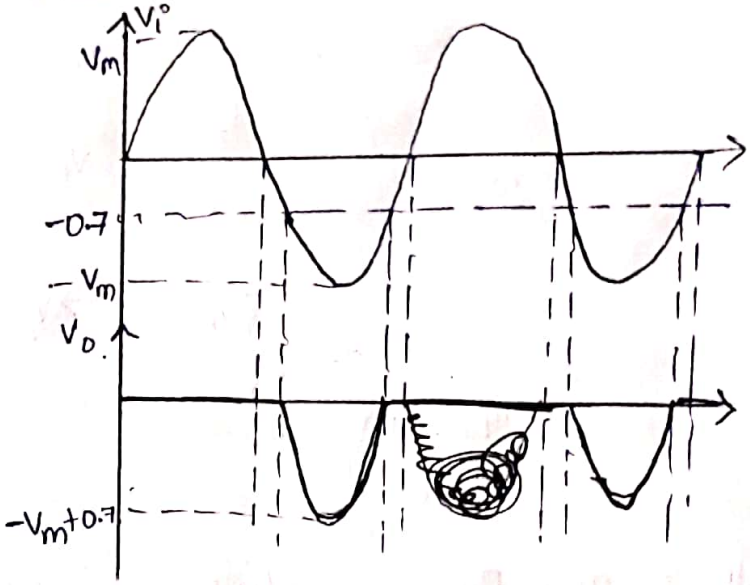
Effect of V_γ on positive clipper circuit $V_N = V_i^\circ$, $V_P = -0.7$



i) $V_P > V_N$, $V_i^\circ < -0.7$, $V_O = V_i^\circ + 0.7$ - Diode ON

ii) $V_P < V_N$, $V_i^\circ > -0.7$, $V_O = 0$ - Diode OFF



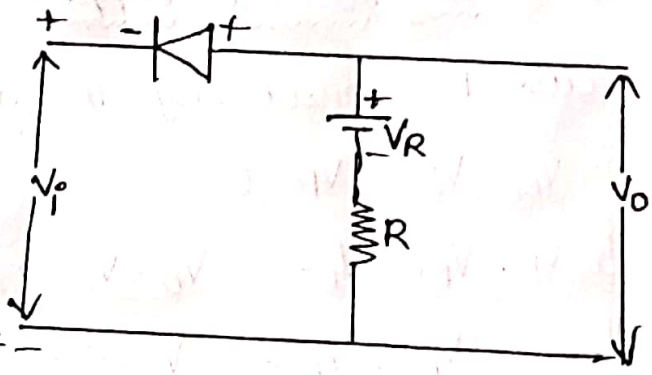


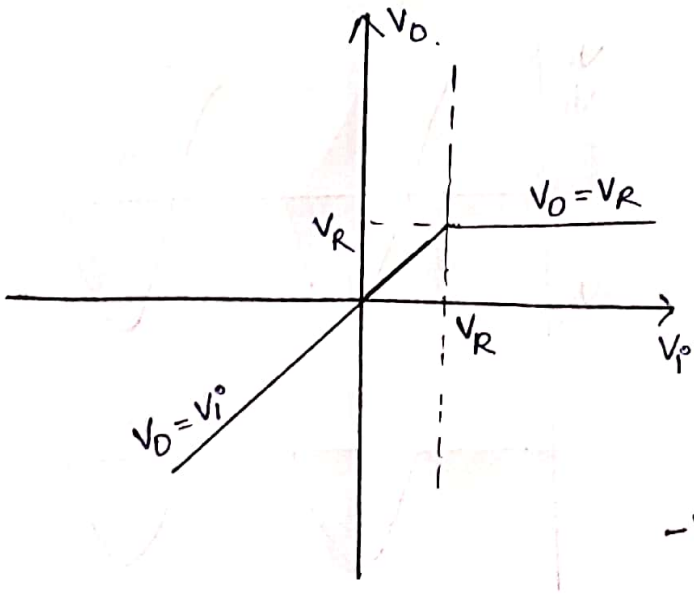
Case-III : Clipping above V_R

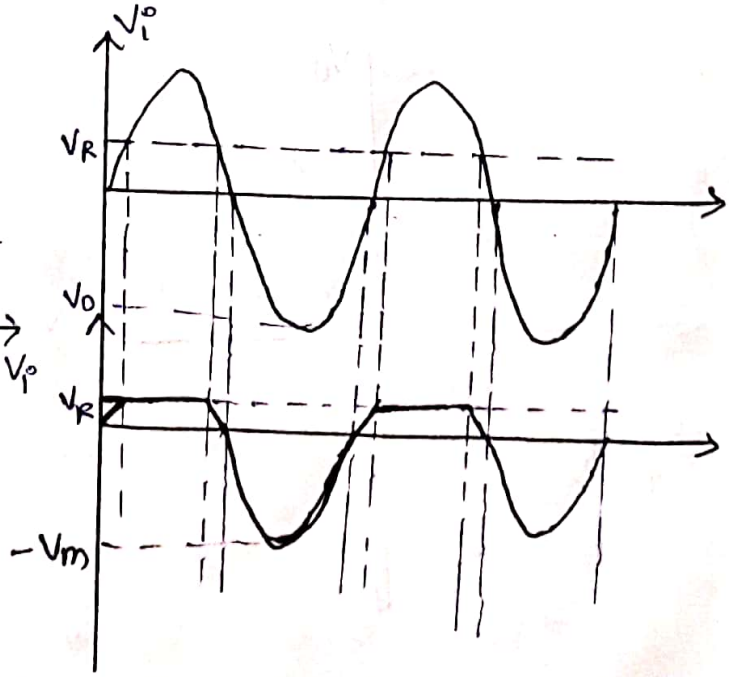
$V_N = V_i^\circ$, $V_P = V_R$

i) $V_P > V_N$, $V_i^\circ < V_R$, $V_O = V_i^\circ$ - Diode ON

ii) $V_P < V_N$, $V_i^\circ > V_R$, $V_O = V_R$ - Diode OFF







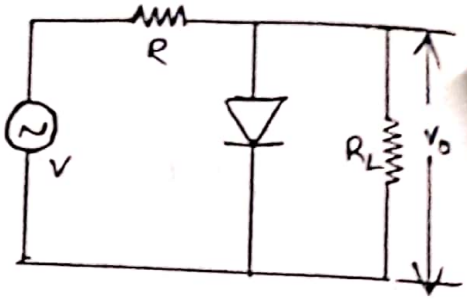
Scanned by CamScanner

(31)

Parallel clippers

In a parallel clipper circuit, the diode is connected across the load terminals. It can be used to clip the positive or negative part of the input signal, as per the requirement

1) Basic parallel clipper with positive clipping



Assume the diode is ideal

acts as S.C when forward biased

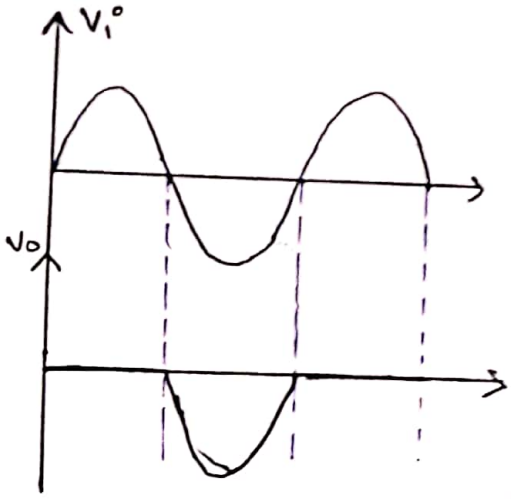
case-1 : $V_P > V_N$, $V_i > 0$ Diode-ON

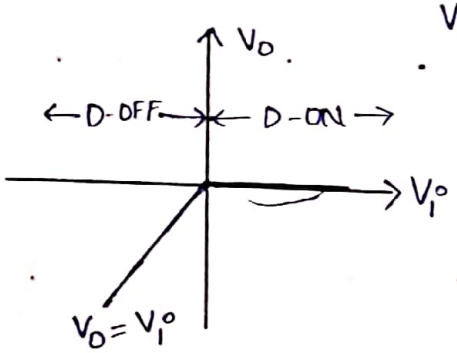
$V_o = 0$.

case-11 : $V_P < V_N$, $V_i < 0$ Diode off

$V_o = \frac{V_i \times R_L}{R}$ iff $R << R_L$

$V_o = V_i$





2) Effect of cut-in voltage with positive clipping

$V_P = V_i$, $V_N = 0.7$

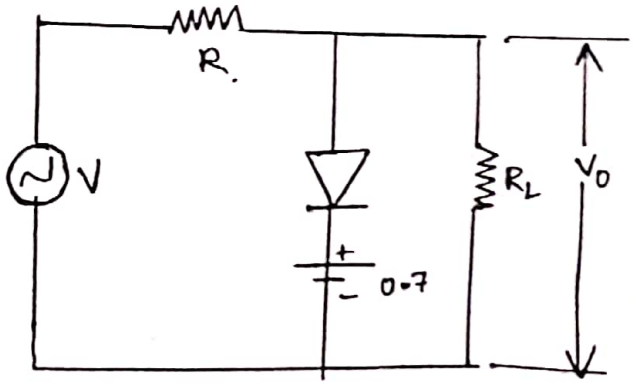
case-1 : $V_P > V_N$, $V_i > 0.7$

D-ON , $V_o = 0.7$

Case-11 : $V_P < V_N$, $V_i < 0.7$

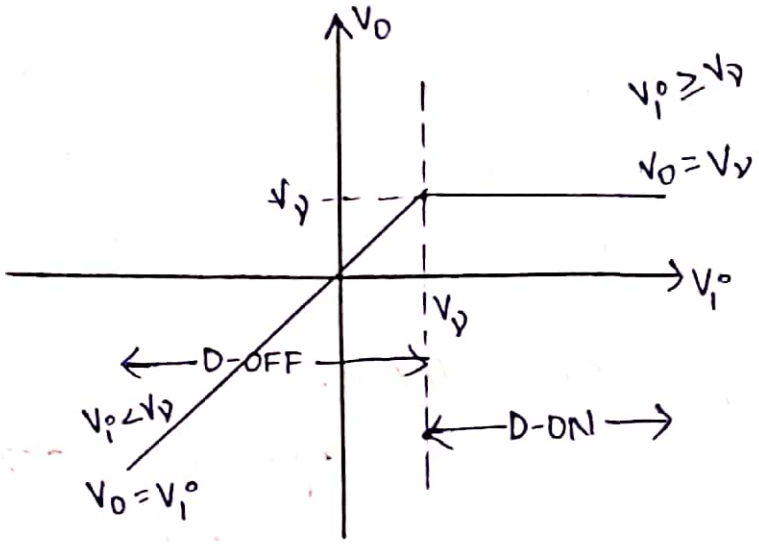
D-OFF $V_o = V_i \times \frac{R_L}{R}$

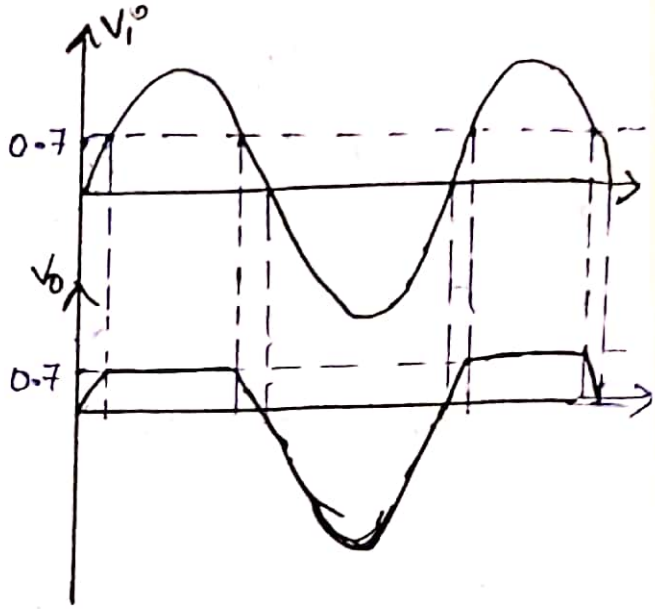
$R << R_L$ $V_o = V_i$



Scanned by CamScanner

(32)





3) Positive parallel clipper with reference voltage V_R

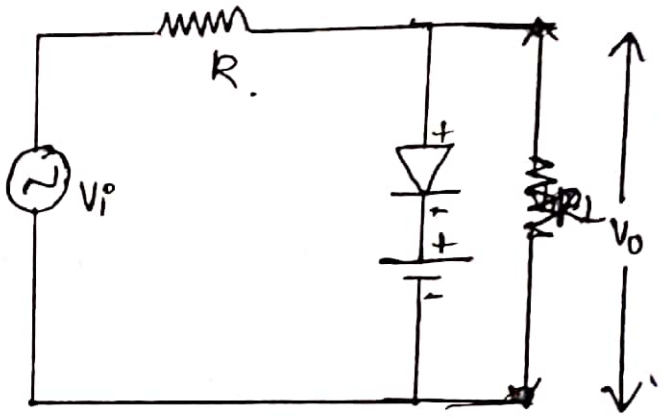
$V_P = V_i^\circ$, $V_N = V_R$

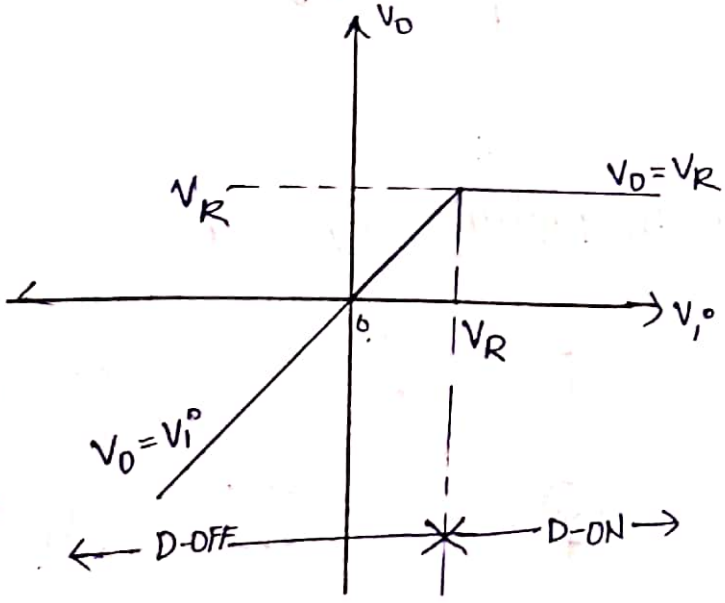
Case-I : $V_P > V_N$, diode-ON

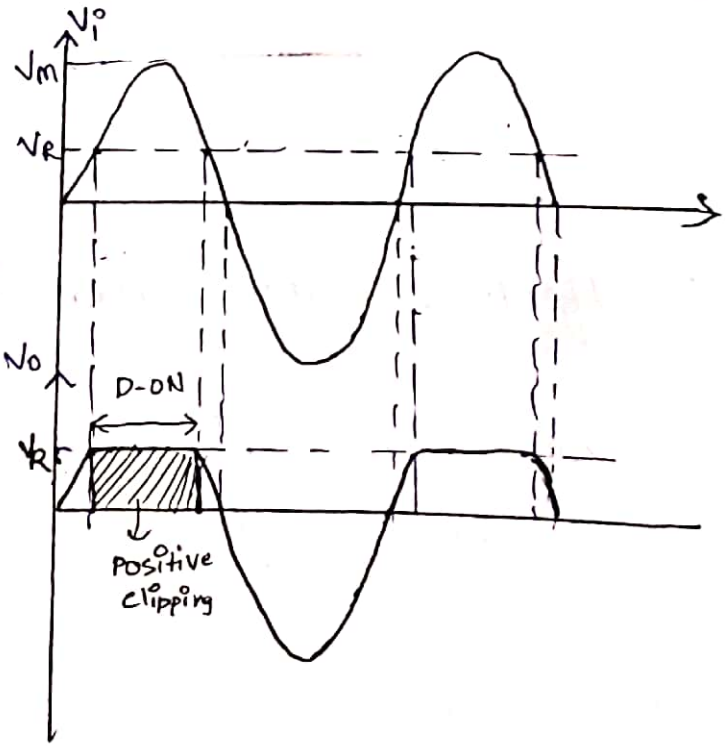
$V_i^\circ > V_R$, $V_0 = V_R$

Case-II : $V_P < V_N$, $V_i^\circ < V_R$

$V_0 = V_i^\circ$ — diode-OFF







Scanned by CamScanner

4) Basic Parallel clipper with negative clipping

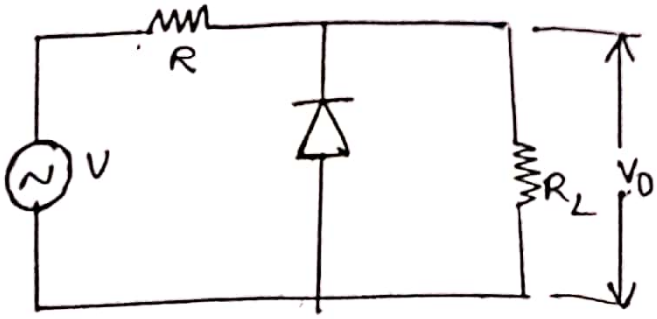
$V_P = 0$, $V_N = V_i$

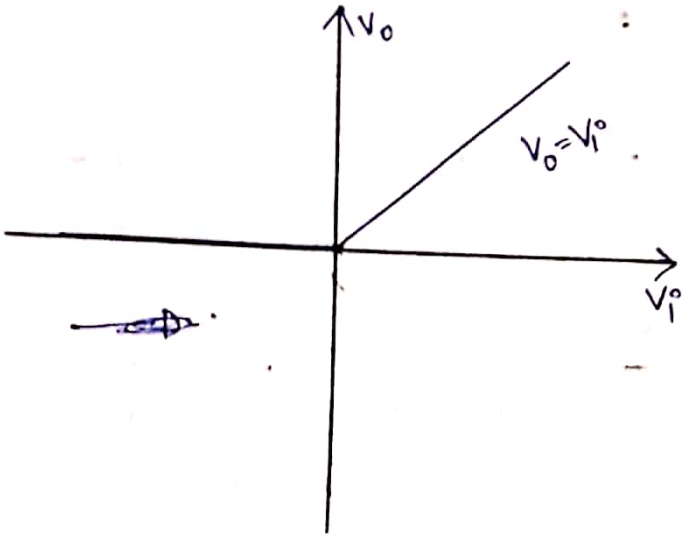
Case-1 : $V_P > V_N$, $V_i < 0$ - D -ON

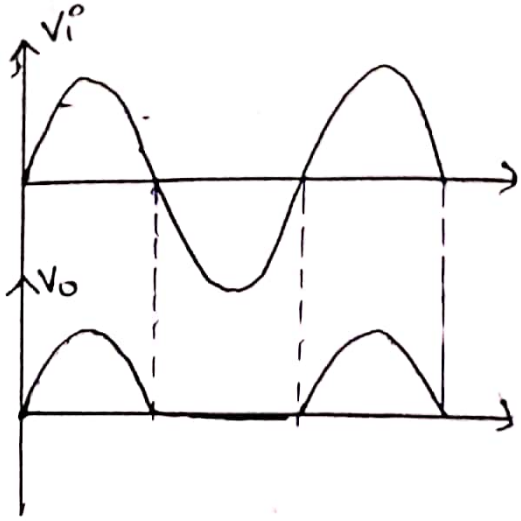
$V_o = 0$

Case-II : $V_P < V_N$, $V_i > 0$ - D-OFF

$V_o = V_i \times \frac{R_L}{R}$ $R << R_L$ $V_o = V_i$







5) Effect of cutin voltage with negative clipping

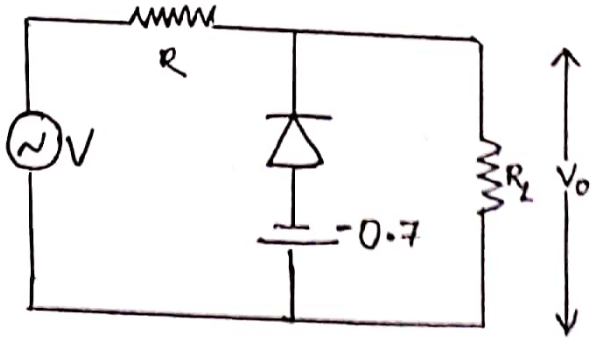
$V_P = -0.7$, $V_N = V_i$

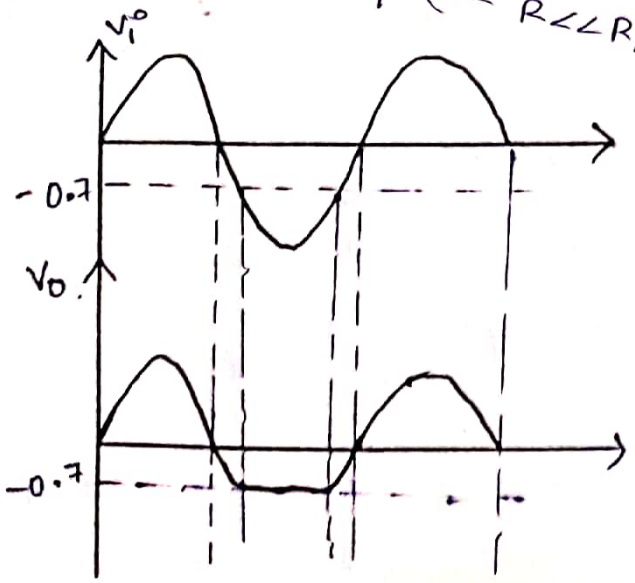
Case-1 : $V_P > V_N$, $V_i < -0.7$, $V_o = -0.7$

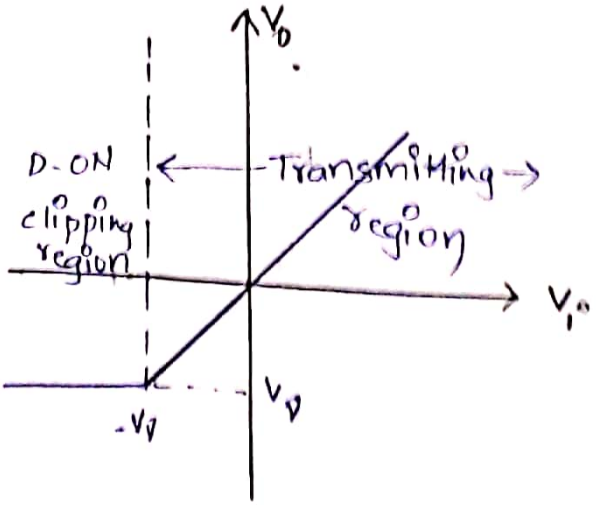
D-ON

Case-II : $V_P < V_N$, $V_i > -0.7$

D-OFF $V_o = V_i$ $\leftarrow R << R_L$ $V_D = V_i \times \frac{R_L}{R}$







Scanned by CamScanner

6) Negative parallel clipper with reference voltage V_R

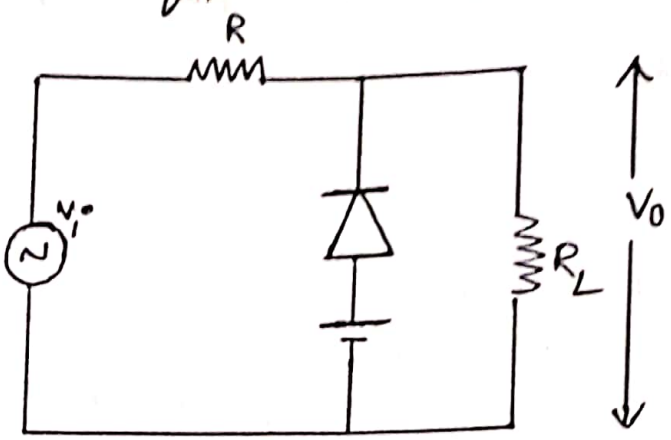
$V_P = V_R$; $V_N = V_i$

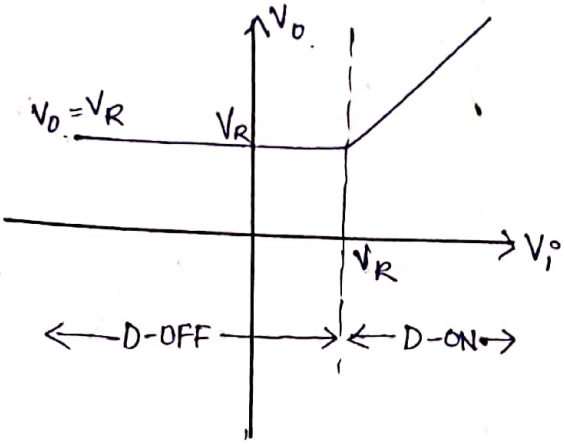
Case-1 : $V_P > V_N \rightarrow$ D-ON

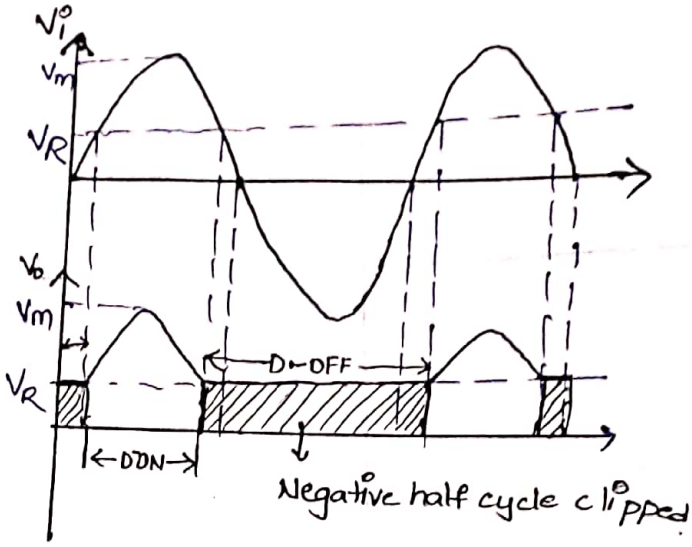
$V_i < V_R$, $V_O = V_R$

case-2 : $V_P < V_N$, $\rightarrow$ D-OFF

$V_i > V_R$, $V_O = V_i$

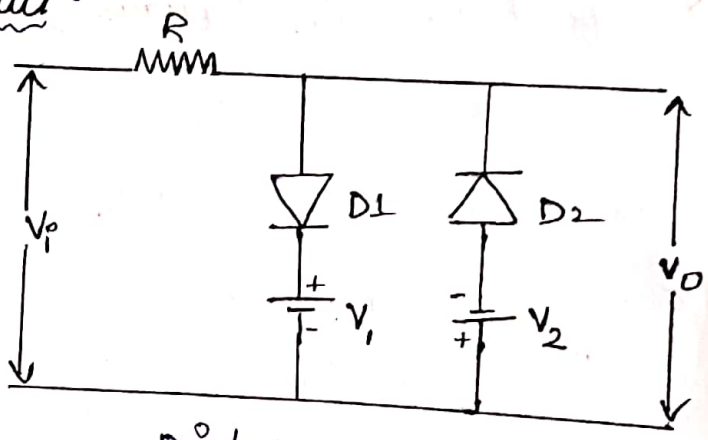






Two way Parallel clipper circuit.

Combining positive and negative clipper circuits with V_R, a two way parallel clipper can be obtained.



Diode 1

Assume D1 - OFF

$V_P = V_i$, $V_N = V_R$

i) $V_P > V_N$, $V_i > V_1$, $V_O = V_R$

D1 - ON

ii) $V_P < V_N$, $V_i < V_1$, $V_O = V_i$

D1 - OFF

Diode 2

Assume D2 - OFF

$V_N = V_i$, $V_P = -V_2$

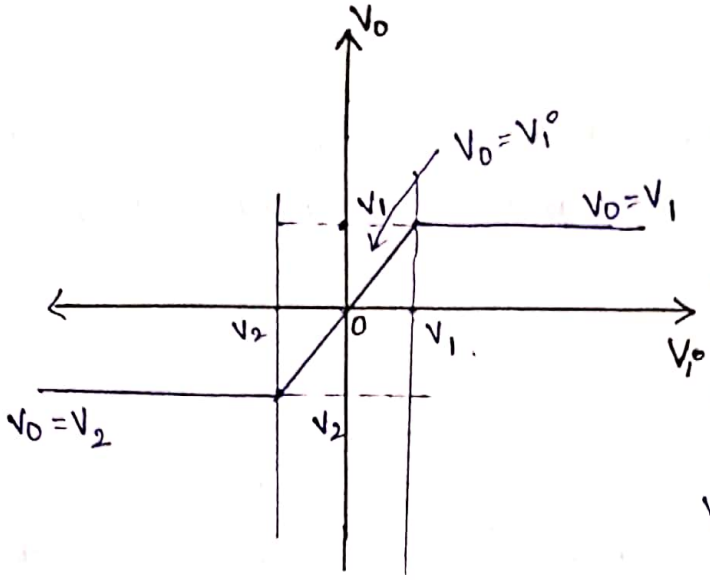
i) $V_P > V_N$, $V_i < -V_2$, $V_O = -V_2$

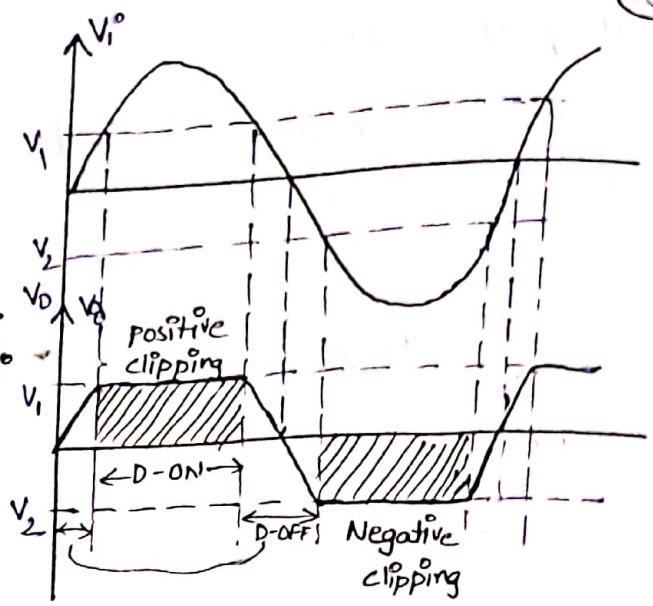
D2 - OFF

ii) $V_P < V_N$, $V_i > -V_2$, $V_O = V_i$

D2 - ON.

Scanned by CamScanner

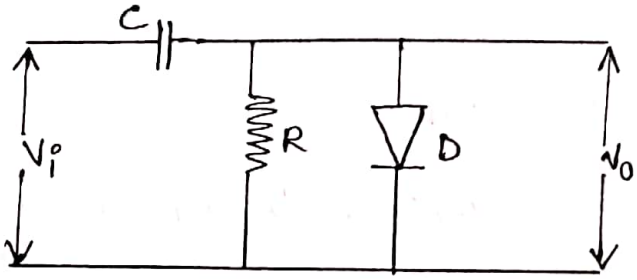




Clamping - Circuit Theorem

Statement: Under steady state conditions, for any input waveform, the ratio of the area under the output curve in forward direction (when the diode conducts) to the area under the output curve is in reverse direction [when diode does not conduct) is given by,

$$\frac{A_F}{A_R} = \frac{R_f}{R}$$



where

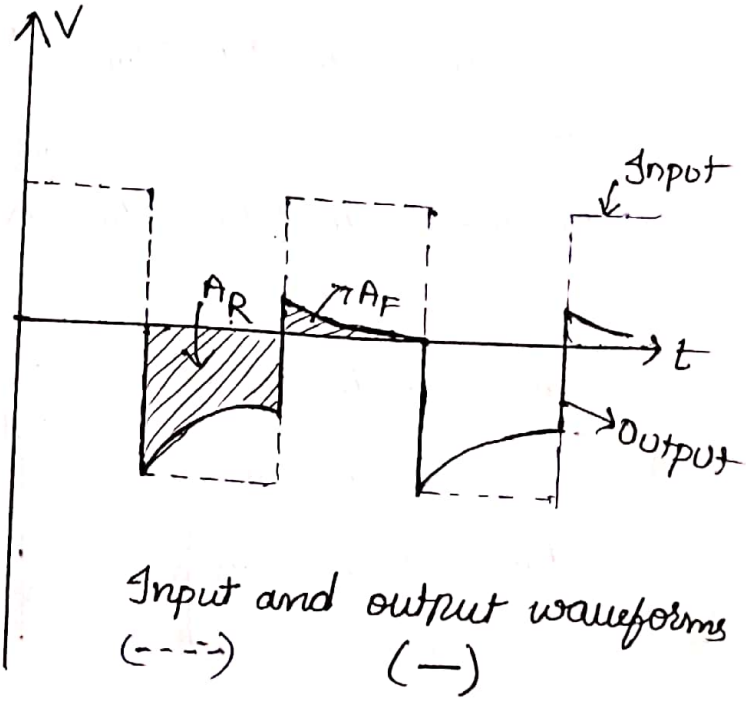
A_F = Area under output curve in forward direction

A_R = Area under output curve in reverse direction

R_f = Forward resistance of the diode

R = shunt resistance.

Input applied is square wave



Input and output waveforms (- - -) (—)

Scanned by CamScanner

Clamper Circuits

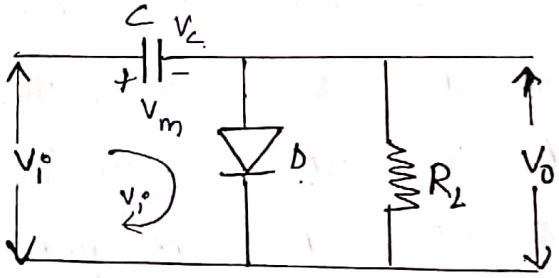
The circuits which are used to add a D.C level as per the requirements to the A.C output signal are called clamper circuits

Types of clampers

i) Negative clamper

The following assumptions are made while analysing the clamper circuit

1. The diode is ideal in behaviour
2. The time constant $\tau = RC$ is designed to be very large by selecting large values of R and C



$V_i° - V_c - V_0 = 0$

$\boxed{V_0 = V_i° - V_c}$

$\boxed{V_c = V_m}$

↳ Due to large RC time const the capacitor holds the entire charge & capcitor V remains as $V_c = V_m$

$V_i° = V_m$;

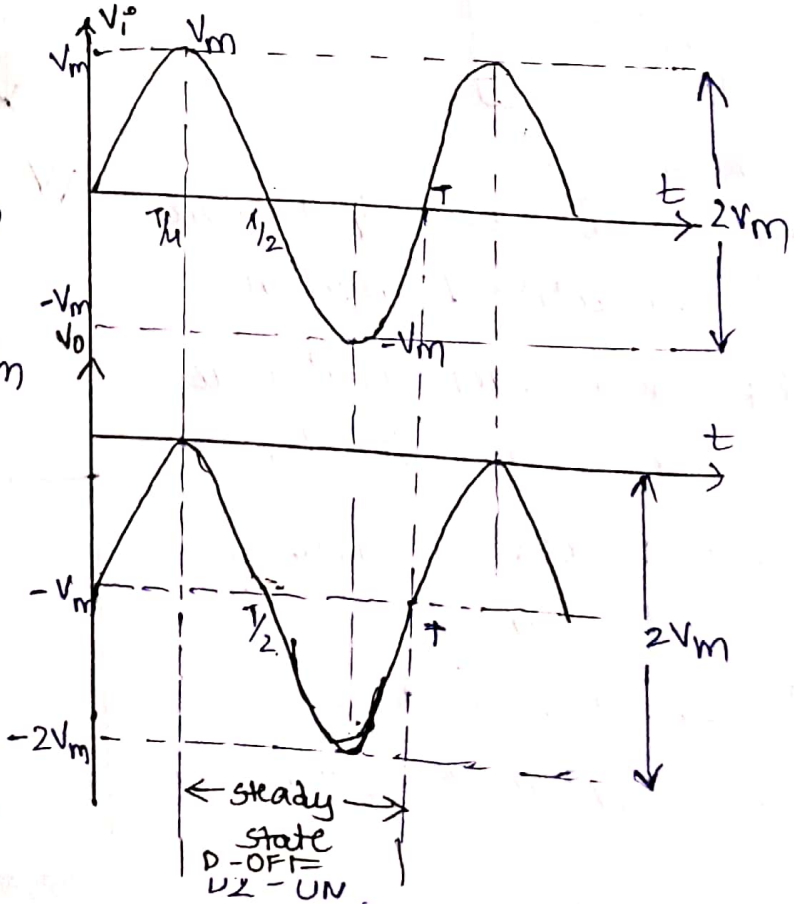
$V_0 = V_m - V_m = 0 \Rightarrow V_0 = 0$

$V_i° = 0$;

$V_0 = 0 - V_m = -V_m \Rightarrow V_0 = -V_m$

$V_i° = -V_m$;

$V_0 = -V_m - V_m = -2V_m \Rightarrow V_0 = -2V_m$

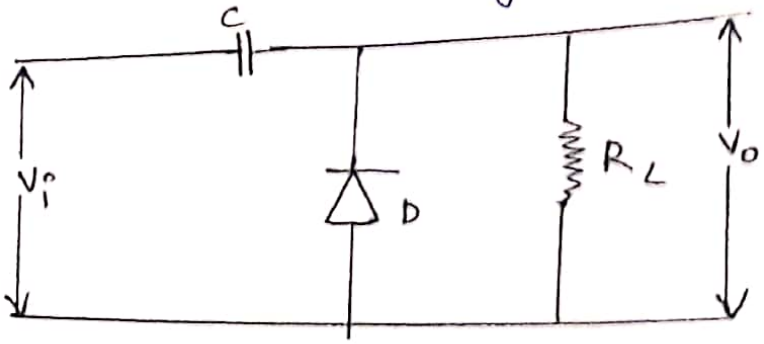


$V_0 = -V_m$	for $V_i° = 0$
$V_0 = 0$	for $V_i° = V_m$
$V_0 = -2V_m$	for $V_i° = -V_m$

Scanned by CamScanner

ii) Positive clamper

It adds +ve DC level to AC output signal



$V_c = -V_m$

$-V_i + V_c - V_o = 0$

$V_o = V_i - V_c$

When $V_i = V_m$

$V_o = V_m + V_m = 2V_m$

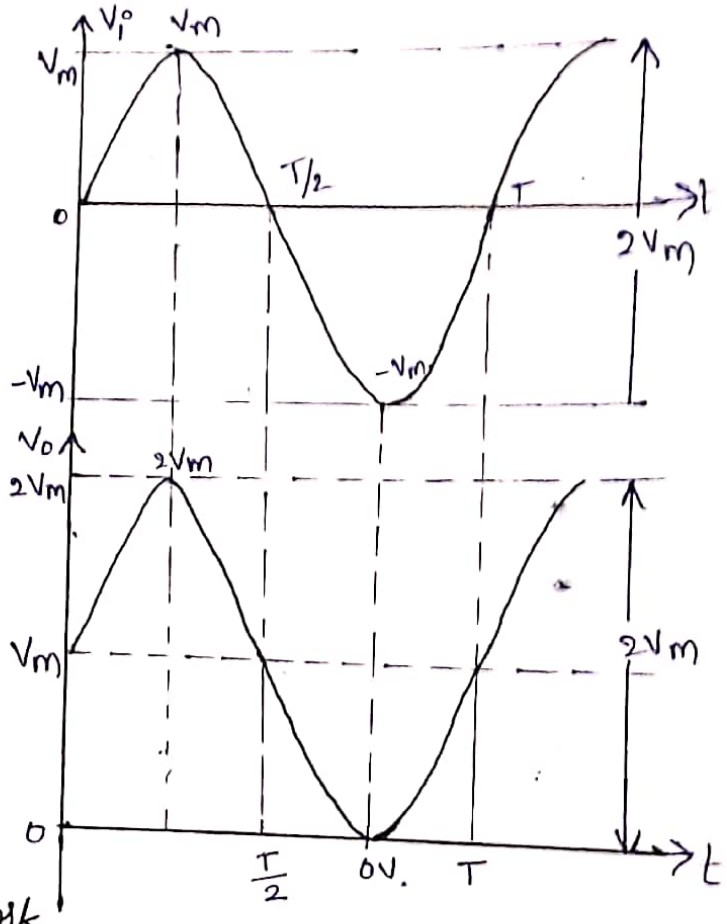
$\Rightarrow V_i = 0$

$V_o = 0 + V_m = V_m$

$\Rightarrow V_i = -V_m$

$V_o = -V_m + V_m = 0$

$V_o = V_m$	for $V_i = 0$
$V_o = 2V_m$	for $V_i = V_m$
$V_o = 0$	for $V_i = -V_m$



Steps to Analyze clamping Network

1) Start the analysis of the clamping network by considering that part of the input which will in forward bias the diode
2) When the diode is conducting, assume the capacitor charges instantly to the peak value of the input
3) Assume that the diode is not conducting, the capacitor remains charged at the peak value as there is no discharging path
4) Analyze the output and sketch the wave form

Scanned by CamScanner

3.1 Introduction: Now we are going to study about the active three terminal device, called BJT. Before 1950 all electronic equipments used vaccume tubes, in 1904, the vaccum-tube was introduced by J.A.Flemins. The vacume tube equipments required a bulky power supply to heat the tube and they created a lot of heat. For the proper operation of the vaccum-tube it requires warm-up period i.e heating time. when in 1950 the transistor was invented, by Dr. William Schockley, Dr John Bardeen and Dr walter.H. Brattain of Bell Telephone Laboratories, USA. its impact was immediate. Transistors have several advantages over vaccum-tubes

→ They require no heating-time
→ They require less power for operation
→ They are much smaller in size and light in weight
→ They are more efficient and have rugged construction
→ they have a much longer operating lifetime and are cheap.

The transistor impact on electronics has been enormous. Almost all electronic equipments now being designed use semiconductor transistor devices. The first transistor i.e point contact transistor, which is designed by Schockley Bardeen and Brattain, The point contact transistor was difficult to produce and was somewhat variable in its operating characteristics.

Figure 3.1

3.2 Junction Transistor:- Transistor is a silicon or a germanium crystal with three distinct regions. Basically, it consists of two p-n junctions connected back to back in a single piece of a semiconductor crystal. A junction transistor is simply a sandwich of one type of semiconductor material between two layers of the other type as shown in the figure 3.2

A transistor can be of two types i.e (i) pnp and (ii) npn.

If a layer of an n-type is sandwiched between two layers of p-type material it is called pnp transistor, and a layer of p-type is sandwiched betwee

two layers of n-type material it is called npn transistor. The middle [illegible] of each transistor type is called the BASE (B) of the transistor. This is very thin (10^{-6} m) and very lightly doped. The remaining two regions are called EMITTER (E) and COLLECTOR (C). The emitter is heavily doped than any of the other regions. It is physically larger than the base region and

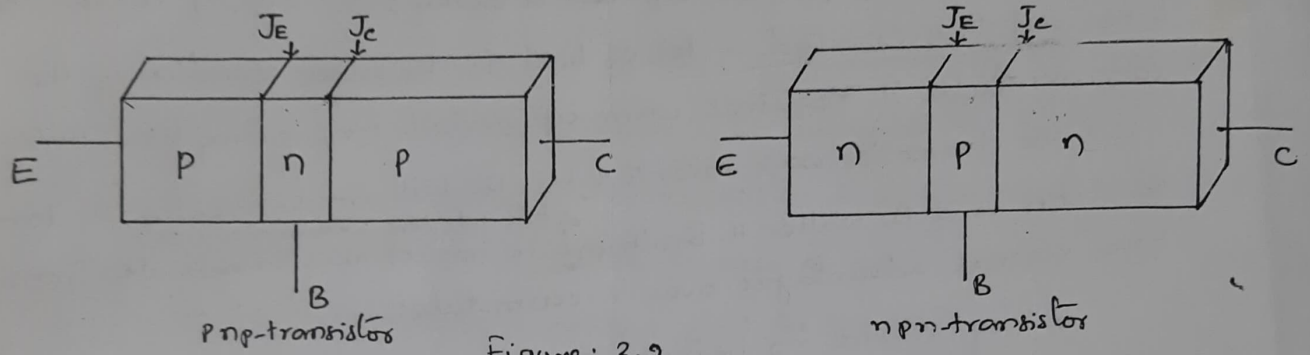


Figure: 3.2

Slightly smaller than that of collector region. Its main function is to supply majority charge carriers to the base (i.e electrons in case of npn transistor and holes incase of pnp transistor). The collector also heavily doped region than the base and slightly lower than that of emitter. It physically larger than any of the other regions. Its main function is to collect majority charge carriers through the base.

A transistor has two p-n junctions. One is between the emitter and the base and is called the emitter-base junction or simply the emitter junction (J_E). The other one is between the base and the collector and is called the collector-base junction or collector junction (J_C). Thus a transistor is called, in general, Junction transistor. The two p-n junction (diode) analogy of a transistor shown in the figure 3.3(A) and figure 3.3(B) illustrates the symbols of the transistors.

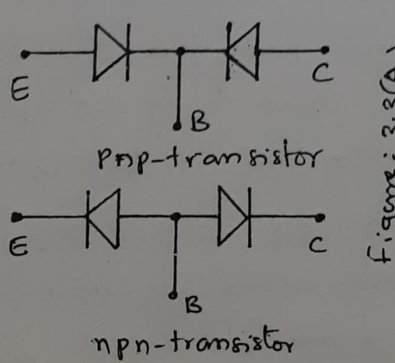


Figure: 3.3(A)

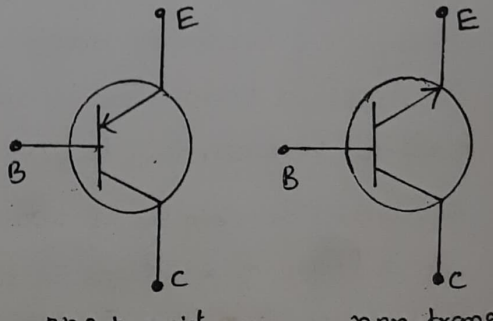


Figure: 3.3(B)

The main principle of a transistor is transfer of resistance, this has given the name Trans(fer) resistor = Transistor. The current conduction in a transistor, generally, is because of both the types of charge carriers electrons and holes hence the name Bipolar Junction transistor (BJT). On the other hand, if the current conduction is only due to one type of carriers (i.e either electrons or holes) then the junction transistor is called Unipolar Junction transistor.

As regards the symbols of the transistors, the arrowhead is always at the emitter (not at collector). It indicates the conventional current flow direction i.e in case of pnp transistor it is from emitter to base (emitter is positive w.r.t base) while in case of npn transistor it is from base to emitter (here base is positive w.r.t the emitter).

Because of difference in the size of the three regions and different ~~dopping~~ dopping levels, there is no possibility of exchange of collector and emitter terminals of a transistor in an electronic circuit.

NOTE: for the sake of convenience, it is customary to show emitter and collector to be of equal size.

When transistor is formed diffusion of charge carriers take place due to the charge gradient exist between the different regions. During the diffusion, the depletion region penetrates more deeply into the lightly dopped region (refere 1.7.3). As shown in the figure 3.4 depletion layer at the emitter junction penetrates more into the base region than the heavily doped emitter. Similarly, at the collector junction depletion layer penetrates more into the base region than the heavily dopped collector. It should be remember that, as collector is slightly less dopped than the emitter, the depletion layer widths at the emitter junction, inside the emitter is less than the depletion layer widths at the collector junction inside the collector.

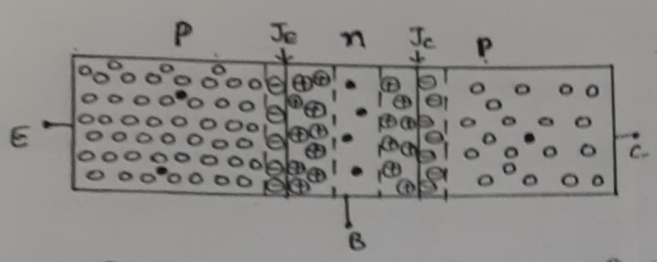


Figure: 3.4(A) pnp-transistor

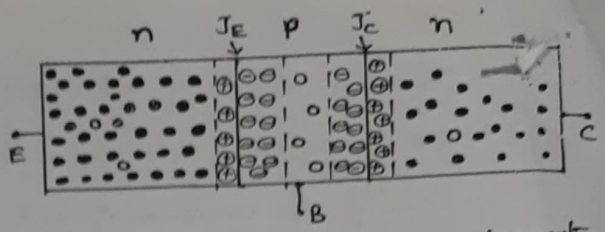


Figure: 3.4(B) npn-transistor

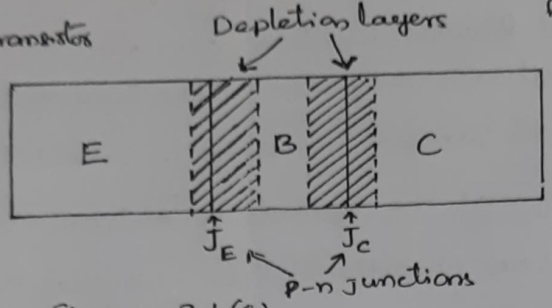


Figure: 3.4(C)

3.3 Operation of BJT :-

(A) Biasing :- For proper operation of a transistor, it is necessary to apply external voltages of correct polarity across its two junctions. Depending upon external voltage polarities used, the transistor works in any one of the three regions they are Active, Saturation and cut-off regions.

(i) for normal operation i.e Active region operation
- → Emitter junction is always forward biased
- → Collector junction is always reverse biased.

(ii) For saturation region
- → Both emitter junction and collector junctions are forward biased.

(iii) For cut-off region
- → Both emitter junction and collector junction are reverse-biased.

(B) Working of npn transistor:- The basic operation of the transistor will now be described using the npn transistor. The figure 3.5 shows a npn transistor with emitter junction forward biased by a dc source V_{EE} and the collector junction reverse biased by another dc source V_{cc}.

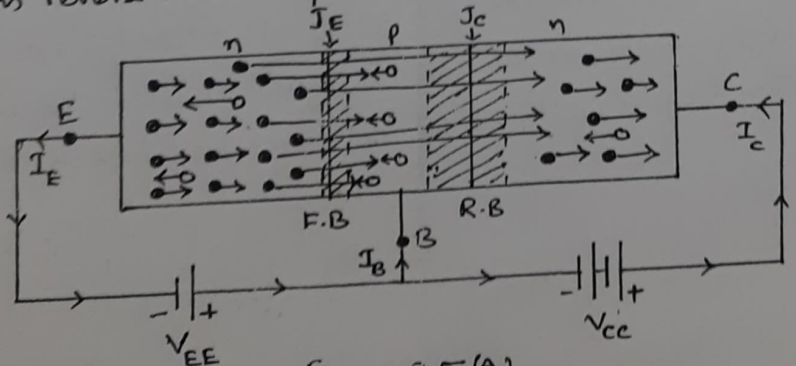


Figure : 3.5 (A)

Figure: 3.6(B)

Due to the forward bias between emitter and base the width of the depletion layer at the emitter junction is reduced i.e the electrons of n-region (Emitter) are repelled by the negative (~~terminal~~) potential of the external source and the potential barrier at this junction is reduced and hence electrons ~~the~~ cross the junction and diffuse into p-region i.e base. This constitutes the emitter current I_E. The width of the base is very thin and is lightly doped. As these (emitted) electrons flow through the p-type base, they tends to combine with holes in base region. Only two to five percent of the emitted electrons will recombine with the holes of the p-~~region~~ type base region. This constitutes the base current I_B, which is, of course, is very small. The remaining large number of electrons (95% to 98%) are able to drift across the base and ~~emitter~~ enter the collector region. And then electrons are sweep by the positive potential of external source V_{cc}. This constitutes collector current I_c.

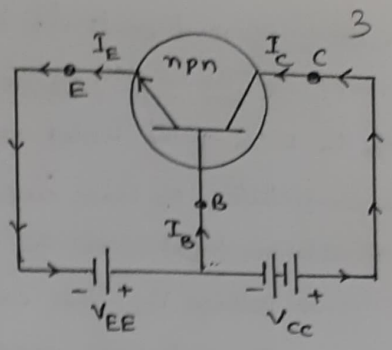


Figure: 3.5(B)

For every electron flowing out and entering the positive terminal of the source V_{cc}, an electron from the negative terminal of the source V_{EE} enters the emitter region. These new electrons then moves immediately toward the emitter junction and the process is thus repeated. In this way electrons conduction take place continuously as long as the two p-n junctions are properly biased. Thus the current conduction in an npn transistor is predominently by electrons.

(C) **Working of p n p transistor** :- Let us consider a pnp transistor with emitter junction forward biased and collector junction reverse biased, as shown in the figure 3.6

The holes of emitter (P-type) region (i.e majority charge carriers) are repelled by the positive potential of the source V_{EE} to wards the base. The potential barrier at emitter junction is reduced as it is forward biased and hence the holes cross

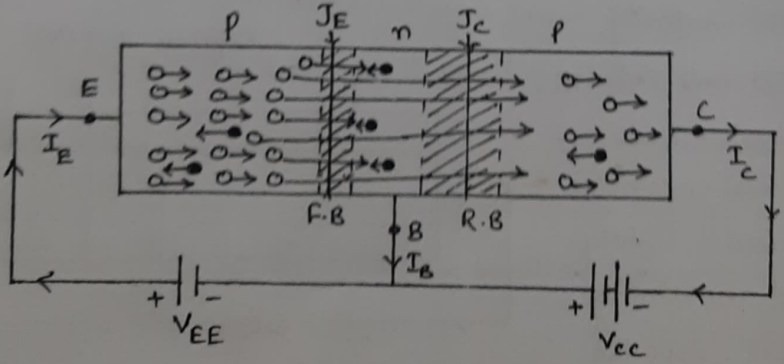


Figure: 3.6(A)

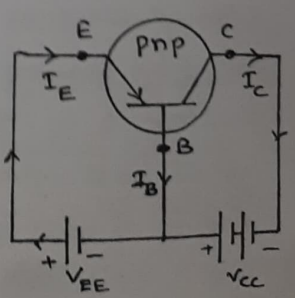


Figure: 3.6(B)

this junction and penetrate into n-type base region. This constitutes the emitter current I_E. The width of the base is very thin and is lightly dopped, hence only 2% to 5% of the holes recombine with the free electrons in n-type base region. This constitutes the base current I_B. The remaining large number of holes i.e 95 to 98% are able to drift across the base and enter the collector. They are sweep by the negative collector voltage V_{cc}. This constitutes the collector current I_C.

As each hole reaches the collector terminal, an electron is emitted from the negative terminal of the source V_{cc} and neutralizes the hole. At the same time a covalent bond near the emitter terminal breaks down and generates electron-hole pair, the new liberated electron leaves the emitter terminal and enters the positive terminal of the source V_{EE} to start its way around the outer circuit to the V_{cc}, while the new hole immediately moves towards the emitter junction and the process is repeated. Hence it should be remembered that the holes are the current carriers with in the pnp transistor from emitter to collector while the current conduction through the external circuit (i.e connecting wires) is carried out by electrons. Further more the collector current is slightly less than the emitter current and the collector current is a function of the emitter current.

NOTE:- In the both cases, i.e npn and pnp operations, explained above beside majority charge carrier current there is a current flow which is due to minority charge carriers

3.4 Transistor currents and current components:-

As shown in the figures 3.5(B) and 3.6(B), for example in a pnp transistor, the current flowing into the emitter (it is flowing-out for npn transistor) is refered to as the emitter current I_E, the currents flowing out (into) of the collector and base are refered to as collector current I_C and Base current I_B respectively.

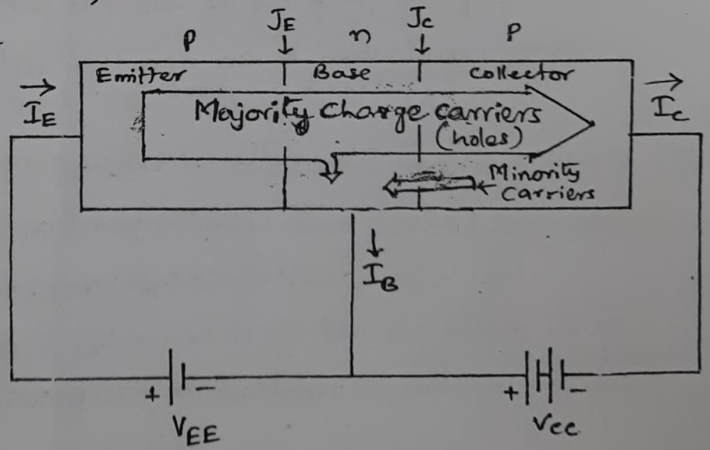


Figure: 3.7 (A)

From the total majority Charge carriers that are entering into (or leaving from) the emitter 2 to 5% are recombine at the base region due to lightly doping of base and remaining 98 to 95% carriers cross the

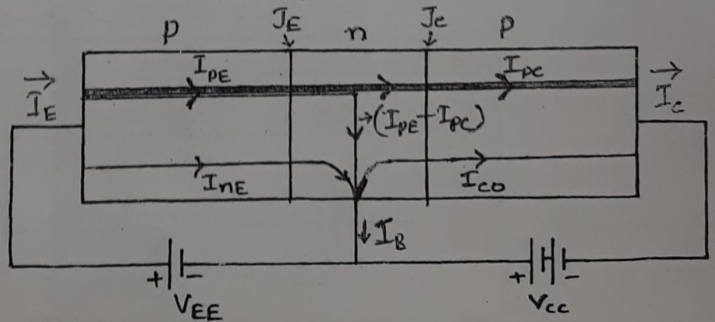


Figure: 3-7(B)

collector junction. Thus the emitter current I_E is always equal to the sum of the base and collector currents. This is true for both types of transistors npn and pnp.

i.e $\boxed{I_E = I_B + I_C}$

Since the base current is very small, therefore the emitter current and collector currents are nearly equal

$\boxed{I_E \approx I_C}$ $\quad \because I_B << I_C$

NOTE: In a typical transistor I_E and I_C are a few milliamperes and I_B is a few microamperes. The value of Base current I_B depends upon base thickness, bias voltage, doping levels and geometry i.e shape of the transistor.

The figure 3.7(A) shows the flow of electrons and holes in the various regions i.e majority and minority carriers flow in a transistor. The figure 3.7(B) shows the various current components which flow across the forward biased emitter junction (J_E) and the reverse biased collector junction (J_C). From the figures, it is clear that, the majority charge carriers (in this case holes) crossing from the emitter into base and the minority charge carriers (i.e electrons) crossing from the base into the emitter. Thus the emitter current I_E consists of hole current I_{pE} (majority carrier current) and electron current I_{nE} (minority carrier current). The ratio of hole to electron current, ie I_{pE}/I_{nE}, crossing the emitter junction is proportional to the ratio of the conductivity of the emitter material (i.e p-type) to that of the base (i.e n-type). In a commercial transistor, we know that, The doping level of the emitter is much larger than that of the base. Hence the emitter current I_E is mainly due to holes. The holes crossing emitter junction J_E and collector junction J_C are constitutes the collector current I_{pC}. Not all the holes (majority carriers of emitter region which are now in the base) crossing the emitter junction J_E reaches the collector junction J_C because some of them are combined with the free electrons in the base. This constitutes a small base current $(I_{pE} - I_{pC})$.

If the emitter terminal is open, i.e $I_E = 0$, then I_{pC} would be zero. As the collector junction J_C is reverse biased, the collector current I_C is only due to the minority carriers, i.e I_C would be equal to the reverse saturation current I_{CO}.

As indicated earlier, the emitter current is sum of the collector and base currents. The collector current, however, is compound of two components - the majority carrier current and minority carrier current components, the

minority component is called the Reverse Leakage current I_{CO} (It is known as collector current with emitter open).

$$\therefore \boxed{I_E = I_B + I_C}$$

and $I_C = I_{C\,majority} + I_{C\,minority}$

i.e $\boxed{I_C = I_{pc} + I_{CO}}$

NOTE: For common base transistor configuration, the reverse leakage current is I_{CBO} while for the common emitter transistor configuration it is I_{CEO}. The relation between the I_{CBO} and I_{CEO} is $\boxed{I_{CEO} = (\beta+1) I_{CBO}}$

3.5 TRANSISTOR AS AN AMPLIFIER:—

Let us consider a pnp transistor Circuit as shown in the figure 3.8. As usual, the emitter junction is forward biased and the collector junction is reverse biased. The input signal is applied between the emitter and base and the output is obtained across the load R_L connected between collector and base.

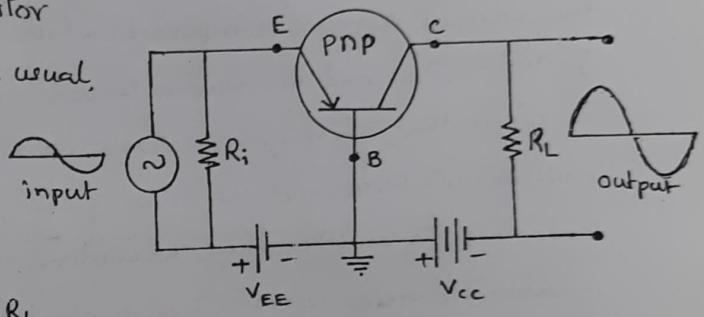


Figure: 3.8

When an ac is fed to the input, During the positive half-cycle increases the forward bias of the emitter junction which causes more holes to flow. Consequently emitter current and hence the collector current increases. These current variations produces corresponding voltage variations across the load R_L. Thus, the voltage drop across the load R_L also increases. Similarly, during the negative half-cycle of ac causes the transistor current to decrease. Since the emitter junction is forward biased, the depletion region around this junction is much smaller than that around collector junction which is reverse biased. Consequently, the internal resistance R_{EB} of emitter junction is much smaller than the internal resistance R_{BC} of the collector junction. Hence the power dissipation in the collector junction is $P_{BC} = I_C^2 R_{BC}$ and the power dissipated in the emitter junction is $P_{EB} = I_E^2 R_{EB}$. But we have seen that $I_C \approx I_E$ and $R_{BC} >> R_{EB}$. Hence $P_{BC} >> P_{EB}$ i.e the power dissipated at the collector junction is much higher than that dissipated at the emitter junction. In other words output power is much greater than the input. This is the amplifying action of the transistor.

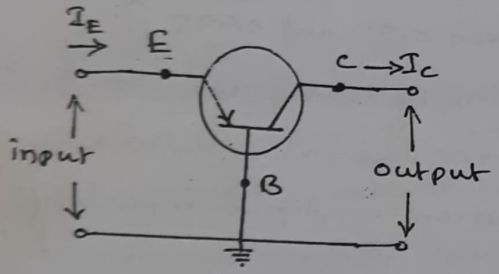
Now n-type layer is to be deposited on this substrate using diffusion process. The opposite type (in this case p-type) silicon is then applied by using diffusion method. Finally an n^+ emitter is diffused and SiO_2 layer and metallic connectors added, as shown in the figure 3.13, to form a npn transistor.

3.7 Transistor configurations :-

The performance of a transistor mainly depends upon the configuration in which it is connected in an electronic circuit. A transistor may be connected in the circuit with any one of its terminals common to both input and output. This common terminal is usually grounded. Accordingly, a transistor may be operated in any one of the following three configurations.

(1) common-base configuration (CB).
(2) common-emitter configuration (CE).
(3) common-collector configuration (CC).

pnp transistors



npn transistors

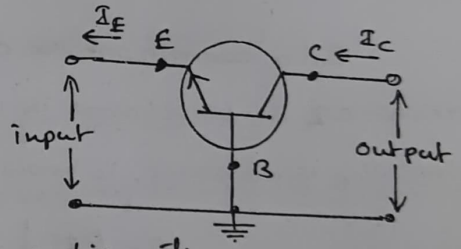
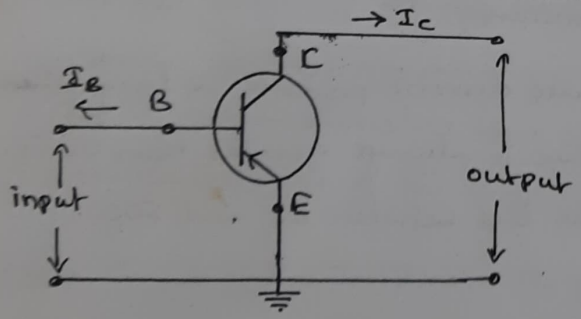


Figure : 3.14(A) Common-base configuration



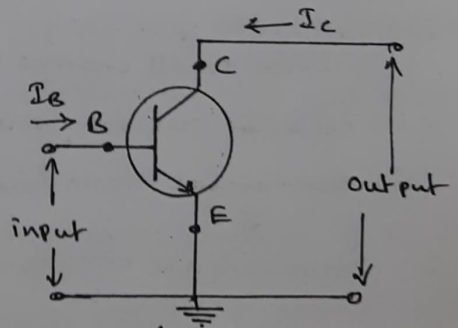
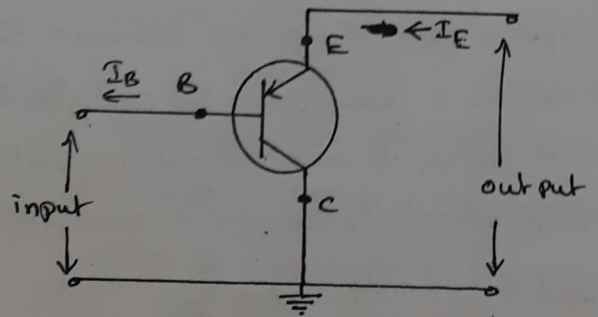


Figure : 3.14(B) Common-emitter configuration



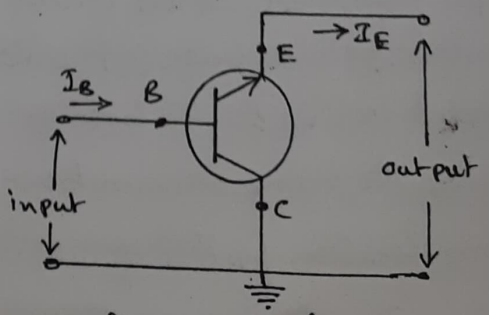


Figure : 3.14(C) Common-collector configuration

3.7.1 Transistor constants Alpha and Beta:-

Before discussing the configurations of the transistor one should know that constants of a transistor. In general, the ratio of the variations in the output to the variations in the input current at constant output voltage, is know as transistor constant or current amplification factor or forward current transfer ratio.

In a common-base configuration, the ratio of change in output current i.e collector current ΔI_c to the change in input current i.e emitter current ΔI_E when the collector to base bias voltage V_{CB} is maintained at a constant, is called current amplification factor α.

$$\text{i.e} \quad \alpha = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=\text{constant}} = h_{fb} \text{ (interms of h-parameters)}$$

We know that, in a CB configuration, the collector current is slightly less than the emitter current, hence the α is slightly less than unity. for commercial transistors α value lies between 0.95 and 0.995.

In a common emitter configuration, the ratio of change in collector current ΔI_c to the change in base current when the collector to emitter voltage V_{CE} is constant, is know as the current amplification factor β.

$$\beta = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}} = h_{fe} \text{ (interms of h-parameters)}$$

Since small changes in the base current produces a large changes in collector current, hence β value is always greater than unity. for commercial transistors β value lies between 20 and 500.

3.7.2 Common-base configuration:-

Figure 3.14(A) shows the common base configuration of pnp and npn transistors. In this circuit the input signal is applied between the emitter (E) and base (B) while the output is taken from the collector C and base (B). As the base is common to input and output circuits hence the name common base configuration. The transistor current amplification factor of C.B is α and is given by $\alpha = \frac{I_C}{I_E}$

The total collector current consists of the following two components

(i) the current produced by the majority carriers in the normal transistor action i.e $\propto I_E$ $\quad \because \alpha = \frac{I_c}{I_E} \Rightarrow I_c = \alpha I_E$

(ii) the current produced by the minority carriers i.e leakage current I_{CBO}

∴ The total collector current $\boxed{I_c = \alpha I_E + I_{CBO}}$ in a C.B. configuration.

3.7.2.1 V-I characteristics of CB configuration :-

Figure 3.15 shows the circuit arrangements to determine the V-I characteristics of a pnp transistor connected in common base configuration Here a pnp transistor is connected in C.B. configuration with the help of variable d.c sources V_{EE} and V_{cc}. Millimeters are connected in series with Emitter and collector to measure the I_E and I_c respectively. Similarly voltmeters are connected in parallel across E and B to measure the voltages V_{BE} and across C and B to measure V_{CB} respectively. The electrical behaviour of a common base transistor can be described by stating the relationship between different voltages and respective currents. This relationship can be plotted graphically and the curves Thus obtained are known as V-I characteristics. Here we shall consider the input and output characteristics of the pnp transistor.

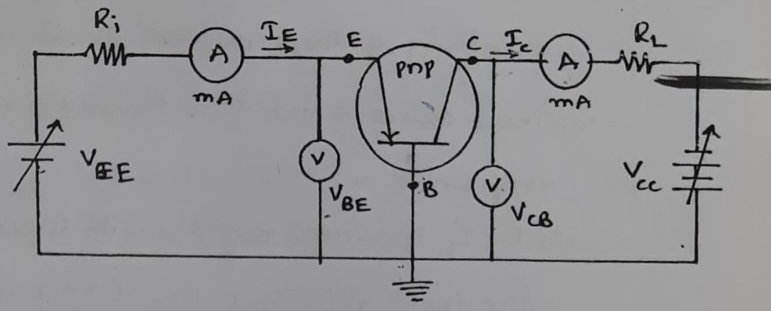


Figure: 3.15

3.7.2.2 Input characteristics :- The curves showing the variation of the (I_E) emitter current with emitter-base voltage V_{EB} at constant collector voltage V_{CB}, are called the input characteristics of the C.B transistor.

For plotting the input characteristics, the collector-base voltage V_{CB} is kept fixed. the ~~coll~~ emitter-base voltage V_{BE} is varied with the help of variable d.c source V_{EE} and the emitter current I_E is noted for each value of V_{BE}. The procedure is then repeated for other fixed values of V_{CB}. Then curves are plotted between V_{BE} and I_E, as shown in fig 3.16.

It may be seen that these curves are exactly similar to the forward characteristics of a p-n diode.

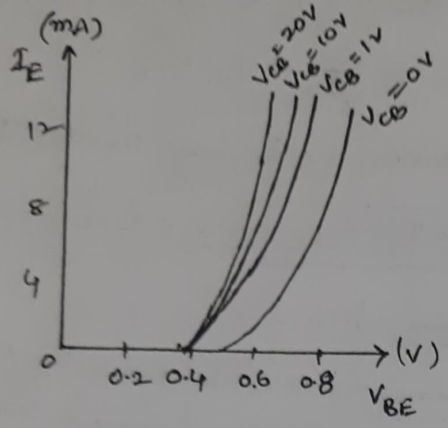


Figure: 3.16

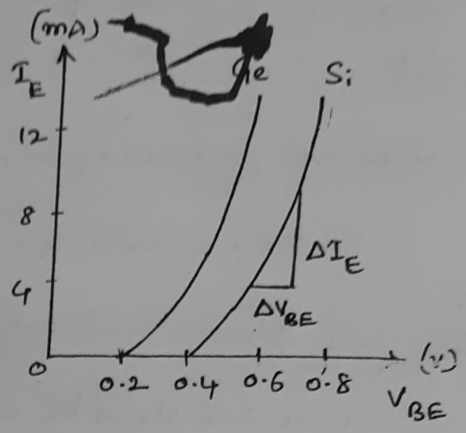


Figure: 3.17

A study of these curves reveals the following facts:

(i) There exists a cut-in or threshold voltage of V_{BE} below which the I_E is very small.

(ii) The I_E increases rapidly with increasing value of V_{BE}. This shows that the input resistence R_{in} is very small

$$\text{i.e } R_{in} = \left.\frac{\Delta V_{BE}}{\Delta I_E}\right|_{V_{CB}=\text{constant}}$$

The Figure 3.17 shows the input characteristics of Si and Ge. These characteristics are hardly affected by changes either in V_{CB} or in temperature

3.7.2.3 Output characteristics:- The curves showing the variation of the (I_C) collector current with the collector-base voltage V_{CB} at a constant emitter current (I_E), are called the output characteristics of the common-base transistor.

For plotting the output characteristics, the emitter current (I_E) is kept fixed. With the help of variable d.c source V_{cc}, the value of V_{CB} is varried in steps and (I_C) collector current is noted for each value of V_{CB}. A curve is then plotted between V_{CB} and I_C. The curve so obtained is known as the output characteristic. The process is then repeated for different fixed values of I_E, as shown in the figure 3.18.

A study of these curves reveals the following facts:-

(i) As the collector voltage V_{CB} is increased starting from zero, initially, there is a rapid increase in the collector current I_c and it reaches a value constant. Thus the entire variations in the collector current take place at very low values of V_{CB}.

(ii) A very large change in the V_{CB} produces only a tiny change in the collector current I_c. It means that the output resistance R_{out} is very high

$$\text{i.e } R_{out} = \left.\frac{\Delta V_{CB}}{\Delta I_c}\right|_{I_E = \text{constant}}$$

(iii) The collector current I_c does not becomes zero when the collector voltage becomes zero for any value of emitter current, but is very small. It is called Reverse leakage current I_{CBO}

We know that, the collector current $I_c = \alpha I_E + I_{CO}$

But $I_E = I_B + I_C \Rightarrow I_C = \alpha(I_B + I_C) + I_{CO}$

$$= \alpha I_B + \alpha I_C + I_{CO}$$

$$(1-\alpha) I_C = \alpha I_B + I_{CO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CO}$$

Now let $\frac{\alpha}{1-\alpha} = \beta$ then $\frac{1}{1-\alpha} = \frac{\beta}{\alpha} = 1+\beta$

$\frac{\alpha}{1-\alpha}$

α

$$\therefore I_C = \beta I_B + (1+\beta) I_{CO}$$

$$\Rightarrow \boxed{I_C = \beta I_B + I_{CBO}} \quad \text{where } I_{CBO} = (1+\beta) I_{CO}$$

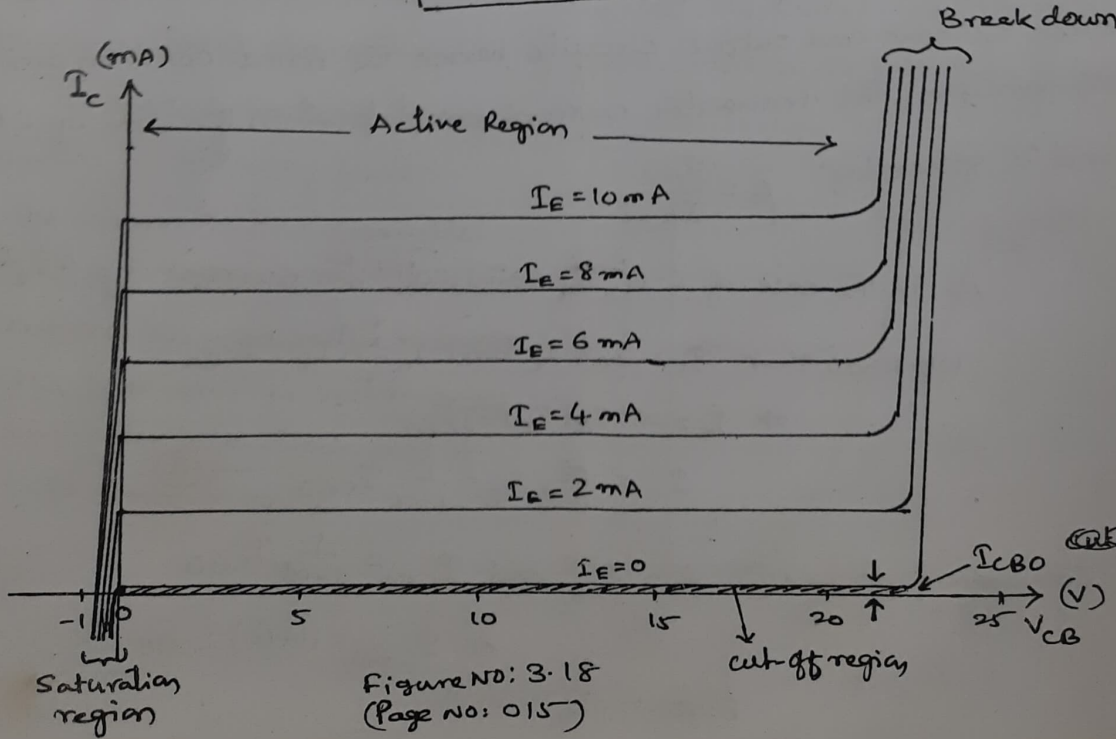


Figure No: 3.18
(Page No: 015)

The family of characteristic curves is divided into three regions

(i) Active region :- when emitter junction is forward biased and collector junction is reverse biased, the collector current I_c is essentially independent of V_{CB} and depends only upon the emitter current. Hence the curves appear to be practically flat. However, if V_{CB} is increased beyond a certain value, the I_c eventually increases rapidly due to avalanche break down.

(ii) Saturation region :- when both emitter junction and collector junctions are forward biased the collector current I_c flows even when $V_{CB}=0$. Actually, in pnp transistor, V_{CB} is slightly positive in this region and because of this forward biasing, there results large change in I_c with a small change in V_{CB}. A forward bias implies that the p-type collector is made positive w.r.t n-type base and hence current flows from collector to base. This hole current causes a positive increment in the collector current. So that the collector current increases rapidly.

(iii) Cut-off region :- When both emitter junction and collector junctions are reverse biased, a small amount of current I_c flows even when emitter current $I_E=0$. This is the reverse leakage current I_{CBO}. The region below $I_E=0$ characteristics is called cut-off region.

3.7.3 Common-Emitter configuration :- Figure 3.14(B) shows the common-emitter configuration of pnp and npn transistors. In this circuit the input signal is applied between the base (B) and emitter (E) while the output is taken from the collector (C) and emitter (E). As the E is common to input and output circuits, hence the name common emitter configuration. The transistor current amplification factor of CE is β and is given by $\beta = \frac{I_c}{I_B}$

As in the case of C.B, the total collector current $I_c = \beta I_B + I_{CEO}$ —(A)

we know that $I_E = I_B + I_c$ and $I_c = \alpha I_E + I_{CBO}$

$\Rightarrow I_c = \alpha(I_B + I_c) + I_{CBO}$

$I_c = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$ —(B)

Comparing (A) and (B) $\beta = \frac{\alpha}{1-\alpha}$ and $I_{CEO} = \frac{1}{1-\alpha} I_{CBO}$

or $I_{CEO} = (1+\beta) I_{CBO}$

3.7.3.1 V-I characteristics of C-E configuration:-

The characteristics of a pnp transistor connected in the common emitter configuration may be determined by the use of a circuit as shown in the figure 3.19.

In this circuit the variable d.c source V_{BB} provides forward bias to emitter junction. A voltmeter is connected across base (B) and emitter (E) to measure V_{BE}.

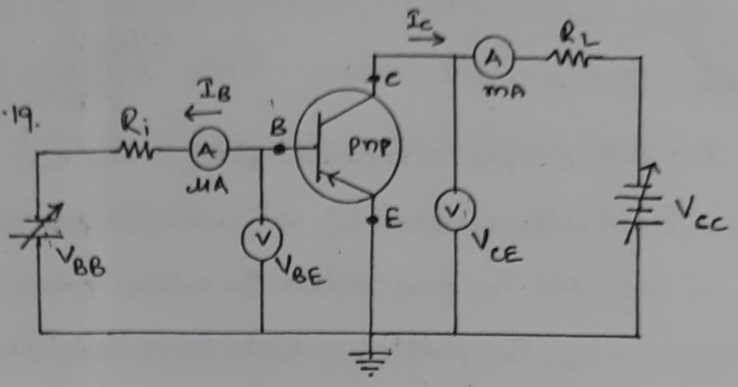


Figure: 3.19

A micro-ammeter is connected is series with the base to measure I_B. Similarly a milliammeter is connected in the collector circuit to measure I_C. To measure V_{CE} another voltmeter is connected across collector (C) and emitter (E). A variable source V_{CC} is connected between C and E to vary V_{CE}.

3.7.3.2 Input characteristics:- The curves, showing the variation of the base current (I_B) with base-emitter voltage V_{BE} at constant collector-emitter voltage V_{CE}, are called the input characteristics of a C.E. transistor.

For plotting the input characteristics, the collector-emitter voltage V_{CE} is kept fixed, the base-emitter voltage V_{BE} is varied with the help of variable d.c source V_{BB} and the base current I_B is noted for each value of V_{BE}. A graph of I_B against V_{BE} is then plotted. The procedure is repeated for other fixed values of V_{CE}. The curves so obtained is known as input characteristics of C.E transistor, as shown in the figure: 3.20

A study of these curves reveals the following facts:

(i) The characteristics resembles that of a forward-biased diode curves. This is expected because the base-emitter section of the transistor is a diode and it is forward biased.

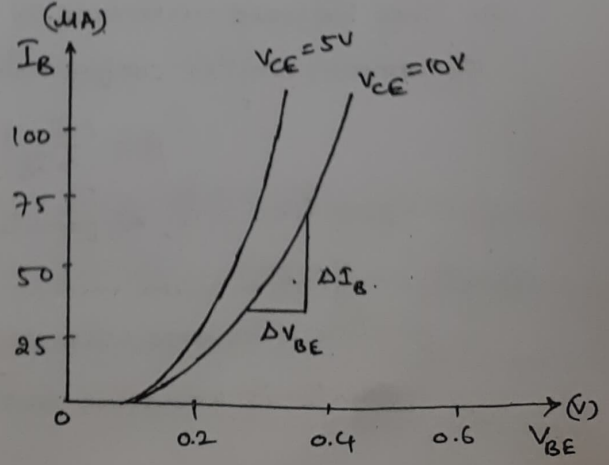


Figure: 3.20

(ii) In this case, I_B increases less rapidly with V_{BE} as compared to C-B configuration. this shows that the input resistance of C-E configuration is higher compared to that in C-B configuration

$$R_{in} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE} = \text{constant}}$$

3.7.3.3 Output characteristics :- The curves, showing the variation of the collector current I_C with collector-emitter voltage V_{CE} at a constant base current I_B, are called the output characteristics of a common emitter transistor.

For plotting output characteristics, the base current I_B is kept fixed, with the help of variable d.c source V_{CC} the value of V_{CE} is varied in steps and the collector current I_C is noted for each value of V_{CE}. The procedure is repeated for other fixed values of I_B. A graph of I_C against V_{CE} is then plotted. the curves so obtained are known as output characteristics as shown in the figure: 3.21.

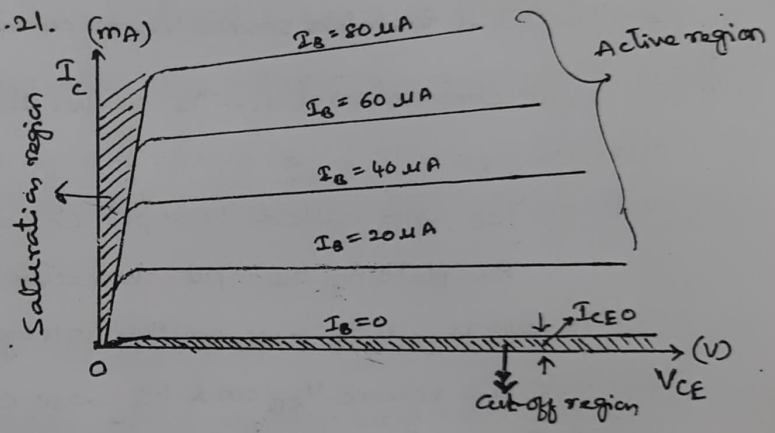


Figure: 3.21

A study of these curves reveals the following facts:

(i) The I_C varies rapidly with V_{CE} for very small voltages. After this I_C becomes almost constant and is decided entirely by base current I_B and becomes independent of V_{CE}.

(ii) The I_C is not zero when base current is zero, this is due to the inherent intrinsic conduction in semiconductors i.e due to minority carriers.

(iii) Since the base current I_B is in micro amperes and I_C is in milliamperes, the common emitter configuration exhibits a current amplification.

$$\beta = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE} = \text{constant}}$$

Just like C-B, the family of o/p curves is divided into three regions:

① Active region:- when emitter junction is forward biased and collector junction is reverse biased, the area above $I_B = 0$ and to the right side of ordinate, is known as active region

for a given value of I_B, the emitter injects certain number of majority charge carriers into the base. When collector-emitter voltage V_{CE} is small, the collector is unable to collect all charge carriers. Therefore, when V_{CE} is increased, collector current I_c first increases (as it collects maximum injected carriers) and then the rate of increase is quite small.

(ii) Saturation region: The region very close to the zero voltage axis where all the curves merge and fall rapidly towards origin, it known as Saturation region. In this region, the emitter junction as well as collector junction are forwarded biased.

(iii) Cut-off region: When both emitter junction and collector junctions are reverse biased, the characteristic for $I_B=0$ passes through origin but there is appreciable gap between the curve for $I_B=0$ and x-axis this small amount of current I_{CEO} is known as reverse leakage current and the area under the $I_B=0$ and x-axis is known as the cut-off region.

3.7.4 common-collector configuration:- Figure 3.14 (c) shown the common collector configuration of pnp and npn transistors. In this circuit, the input signal is applied between the base (B) and collector (C) while the output is taken from the emitter (E) and collector (C). As the C is common to input and output circuits, hence the name common collector configuration. The transistor current amplification factor of C.C is γ and is given by

$$\gamma = \frac{I_E}{I_B}$$

3.7.4.1 V-I characteristics of C.C configuration:- Figure 3.22 shows the pnp transistor connected in common collector configuration for drawing the V-I characteristics. Once again the emitter junction is forward biased by connecting the source V_{EE} and similarly the collector junction is reverse biased by V_{BB}.

3.7 ... configuration):- In the C·B configuration,

3.7.4.2 Input characteristics:-

The curves, showing the variation of base current I_B with collector base voltage V_{CB} at constant collector-emitter voltage V_{CE}, are called the input characteristics

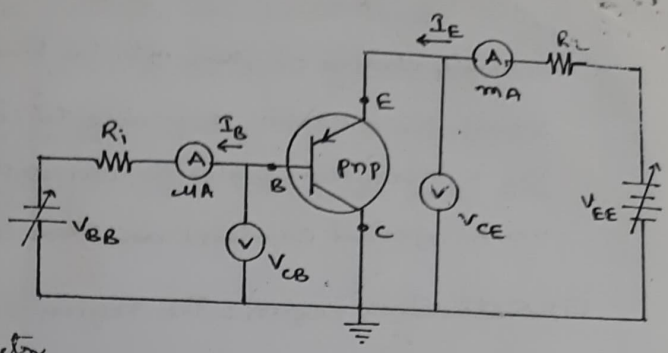


figure : 3.22

for plotting input characteristics, the emitter-collector voltage V_{CE} is kept fixed. The base collector voltage V_{CB} is varied with the help of source V_{BB} and the base current I_B is noted for each value of V_{CB}. A graph of I_B against V_{CB} is then plotted. The procedure is repeated for other fixed values of V_{CE}. the curves so obtained are called the input characteristics.

Figure 3.23 shown the input characteristics of C·C configuration. These characteristics are quite different from those for CB or CE. Because the input voltage V_{CB} is large determined by the value of C·E voltage. It may be seen that with an increase in V_{CB}, V_{BE} gets decreased thereby decreasing I_B.

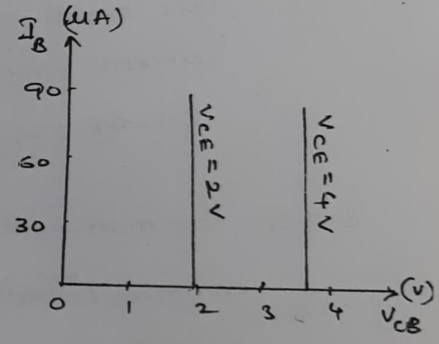


Figure : 3.23

3.7.4.3 Output characteristics:-

The curves, showing the variation of the emitter current I_E with V_{CE} at constant base current, are called output characteristics.

Figure 3.24 gives the plot of I_E versus V_{CE} for several fixed values of I_B. It may be seen that these characteristics are practically identical to that of the C·E because $I_C \simeq I_E$.

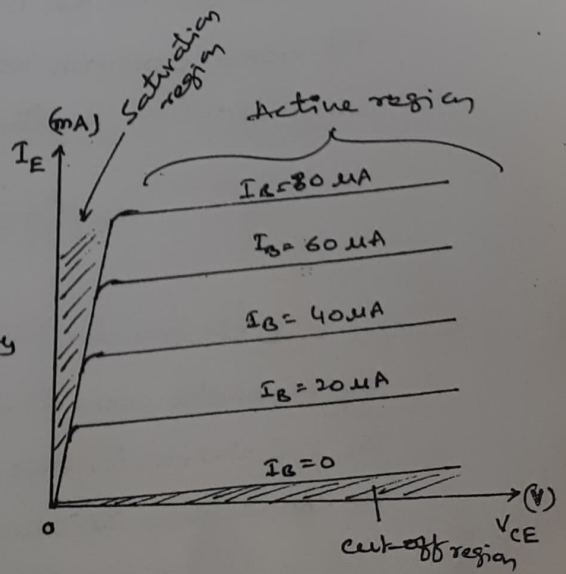


Figure : 3.24

3.7.5: Early effect (Base-width modulation):- In the C.B configuration, as the collector voltage V_{cc} is made to increase the reverse bias, the space charge (depletion region) width between the collector and base tends to increase, with the result that the effective width of the base decreases. This dependency of base-width on collector-to-base voltage V_{CB} is known as the base-width modulation or Early effect. This decrease in the base width has three consequences:

(i) There is less chance for recombination with in the base region. Hence α increases with V_{CB}.

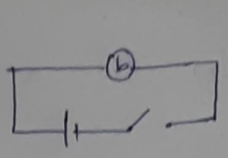
(ii) the charge gradient is increased with in the base, and consequently, the current of minority carriers injected across the emitter junction increases.

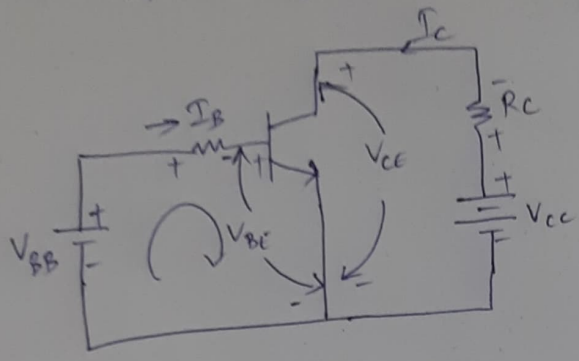
(iii) for extremely large voltages, the effective base-width may be reduced to zero, causing voltage breakdown in the transistor. this phenomenon is called the punch through effect.

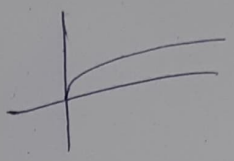
3.87.7 Comparision of Transistor configuralions:-

S.NO	Parameter	C.B	C.E	C.C
1	I/p resistance	very low	low	high
2	O/p resistance	very high	high	low
3	Current amplification factor	$\alpha = \frac{I_C}{I_E}$	$\beta = \frac{I_C}{I_B}$	$\gamma = \frac{I_E}{I_B}$
4	Current gain	less than unity	20 to 500	high (20 to 500)
5	Voltage gain	medium	medium	low
6	Applications	As a input stage of a multistage amplifier	for audio signal amplification	for impedance matching

Transistor as switch







Apply KVL at i/p

$$+V_{BB} - I_B R_B - V_{BE} = 0$$

$$V_{BB} = I_B R_B + V_{BE}$$

$$V_{BE} = V_{BB} - I_B R_B$$

V_i

Apply KVL at o/p

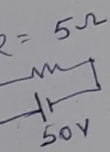
o/p

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CC} = V_{CE} + I_C R_C$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_o = V_{CC} - I_C R_C$$



$$I = \frac{50}{5}$$

$$= 10$$

When $V_i < V_t$

$I_B = 0$

$I_C = 0$

$V_o = V_{CC}$

↓

off state
(current is 0)

when $V_i > V_t$

$I_B \uparrow$

$I_C \uparrow$

$V_o = V_{CC} - I_C R_C$

$V_o = 0$

↓

on state
(current is max)

Switching times of transistor:

1) Delay time (t_d):
time req. for current to rise to 10% of max.

2) t_r rise time:
t.r for current to rise 10 to 90 of max

3) t_{on} turn on time:

$t_d + t_r$

4) t_s (storage time): It is time when I is dropped from 90% of its max.

5) t_f fall time(f) 90 to 10%.

6) t_{off} : $t_f + t_{sf}$

turn off time

→ Operating point

* **BJT Biasing** :- In order to operate transistor in the desired region an external dc voltage has to be applied with correct polarity and magnitude to the two junctions of the transistor. This is known as biasing of the transistor.

→ Because dc voltages are used to bias the transistor, biasing is known as dc biasing of the transistor.

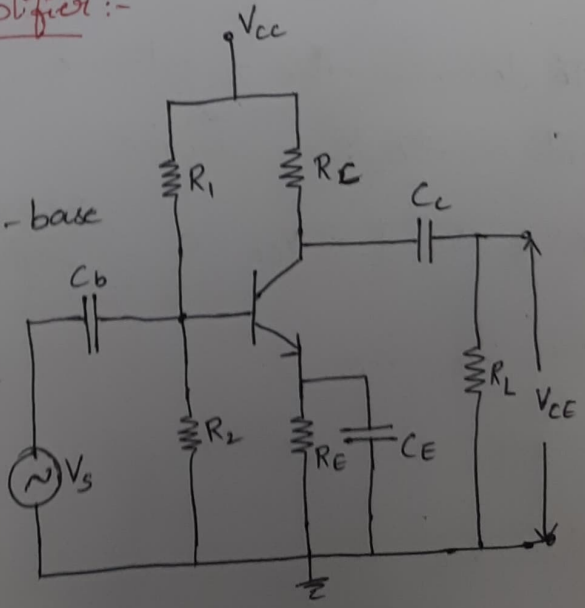
* **Operating point** :- When biasing is provided to a transistor, certain current and voltage conditions are established for the transistor.

→ These conditions are known as operating point or operating conditions or quiescent point (it means quite, still, inactive).

→ The operating point must be stable for proper operation of the transistor.

* **DC equivalent model of CE amplifier** :-

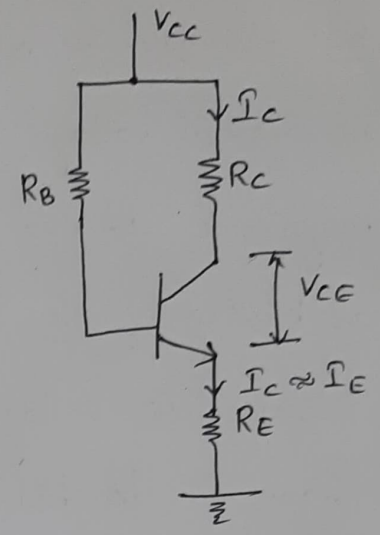
→ Transistor is biased with a common supply such that emitter-base junction is forward biased & collector-base junction is reverse biased, ie, transistor is in active region.



CE amplifier ckt.

→ In the absence of AC signal, the capacitors provide very high impedance ie, open circuit.

→ Applying KVL to the collector circuit we get,



DC equivalent ckt.

$$V_{CC} = I_C R_C + V_{CE} + I_C R_E$$

$$V_{CC} = I_C (R_C + R_E) + V_{CE}$$

$$I_C (R_C + R_E) = V_{CC} - V_{CE}$$

$$\Rightarrow I_C = \left(\frac{-1}{R_C + R_E}\right) V_{CE} + \left(\frac{1}{R_C + R_E}\right) V_{CC}$$

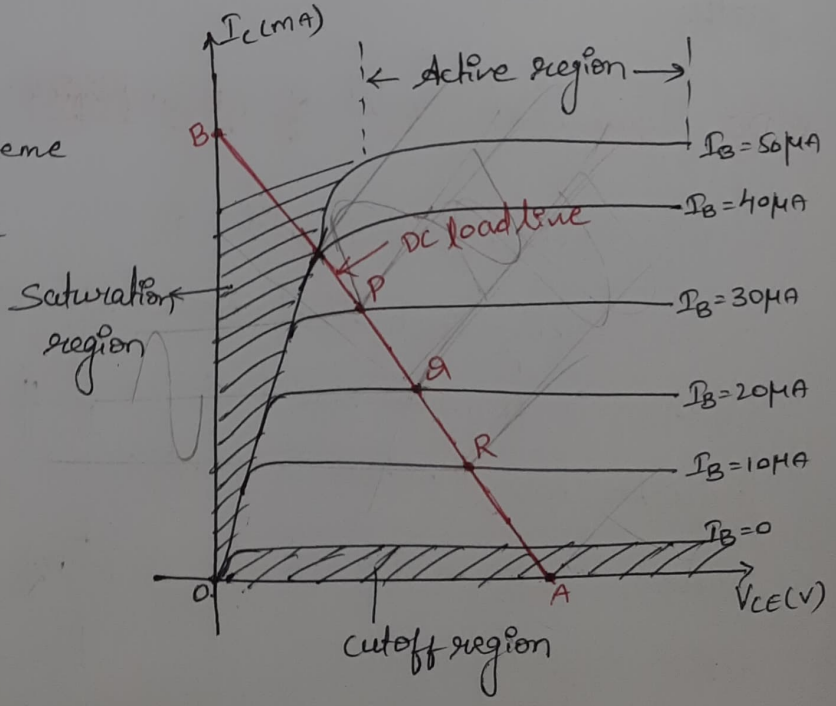
$$I_C = \left(\frac{-1}{R_{dc}}\right) V_{CE} + \frac{V_{CC}}{R_{dc}} \qquad \because R_{dc} = R_C + R_E$$

→ compare this equation with $y = mx + c$.

→ It is a straight line on the graph of I_C vs V_{CE} which is having slope $\left(\frac{-1}{R_{dc}}\right)$.

→ To determine the 2 extreme points on the line, assume

(i) $V_{CE} = V_{CC}$ & (ii) $V_{CE} = 0$



(i) When $V_{CE} = V_{CC}$

$\Rightarrow I_C = 0$, point A

(ii) When $V_{CE} = 0$

$\Rightarrow I_C = \frac{V_{CC}}{R_{dc}}$, point B

→ The line drawn between the points A & B on the output characteristics is called dc load line.

→ The 'dc' word indicates that only dc conditions are considered i.e., input ac signal is assumed to be zero.

→ The intersection of the characteristic curve and dc load line is the operating point.

→ The point is fixed on the curve, so it is called as quiescent point or Q-point.

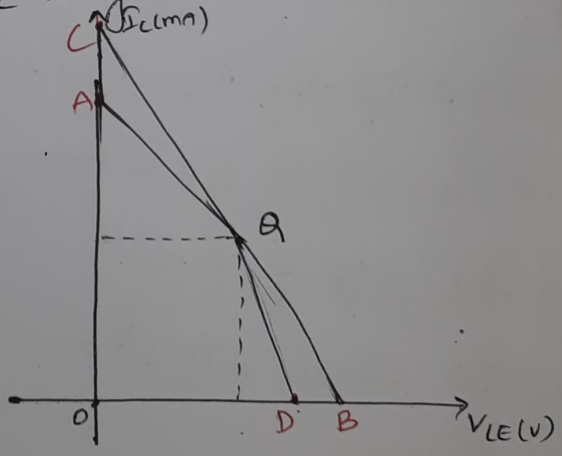
→ For different values of I_B, there will be different intersection points (P, Q, R in the fig.)

→ After choosing the Q point at the center of the dc load line, ac load line is also drawn through the Q point.

→ The effective ac load resistance Rac is given as

$$R_{ac} = R_C \| R_L$$

$$\text{slope of } CQD = \left(\frac{-1}{R_{ac}}\right)$$



→ To draw ac load line, max. V_{CE} & max I_C when the signal is applied are required.

max $V_{CE} = V_{CEQ} + I_{CQ} R_{ac}$, point D

max $I_C = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$, point C

* Bias stabilization :-

→ The biasing circuit should be designed to fix the Q-point, but only fixing of the Q-point is not sufficient.

→ When designing the biasing circuit, care should be taken so that the Q-point will not shift into an undesirable region.

→ Three important factors are to considered while designing the biasing circuit which are responsible for shifting the Q-point.
(i) I_{CO}, (ii) Transistor current gain β, (iii) V_{BE}
Temperature,

* Thermal Runaway :- (I_{CO})

→ Minority carriers are temperature dependent. ie, they increase with the temperature.

→ The increase in the minority carriers increases the leakage current I_{CO}.

→ Specifically, I_{CO} doubles for every 10°c rise in temperature.

→ Increase in I_{CO} in turn increases the I_C which leads to the shift of Q point.

→ This process will become cumulative leading to thermal runaway.

→ Due to this, the ratings of the transistor are exceeded which may destroy the transistor itself.

* Variation in V_{BE} :- V_{BE} is also temperature dependent. If Temp increases by 1°c then V_{BE} decreases by 2.5mV. This dependency of V_{BE} on temp. causes a change in I_B & hence I_C also changes.

* Current gain β :-

→ There are changes in the transistor parameters among different units of same type ie, if 2 transistors units of same type (same number, construction, parameters specified etc) are used in the circuit, there will be a change in β value in actual practice.

→ The β value may change from unit to unit, thus shifting the Q-point.

From all this explanation, the requirements of the biasing circuit can be summarised as follows:

* Requirements of a biasing circuit:

1) The emitter junction must be forward biased and the collector junction must be reverse biased, ie the transistor should be operated in the middle of the active region or Q-point should be fixed at the center of the active region.

2) The circuit design should provide a degree of temperature stability.

3) The Q-point should be made independent of the transistor parameters (β).

* Stability factor :-

→ In order to compare the stability provided by different biasing circuits, one term is raised called stability factor.

→ It indicates the degree of change in Q-point due to variation in temperature.

→ Since there are 3 variables (I_{CO}, V_{BE} & β) which are temperature dependent, 3 stability factors can be defined.

1) $$S = \frac{\partial I_C}{\partial I_{CO}}\Big|_{V_{BE}, \beta \text{ constant}} \quad \text{or} \quad S = \frac{\Delta I_C}{\Delta I_{CO}}\Big|_{V_{BE}, \beta \text{ constant}}$$

2) $$S' = \frac{\partial I_C}{\partial V_{BE}}\Big|_{I_{CO}, \beta \text{ constant}} \quad \text{or} \quad S' = \frac{\Delta I_C}{\Delta V_{BE}}\Big|_{I_{CO}, \beta \text{ constant}}$$

3) $$S'' = \frac{\partial I_C}{\partial \beta}\Big|_{I_{CO}, V_{BE} \text{ constant}} \quad \text{or} \quad S'' = \frac{\Delta I_C}{\Delta \beta}\Big|_{I_{CO}, V_{BE} \text{ constant}}$$

Note: (i) Ideally, stability factor should be zero to keep Q-point stable.

(ii) Practically stability factor should have the value as minimum as possible.

$$\Delta I_C \simeq S.\Delta I_{CO} + S'\Delta V_{EB} + S''\Delta\beta$$

* Stability factor 'S' equation:-

→ For a CE configuration, I_c is given as:

~~$I_c = \beta I_B + I_{CEO}$~~

$$I_c = \beta I_B + (1+\beta) I_{CBO}$$

Differentiating this eqn w.r.to I_c,

$$1 = \beta \frac{\partial I_B}{\partial I_c} + (1+\beta) \frac{\partial I_{CO}}{\partial I_c}$$

$$\Rightarrow (1-\beta) \frac{\partial I_B}{\partial I_c} = (1+\beta) \frac{\partial I_{CO}}{\partial I_c}$$

$$\therefore \frac{\partial I_{CO}}{\partial I_c} = \frac{1-\beta\left(\frac{\partial I_B}{\partial I_c}\right)}{1+\beta}$$

$$S = \frac{\partial I_c}{\partial I_{CO}} = \frac{1+\beta}{1-\beta\left(\frac{\partial I_B}{\partial I_c}\right)}$$

From the above eqn, it is clear that S should be as small as possible to have better thermal stability.

→ The process of making operating point independent of temperature changes (or) variations in the transistor parameters is known as stabilization.

→ For maintaining the Q-point independent of these variations the following techniques are used.

i) ~~Stabilization~~ Biasing techniques, ii) Compensation techniques.

* Methods of transistor biasing :-

The most commonly used methods of transistor biasing are:

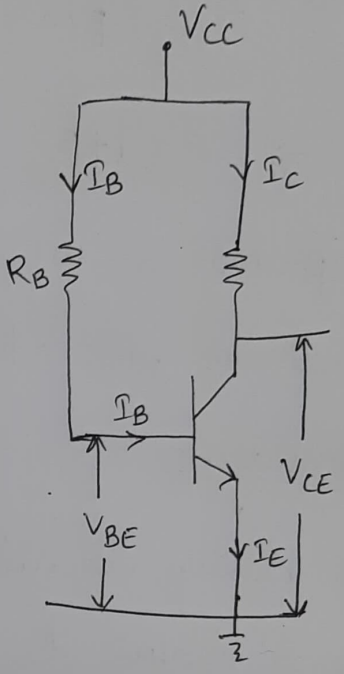
1) Fixed bias / Base resistor method
2) Emitter feedback bias
3) Collector to emitter feedback bias
4) Voltage divider bias or self bias or emitter bias.

1) Fixed Bias or Base bias method:

→ In this method a high resistance R_B is connected between the base and the V_{cc} supply.

→ Biasing is provided by V_{cc}

→ The required value of base current I_B can be made to flow by selecting the proper value of R_B.



$$V_{cc} - I_B R_B - V_{BE} = 0$$

$$V_{cc} = I_B R_B + V_{BE}$$

$$I_B = \frac{V_{cc} - V_{BE}}{R_B} \quad \text{— (1)}$$

→ V_{BE} is 0.3V for Germanium & 0.7V for Silicon (which is very small)

$$\Rightarrow I_B \cong \frac{V_{cc}}{R_B}$$

∴ V_{cc} & R_B are fixed, I_B will be fixed

→ So, the circuit is called Fixed Bias circuit.

→ In eqn. (1) β is not appearing & V_{cc}, R_B are fixed then the biasing point is also fixed.

$$\text{Stability factor } S = \frac{1+\beta}{1-\beta \frac{dI_B}{dI_C}}$$

→ But in fixed bias method, I_B is independent of I_C.

so, $\frac{dI_B}{dI_C} = 0$

$$\Rightarrow S = \frac{1+\beta}{1-\beta \times 0}$$

$$\Rightarrow S = 1+\beta$$

→ If $\beta = 100$, $S = 101$ which is very large i.e, fixed bias method has poor thermal stability.

* Advantages:

(i) The biasing circuit is very simple as only one resistance R_B is required.

(ii) Easy to fix the operating point anywhere in the active region by changing the value of R_B.

(iii) Provides maximum flexibility in design.

* Disadvantages:

(i) This method provides poor stabilization. It is because there is no means to stop a self increase in I_C due to temperature variations & individual variations.

(ii) Stability factor is very high. Therefore, there are strong chances of thermal runaway.

* Self bias or emitter bias or voltage divider bias:-

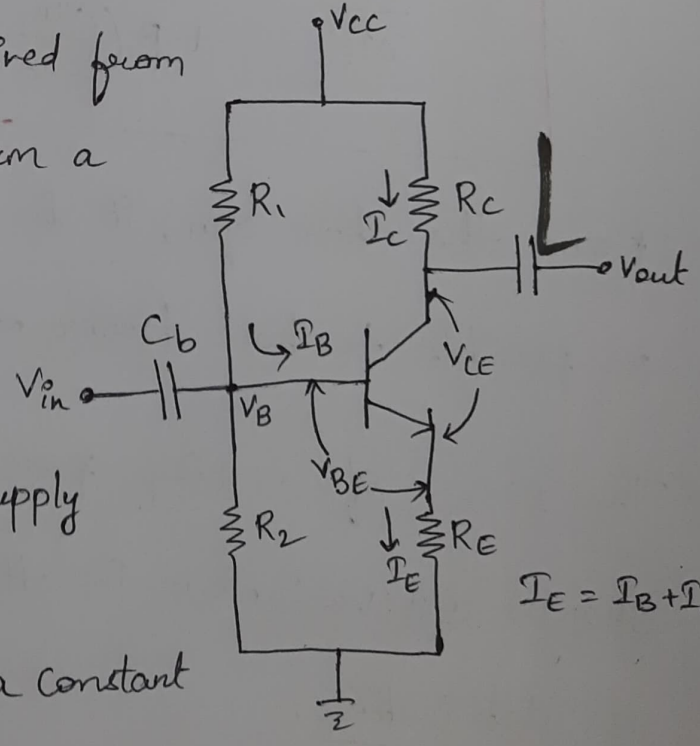
→ A simple circuit used to establish a stable operating point is the self bias configuration.

→ It is also known as universal bias stabilization ckt.

→ The name voltage divider is derived from the fact that resistors R_1 & R_2 form a potential divider across V_{cc}.

→ Voltage drop V_B across R_2 forward biases the emitter where as V_{cc} supply reverse biases the collector.

→ Self-bias circuit can be used as a constant current circuit.



$I_E = I_B + I_C$

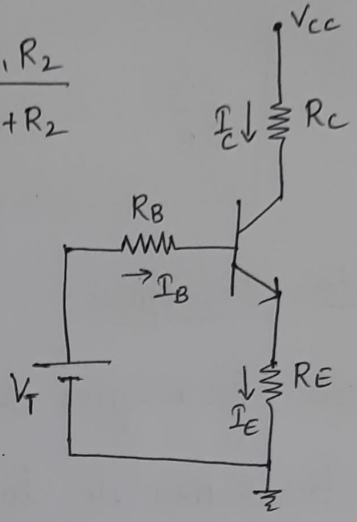
self bias circuit

→ If I_C ↑ses with ↑se in I_{CO} due to temperature, voltage drop across R_E ↑ses there by ↓sing I_B. So I_C is maintained almost constant.

Stability factor 'S':

→ By using Thevenins theorem self bias circuit can be modified as

$$V_T = \frac{R_2}{R_1+R_2} V_{CC} \quad \& \quad R_B = R_1 \| R_2 = \frac{R_1 R_2}{R_1+R_2}$$



Applying K.V.L

$$V_T = I_B R_B + V_{BE} + I_E R_E$$

$$= I_B R_B + V_{BE} + (I_C + I_B) R_E$$

$$= I_B (R_B + R_E) + V_{BE} + I_C R_E$$

$$\Rightarrow I_B = \frac{V_T - V_{BE}}{R_B + R_E} - \left(\frac{R_E}{R_B+R_E}\right) I_C$$

differentiate w.r.to I_C

[if $T\uparrow$, $I_{CO}\uparrow$, $I_C\uparrow$, $\frac{I_C R_E}{R_B+R_E}\uparrow$, $I_B\downarrow$, $I_C\downarrow$]

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_B+R_E}$$

$$S = \frac{1+\beta}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)}$$

$$S = \frac{1+\beta}{1-\beta\left(\frac{-R_E}{R_B+R_E}\right)} = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_B+R_E}\right)}$$

$$\therefore \boxed{S = (1+\beta)\,\frac{1+R_B/R_E}{1+\beta+R_B/R_E}}$$

→ Ratio of R_B/R_E controls the value of stability factor S

if $\frac{R_B}{R_E} \ll 1$ then $S = \frac{(1+\beta)(1+0)}{(1+\beta)+0} = \frac{1+\beta}{1+\beta} = 1$

→ To improve the stability of self bias circuit, R_B must be choosen that

$$\boxed{R_B \ll R_E}$$

$$\frac{\partial I_C}{\partial V_{BE}} = S' = \frac{-\beta}{R_B + (1+\beta) R_E}$$

$$\frac{\partial I_C}{\partial \beta} = S'' = \frac{S I_C}{\beta (1+\beta)}$$

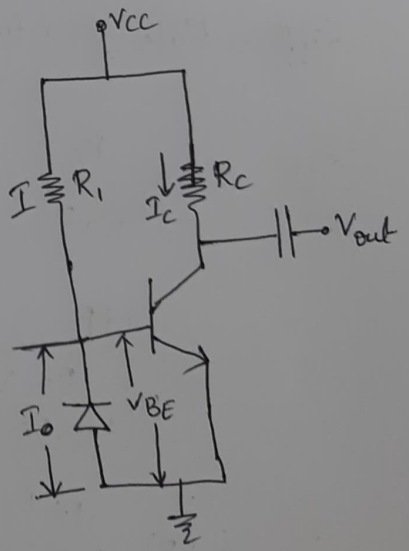
* Compensation techniques:

→ Compensation techniques use temperature sensitive devices such as diodes, transistors etc. to maintain operating point constant.

* Compensation against variation in I_{CO}:

→ Diode compensation techniques are commonly used for stabilizing transistors.

→ As shown in the circuit, diode is kept in reverse bias.



→ In reverse bias condition the current flowing through diode is only the leakage current (I_O).

→ If both diode & transistor are of same type & same material, when I_O ↑ses with temperature I_{CO} also ↑ses with the same rate.

$$I = \frac{V_{CC} - V_{BE}}{R_1} \quad \& \quad I = I_B + I_o$$

$$\Rightarrow I_B = I - I_o$$

as $V_{BE} = 0.2V$

$$I \approx \frac{V_{CC}}{R_1}$$

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

$$= \beta(I - I_o) + (1+\beta) I_{CO}$$

$$I_C = \beta I - \beta I_o + \beta I_{CO} \quad (\because \beta >> 1)$$

$$\Rightarrow I_C = \beta I \quad (\because I_o \approx I_{CO})$$

as I is constant, I_C remains fairly constant

* Thermistor compensation:

→ Thermistor is having negative temperature coefficient. Its resistance ↓ses expotentially with increasing temperature.

→ R_T is the thermistor, with ↑se in temp. R_T ↓ses.

Hence voltage drop also ↓ses (ie, base voltage).

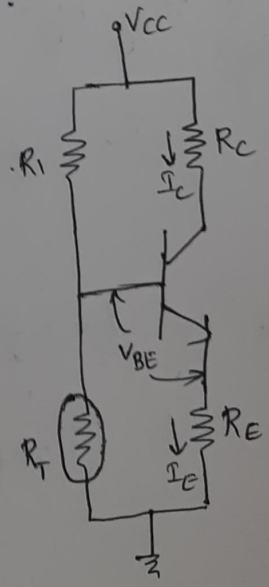
→ So, V_{BE} ↓ses which reduces I_B.

→ This behavior will tend to offset the ↑se in I_C

$$I_C = \beta I_B \downarrow + (1+\beta) I_{CO} \uparrow$$

↓

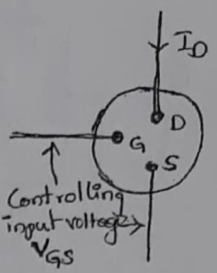
constant



* Field Effect Transistor (FET) :-

The field effect transistor abbreviated as FET is an another semi-conductor device like a BJT. Like BJT, FET is also a three terminal device, however, the principle of operation of FET is completely different from that of BJT. The three terminals of FET are named as Drain (D), source (S) and gate (G). Out of these three terminals gate acts as a controlling terminal.

→ **Voltage Controlled device.**



The voltage applied between gate and source V_{GS} controls the drain current I_D. Therefore, FET is a voltage controlled device. The name field effect is derived from the fact that the output current flow is controlled by an electric field setup in the device by an externally applied voltage.

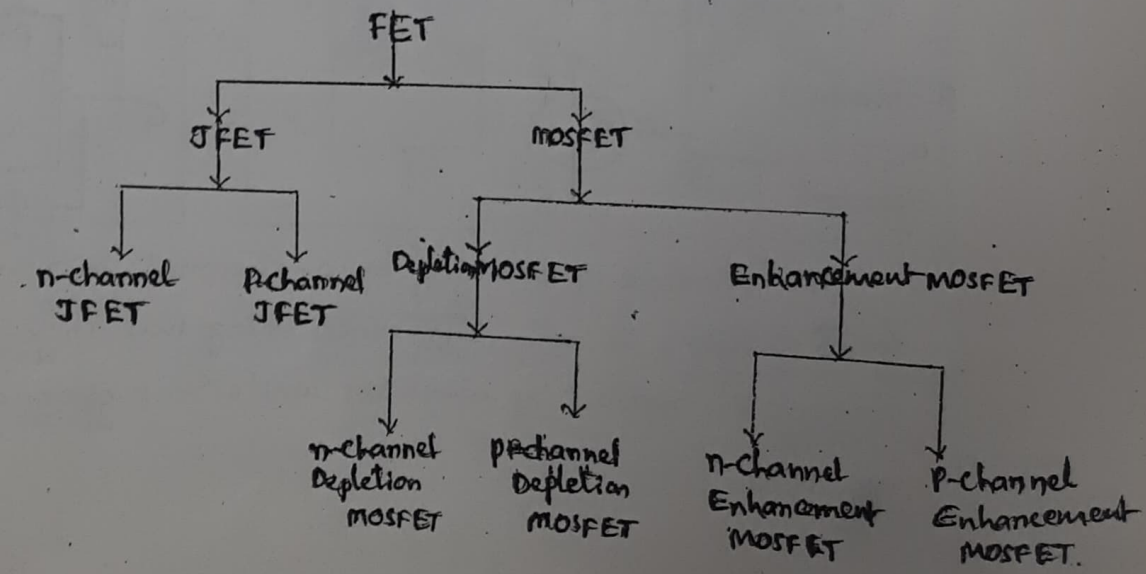
→ **Unipolar device.**

In FET, current is carried by only one type of charge particles, either electrons or holes. Hence FET is called Unipolar device.

→ **Other important features.**

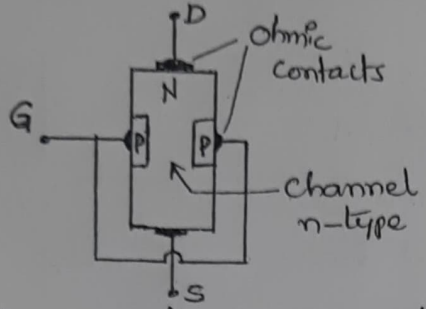
- FET is more temperature stable as compared to the BJT.
- FET has very high input impedance. FETs are preferred in amplifiers where high input impedance is required.
- FETs require less space than that for BJTs, hence they are preferred in integrated circuits.

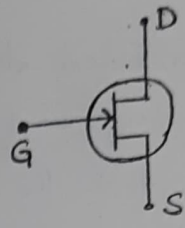
→ **The FETs are categorised as**



* Structure of n-channel JFET :-

A small bar of extrinsic semiconductor material, n-type is taken and at its two ends, two ohmic contacts are made which are the drain(D) and source (S) terminals of FET. Heavily doped electrodes of p-type material form p-n junctions on each side of the bar. The thin region between the two p-gates is called the channel. Since this channel is the n-type bar, the FET is known as n-channel JFET.





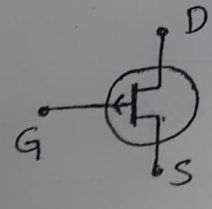
N-channel JFET Symbol

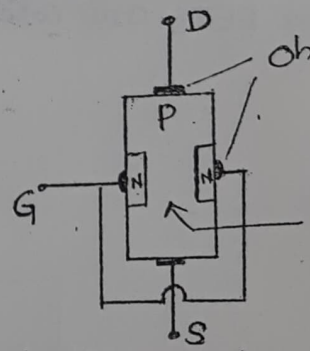
The es enter the channel through the terminal called source and leave through the terminal called drain. The terminals taken out from heavily doped electrodes of p-type material are called gates. Usually these electrodes are connected together and only one terminal is taken which is called gate.

* Structure of p-channel JFET :-

A small bar of p-type semi-conductor is taken and at its two ends, two ohmic contacts are made which are the drain(D) and source terminals of JFET. Heavily doped electrodes of n-type material form p-n junctions on each side of the bar. The thin region between the two n-gates is called the channel. Since this channal is the p-type, the FE is known as p-channel JFET.

p-channel JFET Symbol

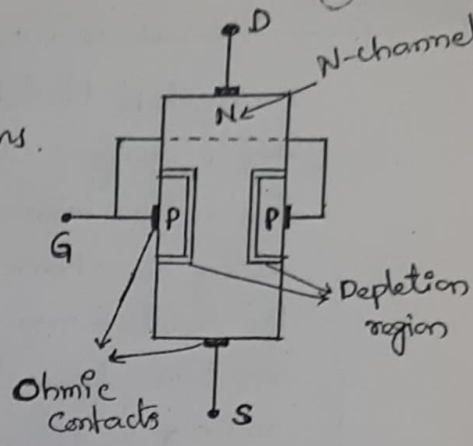




The principle of working of n-channel JFET and p-channel JFE is similar, the only difference being that in n-channel JFET the current is carried by electrons while in p-channel JFET, it is carri by holes.

* Unbiased JFET.

In the absence of any applied voltage, JFET has gate channel junctions under no bias conditions. The result is a depletion region at each junction. This represents same depletion region of a diode under no bias conditions. Therefore is unable to support conduction through the region.



* Principle of Operation of JFET :-

In JFET, the p-n junction between gate and source is always kept in reverse biased conditions. Since the current in a reverse biased p-n junction is extremely small, practically zero; the gate current in JFET is often neglected and assumed to be zero.

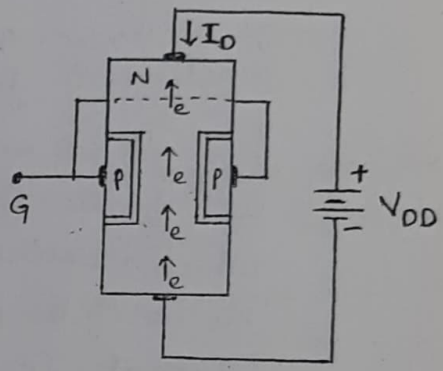
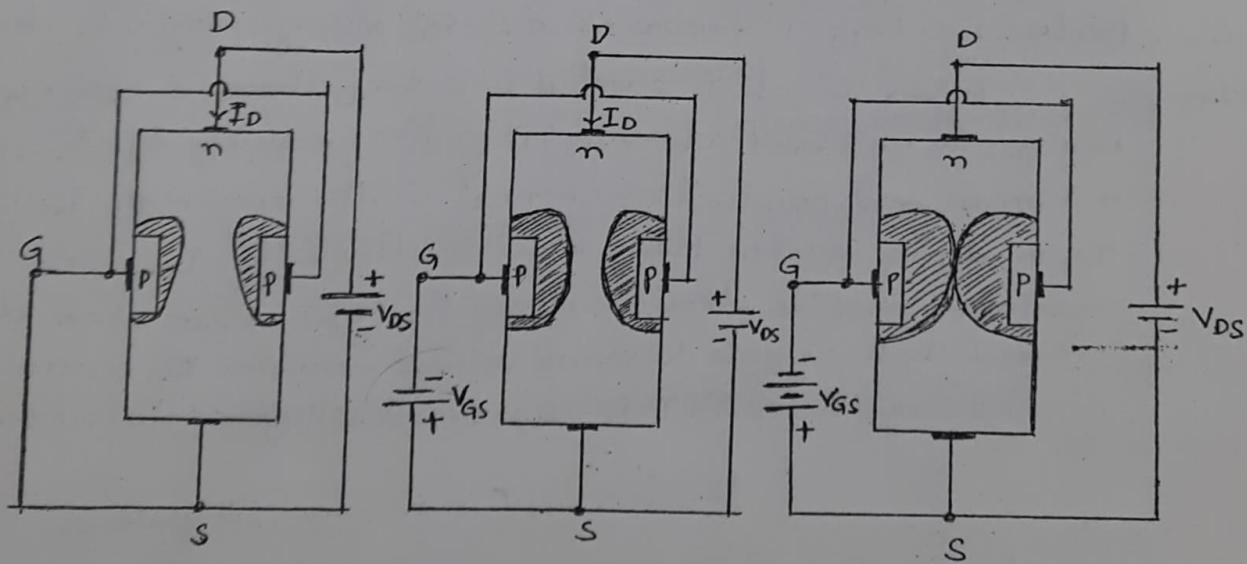


figure-1

Let us consider the circuit as shown in figure-1. The voltage V_{DD} is applied between Drain and Source, Gate terminal is kept open. The bar is of n-type. Due to the polarities of applied voltage, the majority carriers i.e the electrons start flowing from the source to the drain this flow of es makes the drain current I_D. the majority carriers move from source to drain through the space between the gates regions, known as channel.



No bias voltage on gate

Figure-2.

Small negative gate-source voltage

Figure-3.

Large negative gate-source voltage

Figure-4.

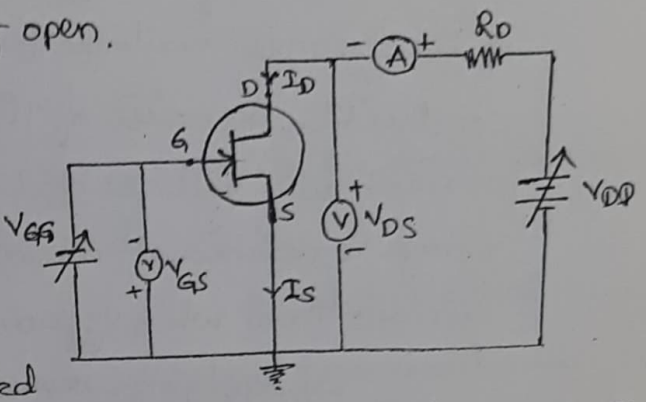
Let us now consider an n-channel JFET with the gate directly connected to the source terminal. When drain voltage V_{DS} is applied, a drain current I_D flows in the direction as shown in the figure-2. Since the n-type material is resistive, the drain current causes a voltage drop along the channel. This voltage drop reverse biases the p-n junctions, and causes the depletion regions to penetrate into the channel. Since gate is heavily doped and the channel is lightly doped, the width of the depletion region will mainly be spread in the channel. Looking at the figure-2 we can observe that depletion region width is more at the drain side as compared to source side because near the junction, voltage at drain side is more than the voltage at the source side. This shows that reverse bias is not uniform near the junction, it gradually increases from source to drain side.

If we externally apply reverse bias voltage to the gate, the reverse bias will further increase and hence increase the penetration of the depletion region which reduces the width of the channel. As width of the channel reduces, the no of $\bar{e}$s flowing from source to drain reduces and hence the drain current. If we go on increasing the reverse bias voltage to the gate as shown in the figures-3 & 4, depletion regions will increase more and more, and a stage will come when the widths of the depletion regions will be equal to the original width of the channel, leaving zero width for conducting. This will prevent any current flow from source to drain and this will cut off the drain current. The gate to source voltage that produces cutoff is known as cut-off voltage and it is denoted by $V_{GS(off)}$

When the gate is shorted to source, there is minimum reverse bias between the gate and source p-n junction, making depletion region width minimum and conducting channel width maximum. In this case maximum drain current flows which is denoted by I_{DSS} and this is the maximum possible drain current in JFET. From above discussion it cleared that the gate to source voltage controlles the current flowing through channel and hence JFET is also called voltage controlled current source

Drain V-I Characteristics for n-channel JFET:

The circuit shows the experimental setup required to plot the drain characteristics.



(1) V_{GS} & V_{DS} both = 0:

When $V_{GS}=0$ the channel is entirely open. But $V_{DS}=0$, so there is no force for the majority carriers and hence drain current does not flow.

(2) $V_{GS}=0$, $V_{DS}\neq 0$:

At $V_{GS}=0$, in response to a small applied voltage V_{DS}, the n-type bar acts as a simple semiconductor resistor, and the current I_D increases linearly with V_{DS}. As V_{DS} increases, the voltage drop along the channel also increases. This increases the reverse bias on gate-source junction and causes the depletion regions to penetrate into the channel, reducing channel width. The effect of reduction in channel width provides more opposition to increase in drain current I_D. Thus, rate of increase in I_D w.r.t V_{DS} is now reduced.

At some value of V_{DS}, drain current I_D can not be increased further due to reduction in channel width. I_D approaches the constant saturation value. The voltage V_{DS} at which the current I_D reaches to its constant saturation level is called 'Pinch-off voltage' (**Self-Pinch-off voltage** because here $V_{GS}=0$)

The pinch off voltage V_p is given by

$$V_p = \frac{2N_D}{2\epsilon} a^2$$

ϵ – Dielectric constant of channel material ($\epsilon_0 = 8.849\times10^{-12}$ F/m; for silicon $\epsilon = 12\epsilon_0$)

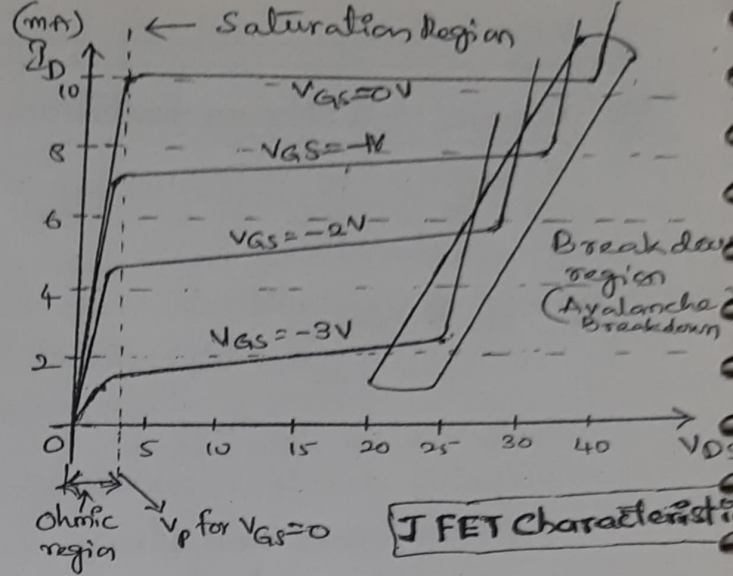
a – Half the region of n-type material without considering channel width (conducting portion)

N_D – Concentration of donar atoms

q – Electronic charge $= 1.6\times10^{-19}$ C.

(3) V_{GS} with negative bias :-

When an external bias, of say -1V, is applied between gate and source, the gate junctions are further reverse biased, reducing the effective width of the channel available for the conduction. Because of this, drain current will reduce and pinch-off voltage is reached at a lower drain current than when $V_{GS}=0$



By applying several values of negative voltages V_{GS}, a family of curves are obtained as shown in the figure. It can be observed that for more negative values of V_{GS}, the pinch-off is reached at lesser values of

The V_{GS} is given by $V_{GS}=\left(1-\frac{b}{a}\right)^2 V_p$, where b - half-channel wid (effective channel

(4) Breakdown region:

We can observe from the characteristics that if we increase valu of V_{DS} beyond pinch-off voltage V_p, the drain current I_D remains consta upto certain value of V_{DS}. If we further exceed V_{DS}, the voltage will b reached at which the gate-channel junction breaks down, due to avalanche effect. At this point the drain current increases very rapidl and the device may be destroyed.

It can be observed that the values of V_{DS} for breakdown are reduced as the negative gate voltage is increased. This is because the total reverse breakdown voltage is the addition of the reverse voltage due to self-pinch off and the externally applied voltage V_{GS}.

(5) **Ohmic** and **Saturation regions** :- It is seen that the drain characteristic of JFET is divided into two regions ① ohmic region and ② saturation regio. In the **Ohmic region**, the drain current I_D varies with V_{DS} and the JFET is said to behave as voltage variable resistance. In the **Saturation region**, the drain current I_D remains fairly constant and does not vary with V_{DS}. Saturation in a FET refers to the no of carriers that can be transported through the channel per unit time is limited or saturated and I_D remain constant.

⑥ **Cut-off**: for an n-channel JFET, the more negative V_{GS} causes drain current to reduce and pinch off voltage to reach at a lower drain current. When V_{GS} is made sufficiently negative, I_D is reduced to 0. This is caused by the widening of the depletion region to a point where it completely closes the channel. The value of V_{GS} at the cut-off is designated as $V_{GS(off)}$.

*NOTE: Do not confuse cut-off with pinch-off.

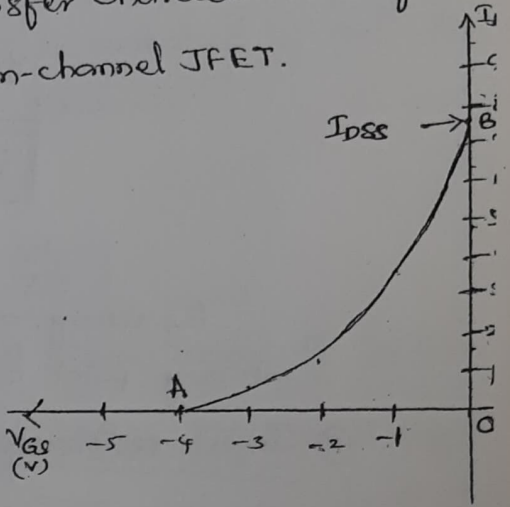
1) The pinch-off voltage V_p is the voltage value + V_{DS} at which the drain current I_D reaches a constant value for a given value of V_{GS}

2) The cut-off voltage $V_{GS(off)}$ is the value of V_{GS} at which the drain current is 0. I_D is 0 only when magnitude of V_{GS} is equal to or greater than the magnitude of V_p. $\boxed{I_D \text{ is zero when } V_{GS} = -V_p}$

*** TRANSFER CHARACTERISTICS FOR N-CHANNEL JFET

The curves represents relationship between the drain current I_D and gate-to-source voltage V_{GS} are known as transfer characteristics of JFE

The figure shows the transfer characteristics of n-channel JFET.



for this characteristics we observe following points:

① The relationship between the drain current I_D and gate-source voltage V_{GS} is non-linear. This is defined by shockley's equation

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2}$$

we can also write $V_{GS} = V_p\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$

② A point 'A' at the bottom end of the curve on the V_{GS}-axis represents $V_{GS(off)}$ and point 'B' at the top end of the curve on the I_D-axis represents I_{DSS}. Thus, this curve shows the operating limits of a JFET. These are:

$I_D = 0$ when $V_{GS} = V_{GS(off)}$

$I_D = I_{DSS}$ when $V_{GS} = 0$.

✱✱ JFET Parameters:

The important parameters of JFET are as follows:

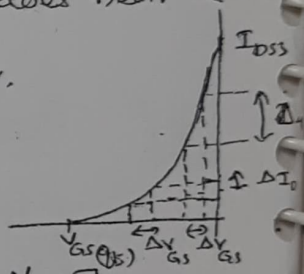
① Transconductance (g_m) ② Input resistance (R_{in})

③ Drain to source resistance (r_d) ④ Amplification factor (μ)

① **Transconductance (g_m):-** It is the change in the drain current for a given change in gate-source voltage with the drain-source voltage constant. It is also called as mutual conductance.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}\Big|_{V_{DS}\text{-const}}$$

from the transfer characteristics, we can say that it is the slope of the transfer characteristics. Since the slope varies, g_m also varies. g_m has a greater value near the top of the curve than it does near the bottom. The practical unit for g_m is millisiemen (mS) or mA/V.



we know that $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$.

Differentiating this eqn w.r.t V_{GS} we get,

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = I_{DSS} \cdot 2\left[1 - \frac{V_{GS}}{V_p}\right] \cdot \frac{-1}{V_p} = \frac{-2I_{DSS}}{V_p}\left[1 - \frac{V_{GS}}{V_p}\right]$$

$$\boxed{g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_p}\right)} \text{ or } \boxed{g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]}$$

where $g_{m0} = \frac{-2I_{DSS}}{V_p}$

By using above eqn we can calculate an approximate value for g_m at any point on the transfer characteristics curve.

② **Input resistance:** JFET operates with its gate-source junction reverse-biased. Therefore the input resistance at the gate is very high. The input resistance can be determined using the following eqn, where the vertical lines indicates an absolute value

$$R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$$

I_{GSS} – Reverse gate current. V_{GS} – Gate to source voltage.

③ Drain to source resistance (r_d):- From the drain characteristics Drain resistance r_d can be calculated. The drain resistance is the a.c resistance between drain and source terminals when the JFET is operating in the saturation region. It is the reciprocal of the slope of the drain-characteristic in the saturation region

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\Big|_{V_{GS}\text{-constant}}$$

④ Amplification factor (μ): It is defined as the ratio between drain source voltage to the gate-source voltage.

$$\text{Amplification factor } \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}\Big|_{I_D\text{-const}}$$

$$\therefore \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}} = r_d \cdot g_m$$

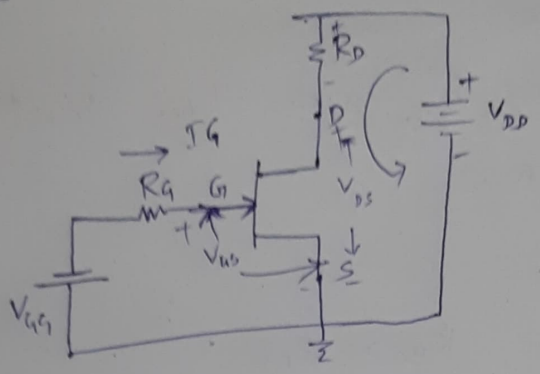
$$\boxed{\mu = r_d \cdot g_m}$$

** COMPARISON OF TRANSISTORS :-

Comparison of BJT and FET.

S.No	Parameter	BJT	JFET
1	Device type	Bipolar	Unipolar
2	Control element	current controlled device	voltage controlled device.
3	Types	n-p-n & p-n-p.	n-channel & p-channel.
*	configurations	CB, CE, CC	CS, CG, CD.
5	Input resistance	less compared to JFET	high compared to BJT
6	Size	Bigger than JFET	smaller in Construction.
7	Sensitivity	Higher sensitivity to changes in the applied signals	Less sensitivity to changes in the applied voltage.
8	Thermal runaway	Exists in BJT	Does not exists in JFET.
9	Gain factor	$\beta = \frac{\Delta I_C}{\Delta I_B}$	$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$
10	Gain bandwidth Product	High	low.

1) Fixed bias



I_{DSS}

V_P

$I_G = \frac{V_{DD} - }{R_G}$

$-V_{GG} - V_{GS} = 0$

$V_{GS} = -V_{GG}$

$V_{DD} - I_D R_D - V_{DS} = 0$

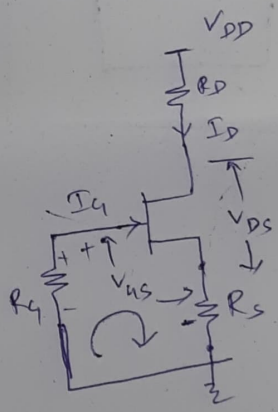
$V_{DS} = V_{DD} - I_D R_D$

$V_{DS} \geq |V_P| - |V_{GS}|$

$-V_{GG} - I_G R_G - V_{GS} = 0$

$V_{GG} = -V_{GS}$

$V_{GS} = -V_{GG}$



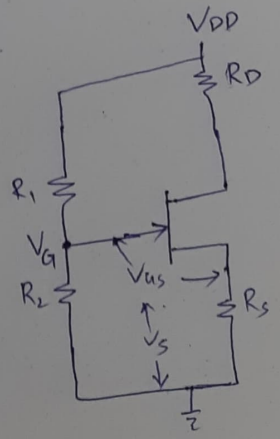
2) Source self bias

$V_S = I_D R_S$

$V_{GS} = V_G - V_S$

$= 0 - I_D R_S$

$V_{GS} = -I_D R_S$



3) Voltage divider bias

R_1, R_2 provides biasing

$V_G = \frac{R_1}{R_1 + R_2} V_{DD}$

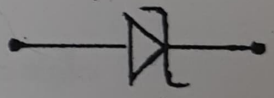
$V_S = I_D R_S$

$V_G = V_{GS} + V_S \Rightarrow V_{GS} = V_G - V_S$

$V_{GS} = V_G - I_D R_S$

ZENER DIODE :- The zener diode is a silicon p-n junction diode except that it is properly doped to have a very sharp and almost vertical breakdown. They are exclusively operated under reverse biased conditions and designed to operate in breakdown region.

Zener diode is a heavily doped p-n junction diode



for heavily doped diodes, the depletion region is very narrow. When the reverse bias across the diode is increased, breaking of covalent bonds takes place by the intense electric field ($\approx 10^8$ V/m) set up across the depletion layer. It produces a large no of e-hole pairs resulting in a sharp increase in reverse current.

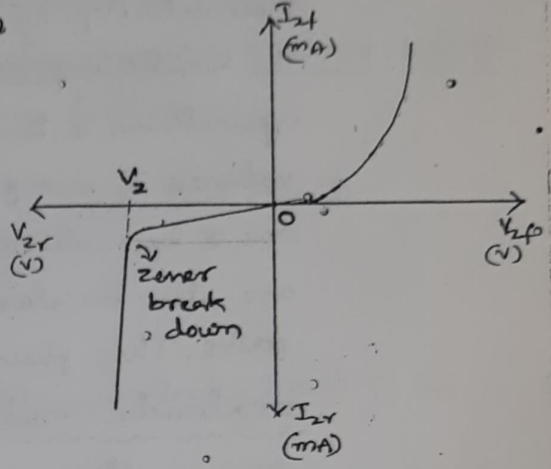
→ Applications of zener diode :-

① As a voltage regulating element in voltage regulators
② Used in various protection circuits
③ In limiter circuits.

→ Characteristics of zener diode

In the forward biased condition, the normal pn diode and the zener diode operate in similar fashion

In the reverse biased condition, the zener diode carries reverse saturation current till the reverse voltage applied is less than the reverse breakdown voltage. When the reverse voltage exceeds breakdown voltage, the current through it changes drastically but the voltage across it remains almost constant. Such a breakdown region is a normal operating region for a zener diode.

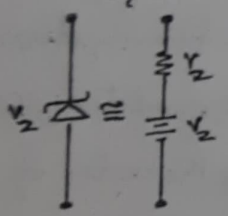


When the reverse voltage to a zener diode is increased, initially the current through it is very small, of the order of few μA. This is the reverse leakage current (reverse saturation current). At a certain reverse voltage, current through zener diode increases rapidly. The change from a low value to large value of current is very sharp and well defined. This voltage is called zener breakdown voltage (zener voltage) V_z.

$$r_z = \frac{\Delta V_z}{\Delta I_z}$$

NOTE:-

Zener diode & equivalent circuit



Dynamic resistance

$$r_z = \frac{1}{\text{slope}} = \frac{1}{\Delta I_z / \Delta V_z}$$

BREAKDOWN MECHANISMS :-

① Avalanche Breakdown:- The applied reverse bias causes a small reverse current I_o to flow in the diode. This is due to movement of minority charge particles. The polarity of reverse bias voltage is such that only the minority carriers are able to cross the junction. As the applied reverse bias voltage becomes larger, the minority carriers increasingly accelerate.

there are collisions between these carriers and $\bar{e}$s involved in the covalent-bonds of the crystal structure.

If the applied voltage is such that the travelling $\bar{e}$s do not have high velocity, then the collisions take some energy away from them, altering their velocity. If the applied voltage is increased, the velocity and hence the kinetic energy ($K.E = \frac{1}{2}mv^2$) of $\bar{e}$ increased. If such an $\bar{e}$ dashes against an $\bar{e}$ involved in covalent bond, then the collision gives bound-valence $\bar{e}$ enough energy to enable it to break its covalent bond. Thus, one $\bar{e}$ by collision creates an $\bar{e}$-hole pair. These secondary particles are also accelerated and participate in collisions that generate new pairs. This phenomenon is known as carrier-multiplication or avalanche-multiplication or self-sustained multiplication. At this stage junction is said to be in breakdown and current starts increasing rapidly.

Key points:- ① The diodes having reverse breakdown voltage greater than 6V, show the avalanche breakdown mechanism. The avalanche breakdown occurs for lightly doped diodes.

② → The breakdown voltage increases as the temp increases for avalanche breakdown. (Avalanche breakdown has positive temp coefficient).

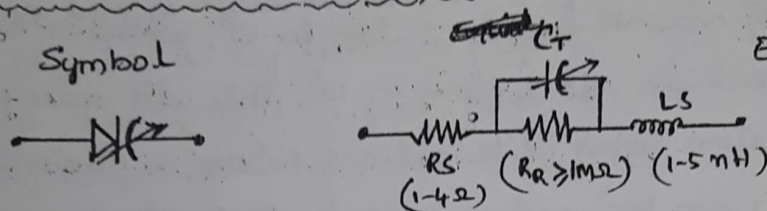
③ → The excessively high temp destroys the junction permanently at higher reverse voltages.

⇒ ② Zener breakdown :- When a p-n junction is heavily doped the depletion region is very narrow. So under reverse bias condition, the electric field across the depletion layer is very intense, of the order of 10^8 V/m or 10^6 V/cm such an intense field is enough to pull the $\bar{e}$s out of the valence bands of the stable atoms. So this is not due to the collision of carriers with atoms. Such a creation of carriers is called zener effect which is different than the avalanche effect. These minority carriers constitute very large current and mechanism is called zener breakdown.

Key points: ① The diodes having reverse breakdown voltage less than 6V shows the zener breakdown mechanism. This occurs for heavily doped diodes

② The breakdown voltage decreases as the temp increases for zener breakdown.

* **VARACTOR DIODE:-** As the transition capacitance varies with the applied voltage, it can be used as a voltage variable capacitance in many applications. In practice, special type of diodes are manufactured which show the transition capacitance property more predominantly as compared to the normal diodes. Such diodes are called varactor diodes, varicap, voltage-variable capacitance (VVC) diodes or tuning diodes.



The above figure shows the symbol and its equivalent circuit in the reverse biased condition.

R_R is the reverse resistance which is very large, while R_S is the geometric resistance of diode which is very small. The series inductance Ls indicates that there is a high frequency limit associated with the use of varactor diode.

→ Expression for capacitance:-

$$C_T = \frac{k}{(V_j + V_R)^n}$$

where k – constant depends on semiconductor material and construction technique (not a boltzmann's constant)

V_j – junction potential (barrier potential)

V_R – magnetude of reverse applied voltage.

n – $\frac{1}{2}$ for alloy junctions

– $\frac{1}{3}$ for semiconductor junctions (diffused junctions).

* → **Applications:-** the various applications of varactor diodes are, in

① Tuned circuits (as electrical tuner),
② Automatic frequency controlled devices,
③ Adjustable bandpass filters,
④ Television, Radio receivers,
⑤ FM modulators, ⑥ Parametric amplifiers, etc.

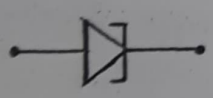
TUNNEL DIODE:—

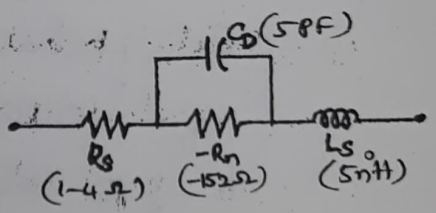
The tunnel diode was first introduced by Leo Esaki in 1958. Its characteristics are different from any diode, it has negative resistance region. In this region, an increase in terminal voltage results in a reduction in the diode current.

The tunnel diode is fabricated by doping the semiconductor material that will form the p-n junction at a level one hundred to several thousand times that of ordinary semiconductor diode. For normal diode impurity concentration is 1 atom in 10^8, while in the tunnel diode impurity concentration is 1 atom in 10^3. This will results in a greatly reduced depletion region, of the order of 10^{-6} cm, or typically about $\frac{1}{100}$ the width of this region for a normal diode. It is this thin depletion region that many carriers can tunnel through, rather than attempt to surmount, at low forward bias potentials.

We know that, a particle must have an energy at least equal to the height of a potential energy barrier, if it is to move from one side of the barrier to the other. However, for barriers as thin as those in diodes introduced by Esaki, the schrodinger wave equation indicates that there is a large probability that an $\bar{e}$ (Here $\bar{e}$ has energy less than the barrier height) will penetrate through the barrier. This Quantum-Mechanical behaviour is referred as tunneling, and hence these high impurity density p-n junction devices are called tunnel diodes.

→ Symbol & Equivalent circuit.





$-R_n$ – The negative resistance.

R_s – The series resistance, due to Ohmic contacts.

L_S – The series inductance, it depends on the lead lengths and the geometry of the diode package.

→ Advantages of tunnel diode:-

① Low cost,
② Low noise,
③ Low power consumption,
④ Environmental immunity ⇒ i.e the peak point is not a temperature sensitive function,
⑤ High speed

* The only disadvantage of this diode is, being two terminal device, there is no isolation between input and output.

ENERGY BAND STRUCTURE OF TUNNEL DIODE :—

We have seen that in the energy band structure for the lightly doped diode, the fermi level E_f lies inside the forbidden gap.

We know that

$$E_f = E_c - kT\log_e\left(\frac{N_c}{N_D}\right) \longrightarrow \text{for n-type}$$

for a lightly doped semiconductor $N_D < N_c$, so the log term is a positive, Hence $E_f < E_c$, and the fermi level lies inside the forbidden band. for highly doped semiconductors $N_D > N_c$ and log term is negative,

$$E_f = E_c - \left[-kT\log_e\left(\frac{N_c}{N_D}\right)\right] \Rightarrow E_f = E_c + kT\log_e\left(\frac{N_c}{N_D}\right)$$

Hence $E_f > E_c$, and the fermi level lies out side the forbidden band i.e in the conduction band. for the similar reason, for heavily doped 'p' region $N_A > N_v$, and the fermi-level lies in the valence band

$$\left[E_f = E_v + \left(-kT\log_e\frac{N_v}{N_A}\right) \Rightarrow E_f = E_v - kT\log_e\left(\frac{N_v}{N_A}\right)\right]$$

We know the energy gap $E_g = kT\log_e\frac{N_cN_v}{n_i^2} = V_T\log_e\frac{N_cN_v}{n_i^2}$

and potential barrier energy $E_0 = V_T\log_e\frac{N_AN_D}{n_i^2}$

When we compare the above two eqns for heavily doped p-n diode we find that $E_0 > E_g$. Hence, at open circuit condition the band structure for heavily doped p-n junction (Tunnel) diode is as shown in the above figure. Here the fermi-level in the p-side is at the same energy as the fermi-level in the n-side. Hence, at open circuit, there can be no flow of charge in either direction across the junction, and the current is zero.

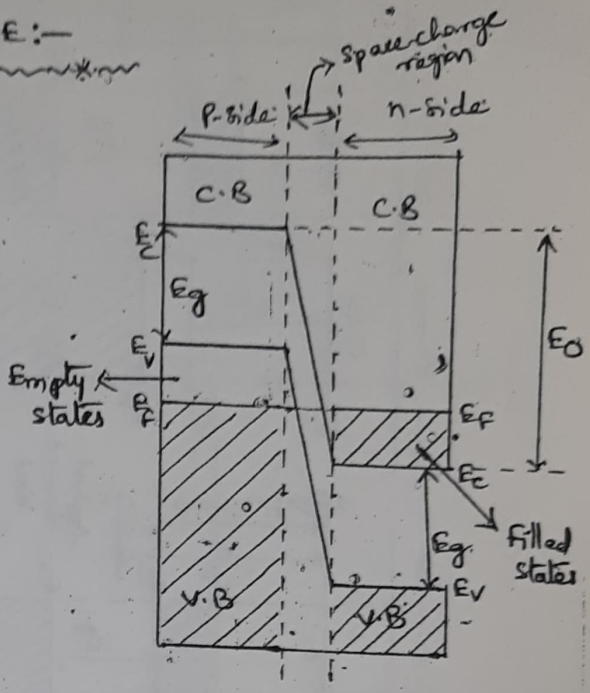


figure 1

When reverse biase is applied, the height of the barrier is increased above the open circuit value E_0. Hence the n-side levels must (i.e E_c) shift downwards with respect to the p-side levels (i.e E_c on p-side). Now we can notice that there are some energy states (Portion in crossed lines on p-side) in the valence band of the p-side which lie at the same level as allowed empty states in the conduction band of the n-side. Hence these es will tunnel from p-side (crossed portion) to the n-side, giving rise to a

Under reverse bias

figure 2

Under forward bias

figure 3

At peak point
Under forward bias

figure 4

At valley point
Under forward bias.

figure 5

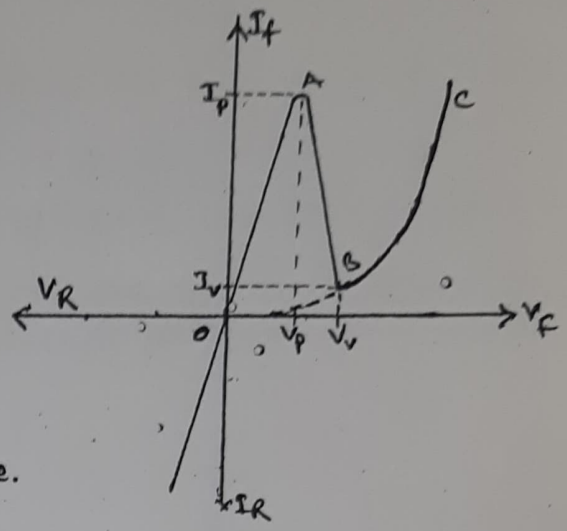
reverse current. As, the reverse bias increases, the crossed portion increases, causing the reverse current to increase

When forward bias is applied the barrier height decreases. Hence the n-side levels must shift upward with respect to those on the p-side. This is illustrated in the figure 3. Now, there are occupied states in the conduction band of the n-side (crossed area) which are at the same energy as allowed empty states in the valence band of the p-side. Hence es will tunnel from the n-side to the p-side, giving rise to the forward current.

As the forward bias is increased further, n-side shifts farther upward as shown in the figure 4. In this situation the maximum no of es can leave occupied states on n-side, giving rise to the peak current Ip. If still more forward bias is applied the situation shown in figure 5 exists and tunneling current decreases, finally the tunneling current drops to zero.

As the forward bias is increased further, barrier height decreases to zero ~~and~~. Now majority carriers enter into the picture and forward current increases exponentially as the in normal p-n diode.

* Characteristics of a Tunnel diode:-



The shape of the V-I characteristics curve of a tunnel diode is quite different from that of a normal diode.

When a reverse bias voltage is applied to a tunnel diode, it conducts. It is on account of the heavy doping. The diode appears to be broken down for any reverse voltage.

As soon as a forward bias is applied, the tunnel diode passes a considerable current which quickly reaches to its peak value I_p at a low voltage (peak voltage) V_p, i.e OA region and A is peak point. As the applied voltage is increased, diode current starts decreasing and achieves a minimum value I_v (valley current) corresponding to valley voltage V_v i.e point B (valley point). When the ~~valley~~ forward voltage is further increased beyond the valley point, the current increases again as in any conventional junction diode.

→ Applications of tunnel diode:-

1. As a high speed switch due to its switching time is very low (n sec to p sec)
2. In pulse and digital circuits
3. As a sinusoidal oscillator
4. In high frequency (microwave) oscillator (in negative resistance)
5. In switching networks
6. In timing and computer logic circuits
7. In amplifiers.

7.8 The Unijunction Transistor (UJT):

7.8.1 Introduction

A Unijunction transistor is a three terminal semiconductor switching device. This device has only one of its kind characteristic that when it is triggered, their emitter current increase re-generatively (because of negative resistance characteristic) until it is constrained by emitter power supply. The low price per unit, combined with its distinctive characteristic, has warranted its use in a large range of applications. A few include oscillators, pulse generators, saw-tooth generators, triggering circuits, phase control, timing circuits, and voltage-or current-regulated supplies. The device is in most cases, a low-power-absorbing device under typical working conditions and provides wonderful support in the continual effort to design fairly efficient systems.

7.8.2 Construction of a UJT

The basic structure of a unijunction transistor is shown in figure 7.10. It basically consists of a lightly-doped N-type silicon slab with a small piece of heavily doped P-type material alloyed to its one side to produce single P-N junction. The single P-N junction accounts for the terminology unijunction. The silicon slab, at its ends, has two ohmic contacts are denoted as base-1 (B_1) and base-2 (B_2), as shown and the P-type region is termed the emitter (E). The emitter junction is generally situated closer to base-2 (B_2) than base-1 (B_1), accordingly, that the device is not symmetrical, because symmetrical unit does not provide optimum electrical characteristics for most of the applications.

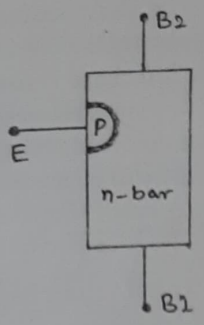


Figure: 7.10

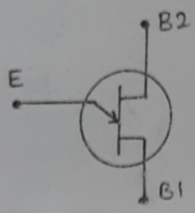


Figure: 7.11

UJT Symbol

The symbol for unijunction transistor is shown in figure 7.11. The emitter lead is drawn at an angle to the vertical line representing the N-type material slab and the arrowhead points in the direction of conventional current when the device is forward-biased, active or in the conducting state.

The following points are worth noting about UJT:

- The device has only one junction; hence it is called the unijunction device.
- The device, as a result of one P-N junction, is quite similar to a diode but it differs from regular diode as it has three terminals.
- The structure of a UJT is quite similar to that of an N-channel JFET. The key difference is that P-type (gate) material surrounds the N-type (channel) material in case of JFET and the gate surface of the JFET is much larger than emitter junction of UJT.
- In a unijunction transistor the emitter is heavily doped while the N-region is lightly doped, so the resistance between the base terminals is relatively high, typically 4 to 10 KΩ when the emitter is open.
- The N-type silicon bar has a high resistance and the resistance between emitter and base-1 is larger than that between emitter and base-2. It is because emitter is closer to base-2 than base-1.
- UJT is operated with emitter junction forward-biased whereas the JFET is normally operated with the gate junction reverse-biased.

- UJT does not have ability to amplify but it has the ability to control a large ac power with small signal. It exhibits a negative resistance characteristic and so it can be employed as a oscillator.

7.8.3 Equivalent circuit of UJT:

Figure shows the equivalent circuit of a UJT. The point A denotes the point where p-n junction is formed. The point A is such that $R_{B_1} > R_{B_2}$ where R_{B_1} and R_{B_2} denote the resistance of the silicon bar between B1 and A, and between A and B2 respectively.

Usually

$$R_{B_1} = 60\% \text{ of } R_{BB}$$

Where $R_{BB} = R_{B_1} + R_{B_2}$

is the resistance between B2 and B1 i.e. the total resistance of the bar from one end to the other and is known as the **interbase resistance** and is denoted by R_{BB}.

It may be seen that emitter acts as a voltage divider tap on the fixed resistance R_{BB}. The voltage division factor is called **intrinsic stand-off ratio** and is denoted by η. It is given by $\eta = \dfrac{R_{B_1}}{R_{B_1} + R_{B_2}} = \dfrac{R_{B_1}}{R_{BB}}$ when $I_E = 0$.

The typical value range of η is from 0.5 to 0.8.

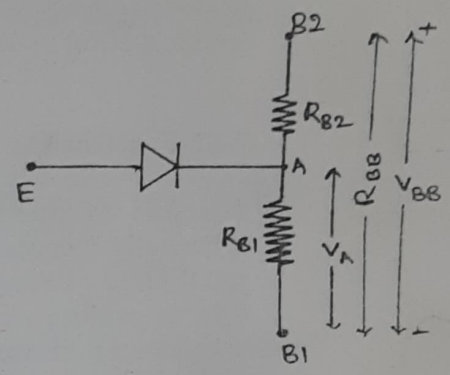


Figure: 7·12

7.8.4 Operation of UJT

The device has normally base B2 positive w.r.t base B1 i.e. B1 is grounded and a positive voltage V_{BB} is applied at B2. If voltage V_{BB} is applied between B2 and B1 with emitter open. Voltage gradient is established along the n type bar since emitter is located nearer to B2 more than half of VBB appears between the emitter and B1. The voltage V_A between emitter and B1 establishes a reverse bias on the p-n junction and the emitter current is cut off. A small leakage current, I_{EO} flows from B2 to emitter due to minority carriers.

If a positive voltage is applied at the emitter the p-n junction will remain reverse biased so long as the input voltage is less than V_A or $V_P(= \eta V_{BB})$, if the input voltage to the emitter exceeds V_A the p-n junction becomes forward biased. Under these conditions holes are injected from the p type material into the n type bar these holes are repelled by positive B2 terminal and they are attracted towards B1 terminal of the bar. This accumulation of holes in the emitter to B1 region results in the ~~degrees~~ decrease of resistance in this section of the bar the internal voltage drop from emitter to B1 is decreased hence emitter current I_E increases as more holes are injected a condition of saturation will eventually be reached at this point a emitter current limited by emitter power supply only. The device is in on state.

If a negative pulse is applied to the emitter, the p-n junction is reverse biased and the emitter current is cut off. The device is said to be off state.

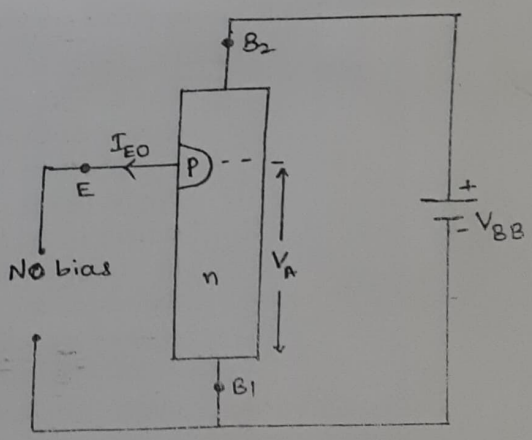


Figure 7·13(A)

* (PTO)

7.8.5 Characteristics of UJT

The curve between emitter voltage V_E and emitter current I_E of a UJT at a given voltage V_{BB} is known as emitter characteristics of UJT. Referring to figures 7.13(A) and 7.13(B) when V_{BB} is applied between the two bases with emitter terminal open, a voltage gradient is developed along the n-type bar. This voltage reverse biases the p-n junction and UJT is cut off. But a small leakage current I_{EO} flows from base B2 to emitter due to minority carriers. Now let the emitter voltage V_E be slowly increased, when V_E becomes equal to $V_A = \eta V_{BB}$, I_{EO} will be reduced to zero. When emitter voltage is increased, the diode becomes forward biased as soon as it exceeds the total reverse bias voltage $\eta V_{BB} + V_B$. This emitter voltage increases up to a certain point V_P is reached. This value of emitter voltage $V_P = V_E$ is called the ***peak point voltage*** when $V_P = V_E$ the emitter current I_E ($= I_P$) starts to flow through R_{B1} to base B corresponding to the peak point voltage. This is the minimum current (I_E) that is required to trigger the UJT is called ***peak point current*** I_P. The region below peak point current is known as ***cut off region***. This is the high impedance off state.

Behind the peak point value of emitter voltage V_P an attempt to increase V_E is followed by a sudden increase in the emitter current I_E with decrease in V_E consequently the bar resistance decreases. This portion of the characteristic curve is known as ***negative resistance region***. This negative portion of the curve lasts untill the valley point is reached with ***valley point voltage*** V_V and corresponding ***valley current*** I_V. After the valley point the UJT is driven to saturation. The region between the peak point and the valley point is known as ***negative resistance region***. After the valley point, now, the device is in the ON state. The region above the valley point is called the ***saturation region***. This region is similar to that of a semiconductor diode characteristic curve. Figure 7.14 shows the typical emitter characteristics of a UJT.

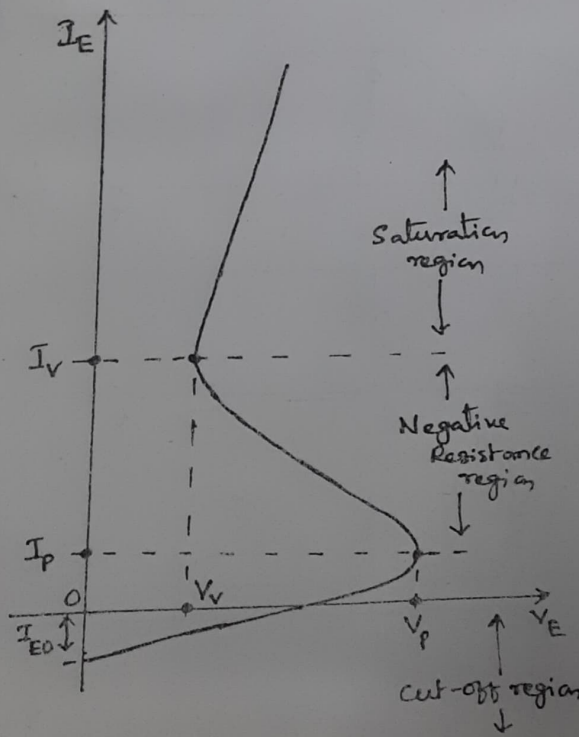


Figure 7.14

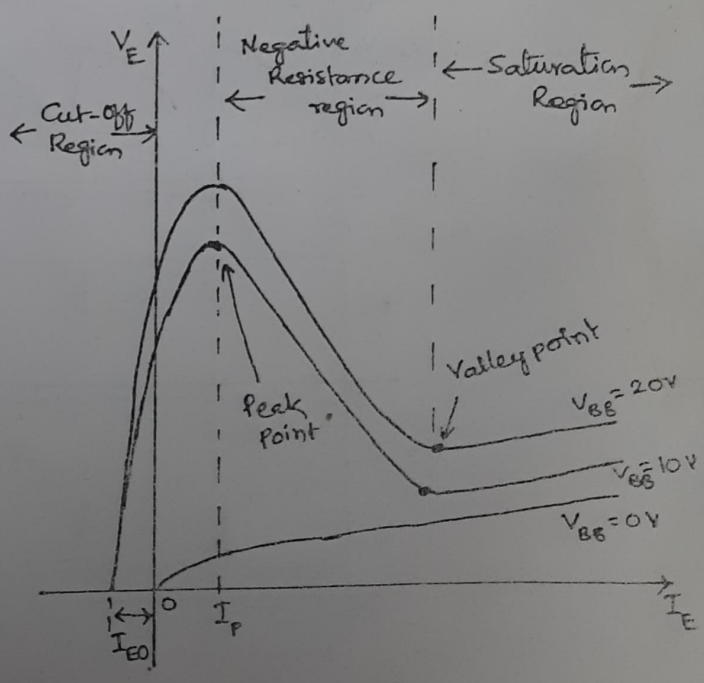


Figure 7.15

Figure 7.15 shows the family of typical emitter characteristic curves of a UJT for various values of V_{BB}. It may be observed that the peak point voltage V_P increases steadily with in increasing V_{BB} and so does the valley point voltage V_V at which the curve has its lowest value. This switching efficiency of UJT is the difference V_P-V_V and it increases with increase in V_{BB}.

7.8.6 Advantages of UJT

1. It is a low cost device
2. It has excellent characteristics
3. It is a low power absorbing device under normal operating conditions

7.8.7 UJT as a Relaxation Oscillator.

Figure 7.16 shows the basic circuit of relaxation oscillator It consists of a UJT and biasing resistors R1and R2 in series with bases B1 and B2 the resistance R and capacitance C of the circuit will decide oscillating frequency of the circuit. The capacitor C is charged through R when the capacitor voltage V_C reaches the value of V_P, the UJT fires and rapidly discharges capacitor C through base B1 so that UJT than cuts off and C starts to charge again. This cycle is repeated continuously generating a saw tooth wave form across C.

By changing the value of capacitance C or resistance R we can change the frequency of the output wave form. Figure 7.17 shows typical saw tooth wave form of the relaxation oscillator.

If the charging period of the capacitor is T1 and discharging period is T2 than the time period of the output wave form is T=T1+T2. The value of C and R so selected that the charging period is much greater than the discharging. Therefore the time period of the output is approximately equal to the T1, i.e. T=T1.

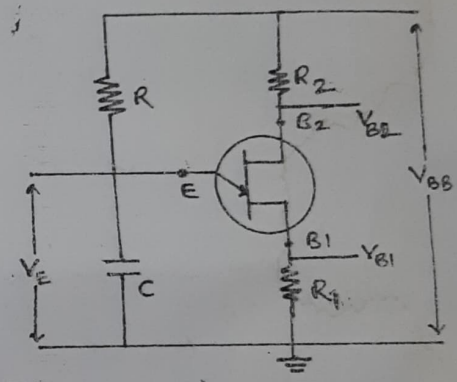


Figure 7.16

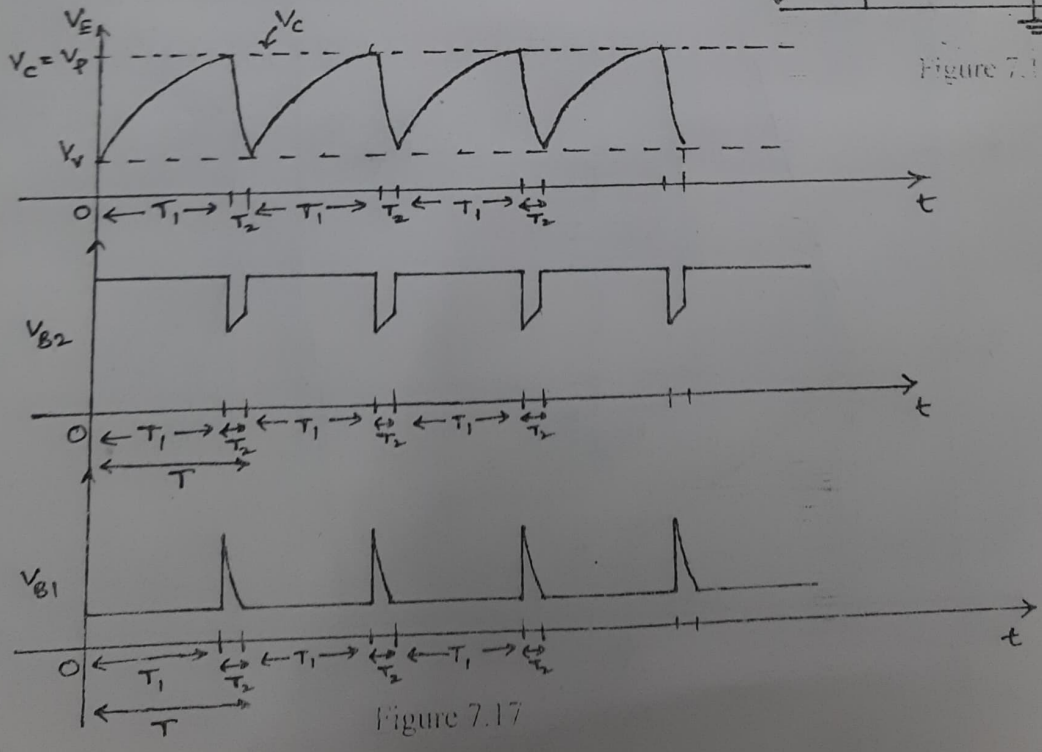
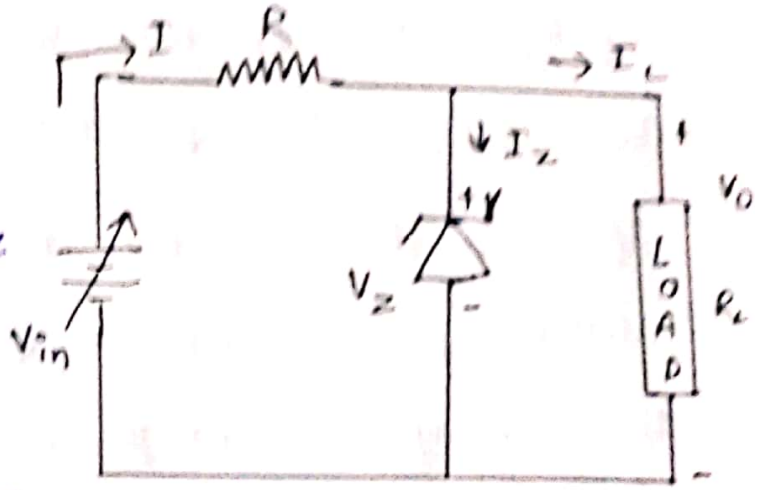


Figure 7.17

Zener Diode as a Voltage Regulator



→ As long as current through the zener diode is between $I_{Z,min}$ & $I_{Z,max}$ the voltage across it is constant and equal to zener voltage

→ Zener diode is connected in shunt with load. Hence output voltage $\boxed{V_o = V_z}$

→ from the above figure KCL total current $I = I_L + I_Z$

Case-1: Regulation with vary in input voltage (V_{in})

load current $(i_L) = \frac{V_o}{R_L} = \frac{V_z}{R_L}$ $\quad I_L$ = constant

If $V_{in} \uparrow$ total current $I \uparrow$ but I_L is constance. Hence the I_Z increases to keep I_L constant

$$\uparrow I = (I_L) + I_Z \uparrow$$

when $V_{in} \uparrow$ $\quad I \downarrow$

$$\downarrow I = (I_L) + I_Z \downarrow$$

but to keep I_L constant $I_Z \downarrow$. Thus the change in I/p voltage is compensated and O/P is maintained constant.

ii) Regulation with varying load.

V_{in} = constant [I/P voltage]

R_L = variable [load resistance]

$I = I_L + I_Z$ $\qquad I = \frac{V_{in} - V_z}{R}$ = constant

Scanned by CamScanner

and V_{in} = constant, V_z = constant

⇒ If $R_L \uparrow$ then I_L decreases and to keep I constant $I_z \uparrow$ accordingly Ⓘ = $\downarrow I_L + I_z \uparrow$

→ If $R_L \downarrow$ then I_L increases and to keep I constant $I_z \downarrow$ accordingly Ⓘ = $\uparrow I_L + I_z \downarrow$

thus change in load gets compensated and constant o/p is maintained

Silicon Controlled Rectifier (SCR)

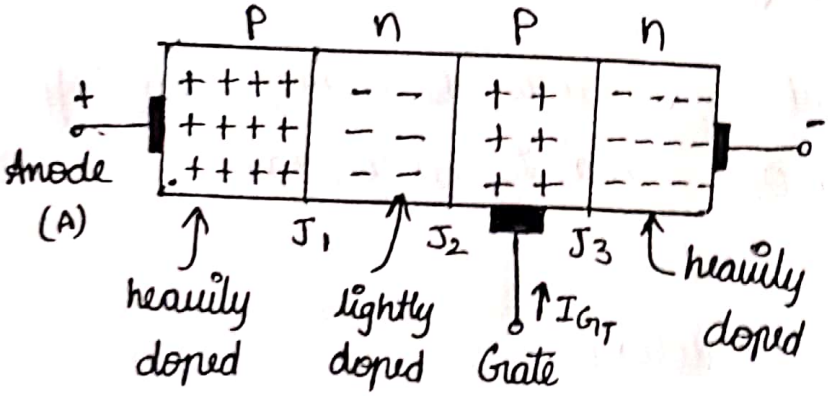
Construction:

→ The SCR is a four layer p-n-p-n device where p and n layers are alternately arranged. The outer layers are heavily doped while inner layers are lightly doped.

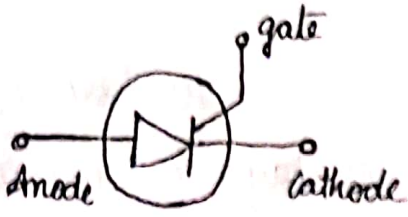
→ There are three p-n junctions called J_1, J_2 and J_3

→ The outer p layer is called anode while outer n layer is called cathode. Middle p layer is called gate

→ The three terminals are taken out respectively from these three layers, as shown in figure



Construction of SCR



Symbol of SCR

Scanned by CamScanner

→ Anode must be positive with respect to cathode of forward bias the SCR

→ But this is not sufficient criterion to turn SCR ON. To make it ON, a current is to be passed through the gate terminal denoted as I_{GT}. Thus it is a current operated device

→ The I_{GT} is gate trigger current required to make the SCR ON

→ The basic material used for the SCR fabrication is silicon

Working principle of SCR

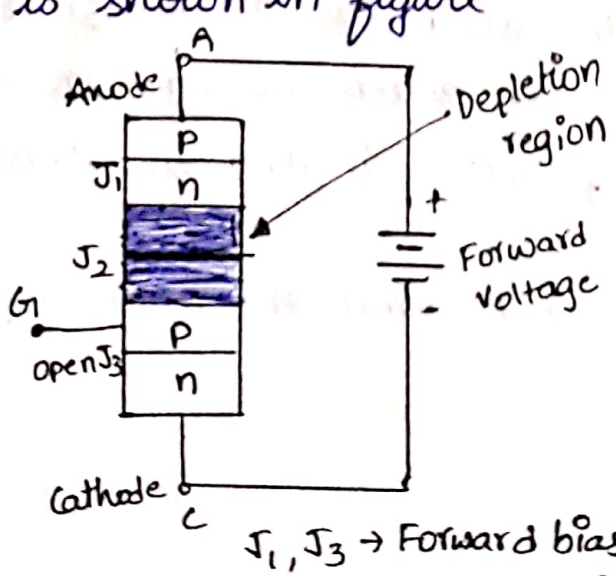
The operation of SCR is divided into two categories,
i) when gate is open and ii) when gate is closed

1) when gate is open:

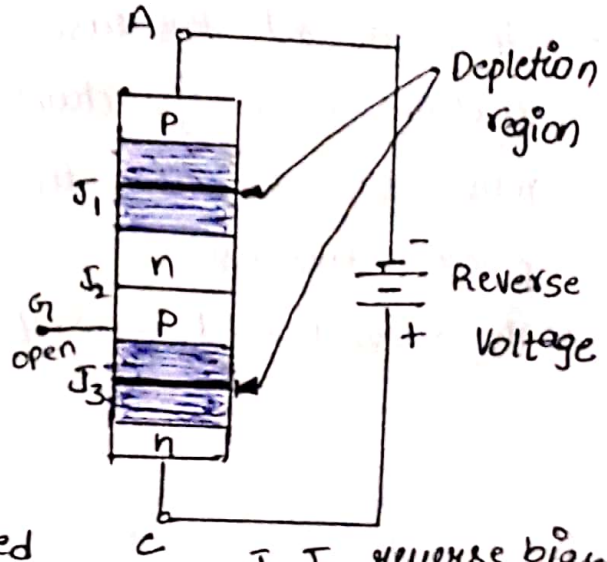
→ Consider that the anode is +ve with respect to cathode and gate is open

→ The junctions J_1 and J_3 are forward biased and junction J_2 is reverse biased. There is depletion region around J_2 and only leakage current flows which is negligibly small

→ Practically the SCR is said to be OFF. This is called forward blocking state of SCR and voltage applied to anode and cathode with anode +ve is called forward voltage. This is shown in figure



J_1, J_3 → Forward biased
J_2 – reverse biased



J_1, J_3 reverse biased
J_2 Forward biased

Scanned by CamScanner

→ With gate open if cathode is made +ve with to anode, the junctions J_1, J_3 become reverse biased and J_2 forward biased. Still the current flowing is leakage current, which can be neglected as it is very small

→ The voltage applied to make cathode +ve is called reverse voltage and SCR is said to be in reverse blocking state. This is shown in the figure

→ In forward blocking state, if the forward voltage is increased and made sufficiently large, the reverse biased junction J_2 breaks down and SCR conducts heavily

2) When gate is closed:

→ Consider that the voltage is applied between gate and cathode when the SCR is in forward blocking state

→ The gate is made positive with respect to the cathode.

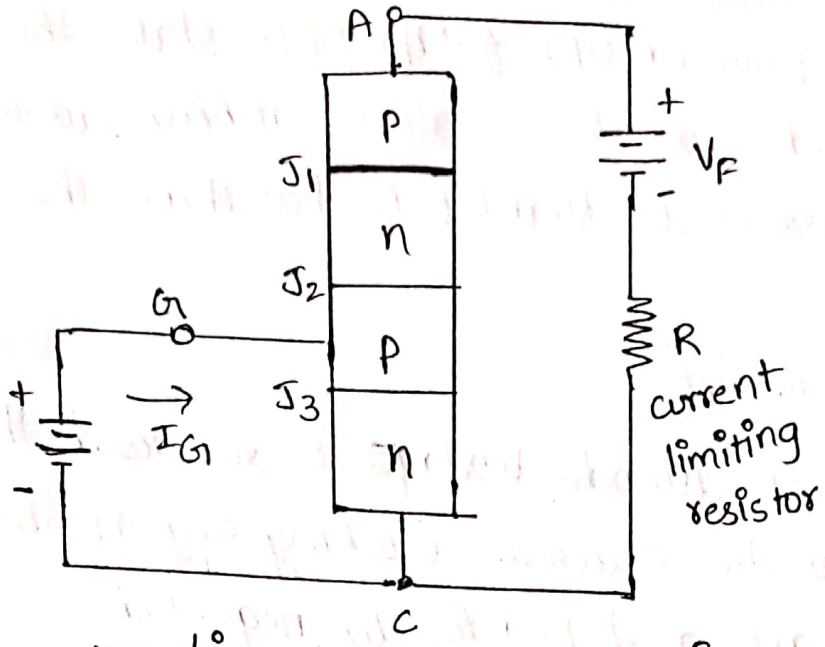
→ The electrons from n-type cathode which are majority in number, cross the junction J3 to reach to positive of battery

→ While holes from P types move towards the negative of battery, this constitutes the gate current

→ This current increases the anode current as some of electrons cross junction J_2. As anode current increases, more electrons cross the junction J_2 and the anode current further increases

→ The resistance R is required to limit the current.

Scanned by CamScanner



operation of SCR when gate is closed

→ once the SCR conducts, the gate loses its control

Characteristics of SCR:

1) Forward characteristics:

→ It shows a forward blocking region, when $I_G = 0$, It also shows that when forward voltage increases upto V_{BO}, the SCR turns ON and high current results. The drop across SCR reduces suddenly which is now the ohmic drop in the four layers. The current must be limited only by the external resistance in series with the device

→ It also shows that, if gate bias is used then as gate current increases, less voltage is required to turn ON the SCR.

→ If the forward current falls below the level of the holding current I_H, then depletion region begins to develop around J_2 and device goes into the forward blocking region

Scanned by CamScanner

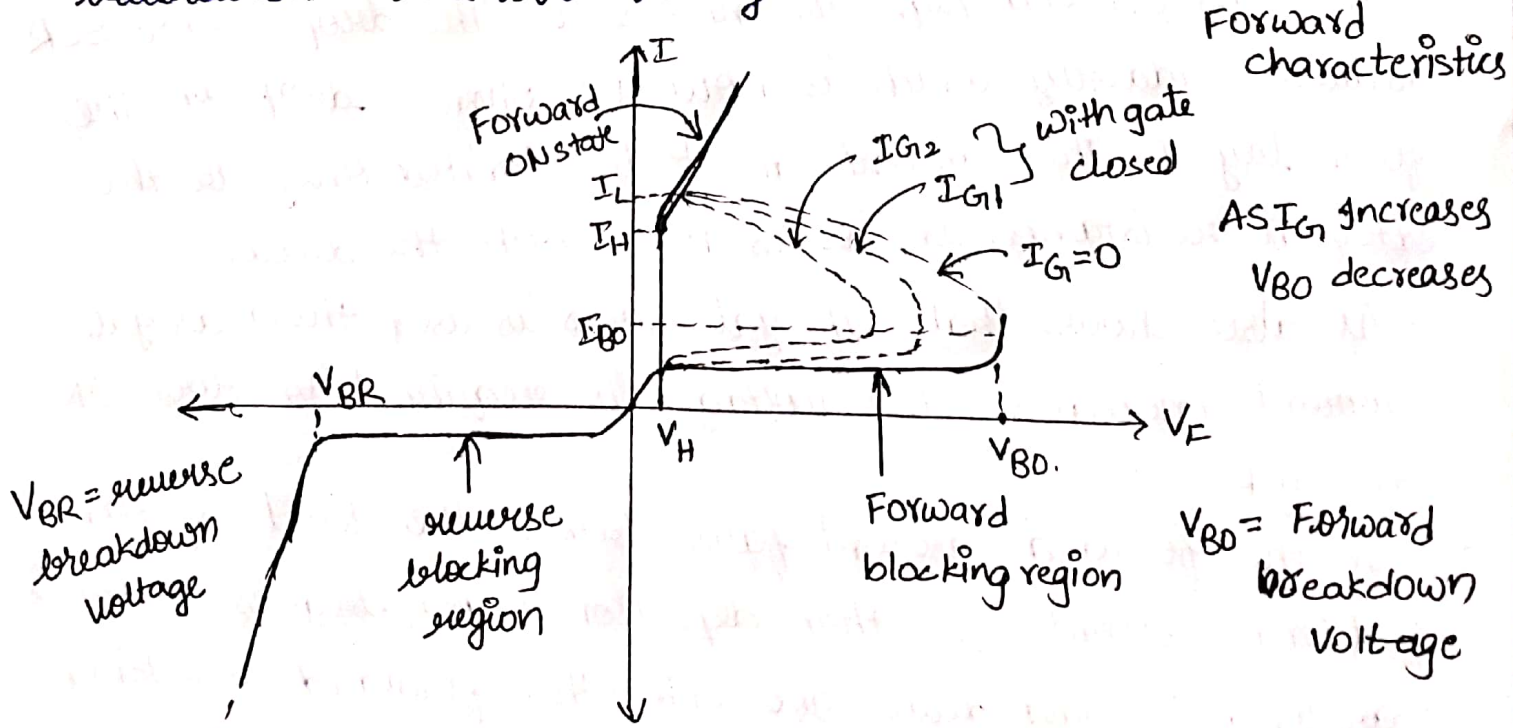
→ When SCR is turned ON from OFF state, the resulting forward current is called latching current I_L. The latching current is slightly higher than the holding current

Reverse Characteristics:

→ If the anode to cathode voltage is reversed, then the device enters into the reverse blocking region. The current is negligibly small and practically neglected.

→ If the reverse voltage is increased, similar to the diode, at a particular value avalanche breakdown occurs and a large current flows through the device. This is called reverse breakdown and the voltage at which this happens is called reverse breakdown voltage V_{BR}.

→ The forward breakover voltage is greater than reverse ~~breakdown~~ breakover voltage.



Characteristics of SCR

Scanned by CamScanner

M. PAVANI

--: Small signal Low frequency BJT models :—

5.0 Introduction:-

We know that the V-I characteristics of BJT are non-linear. The analysis of such non-linear devices is complex. The analysis of BJT circuits depends upon the magnitude of the applied input (a.c) signal. It will determine whether small-signal or large-signal analysis should be applied. Here, we will begin by idealizing a transistor with the help of simple approximations that will retain transistor important features while discarding its less important quantities. These approximations will help us to analyse transistor circuits easily and rapidly.

In this chapter, we will discuss only the analysis of the small (a.c) signal equivalent models. Conceptually, analog circuits often operate with signal level that are small compared to the bias voltages and currents (i.e Q-point values) in the circuit. Under this condition, small-signal model can be derived that allow calculations of the circuit, like gain, input, output terminal impedances, without the necessity of including the bias quantities. The parameters introduced in the equivalent model presented here are interpreted interms of the external voltage-ampere (V-I) characteristics of the transistor configurations.

NOTE:- Before going into the discussion, one should know about the following terms (i) Port and (ii) Two port network. Port means a set of two terminals (pair of terminals). Two port network means any circuit or device having four terminals in which two for input purpose and the other two for output purpose i.e input port and output port. A transistor may be regarded as a four pole (terminal) network or two port network irrespective of its circuit configuration. for example, considering a CE configuration. The base and emitter terminals may be regarded as input terminals (input port) while the collector and emitter terminals as output terminals (output port). This representation is

advantageous because the four pole i.e two port network theory may be applied to the circuit analysis which is readily available. figure 5.1 shows the transistor as a four pole block box i.e two port network representation of the transistor.

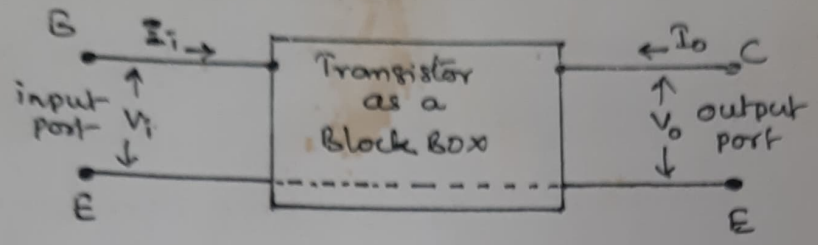


Figure: 5.1 Two port representation of a transistor

The currents are taken positive when they enter the transistor and negative when they leave the transistor.

5.1 Practical circuit of transistor amplifier:-

Figure: 5.2 shows a practical single stage CE transistor amplifier circuit. Its various circuit elements and their functions are as follows:

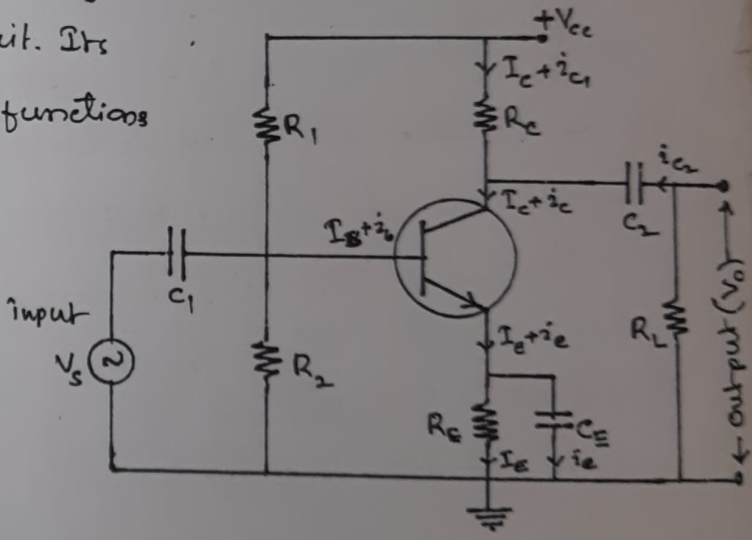


Figure: 5.2 CE amplifier

(i) Biasing:- The emitter resistor R_E and two resistors R_1 and R_2 establishes a voltage divider biasing, to provide proper operating point for the CE amplifier.

(ii) Coupling capacitors C_1 and C_2:-

The capacitor C_1 couples input ac signal to the base of the transistor. If it is not used the resistance of the source (a.c) will be in parallel to R_2 and the bias voltage of the base will change. Thus capacitor C_1 used to block any d.c component present in the signal and allows only a.c signal to flow into the input circuit and isolates the signal from R_2.

Similarly, the capacitor C_2 couples the output of the amplifier to the load or to the next stage. If C_2 is not used, R_c will come in parallel with the resistance R_1 of the biasing network of the next stage. This will distrubs

(.....)

the biasing condition of the next stage. In general, capacitance values of the coupling capacitors are approximately ($C_1, C_2 \approx$) 10 μF.

(iii) Bypass capacitor $R_E C_E$:-

The emitter bypass capacitor C_E (of large value ≈ 100 μF) is connected in parallel with the emitter resistor R_E. So that its reactance X_c is small. It, therefore, bypasses the amplified a·c signal present in the emitter current. If it is not used, then amplified a·c signal passing through R_E will cause a voltage drop across it which will reduce the output voltage, reducing the gain of the amplifier.

The reactive impedance of a capacitor is given by

$$X_c = \frac{1}{2\pi f C}$$

Thus, for d·c components, all the capacitors have extremely high (infinity) impedance and they can be treated as open circuits where as for a·c signals, all the capacitors offers small impedances and hence they can be treated as an a·c short circuits, to maintain stable biasing condition even after connecting the source and load. Therefore, replacing the capacitors with short circuits we get resultant circuit as shown in figure 5.3

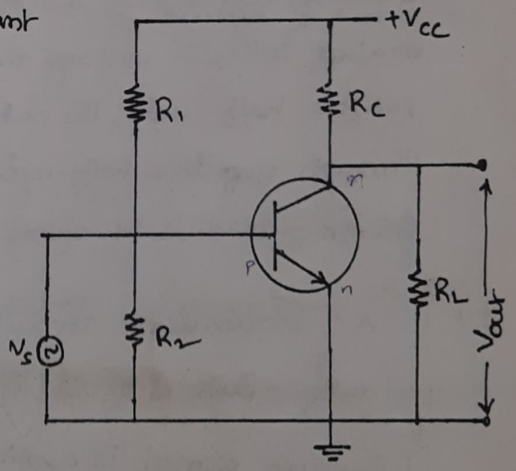
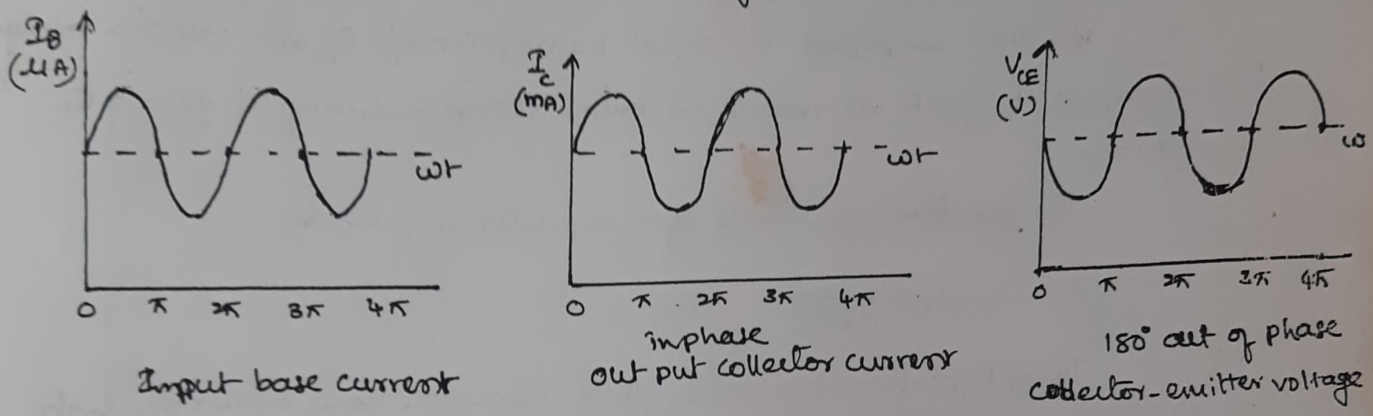


Figure: 5.3

In a common-emitter circuit, the collector-current is controlled by the base-current rather than emitter-current. When input (signal) is applied to the base (the signal, we wish to amplify is connected in series with the bias source and is of quite small amplitude), a very small change in base-current provides a larger change in collector current and thus extremely large ~~base~~ current gains are possible with CE amplifier.

Since the transistor is biased to operate in the active region, the output is linearly proportional to the input. The output i.e collector-current is β times larger than the input base current in the CE amplifier.

Hence, the collector current will also vary sinusoidally about its Q-point values. Consequently, the output voltage will also vary sinusoidally. The collector current varies above and below its Q-point values same as the input base current i.e I_c in phase with I_B and the collector-to-emitter voltage varies above and below its Q-point values 180° out of phase with the base voltage, as shown in the figure 5.4



Input base current

inphase
out put collector current

180° out of phase
collector-emitter voltage

Figure: 5.4 waveforms

NOTE:- Referring to the figure 5.4, when positive half-cycle is applied to the input, it opposes the forward bias of the circuit which causes the decrease in collector-current. It decreases the voltage drop across the load R_L and thus makes collector voltage more negative. Hence, when input varies through a positive half-cycle, the output voltage developed at the collector varies through negative half-cycle and vice-versa. Thus the output voltage in a CE amplifier is in out of phase (180° phase difference) with the input signal

5.1.1 AC equivalent circuit:-

Both d.c and a.c conditions exist in a transistor amplifier. When no signal is applied, base current I_B, collector current I_C and emitter current I_E (are only due to d.c supply) flow in the circuit. When a.c signal is applied, a.c base current i_b, ac collector current i_c and a.c emitter current i_e also flow in addition with the d.c currents.

To draw the a.c equivalent circuit of transistor amplifier, we consider only the a.c conditions, d.c voltages are considered zero (or shorted to ground) and capacitors are replaced by short circuits

(Page no: 0016)

to bypass the a.c signals. Figure 5.5 shows the a.c equivalent model of the CE amplifier. Here, R_1 appears in parallel with R_2, Similarly, R_C appear in parallel with load R_L.

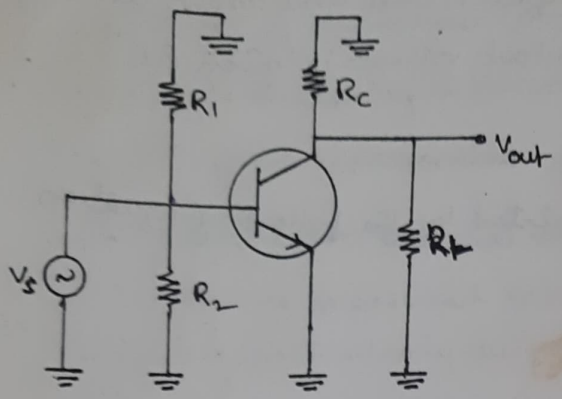


Figure: 5.5(A)

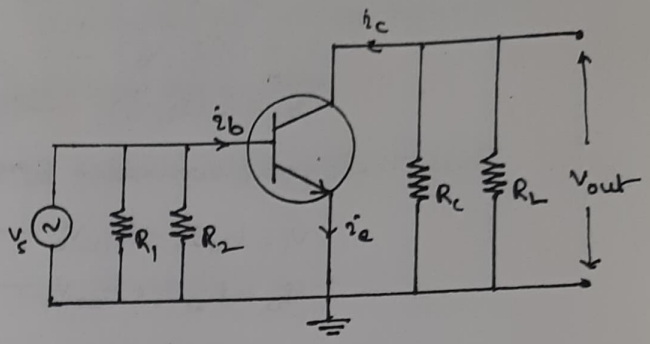


Figure: 5.5(B)

Therefore, the effective load R_L' for ac signal is given by

$$R_L' = R_C \| R_L = \frac{R_C R_L}{R_C + R_L} \quad \text{and} \quad R_i = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

i.e input impedance of the amplifier $R_i = \frac{R_1 R_2}{R_1 + R_2}$ and the output impedance is $R_L' = \frac{R_C R_L}{R_C + R_L}$. Therefore, the input voltage V_i and output voltage V_o can be written as

$$V_i = i_b R_i \quad \text{and} \quad V_o = i_c R_L'$$

Hence, the voltage gain of the amplifier, which is the ratio of output a.c voltage to the input a.c voltage, is given by

$$A_V = \frac{V_o}{V_i} = \frac{i_c R_L'}{i_b R_i} = \beta \frac{R_L'}{R_i} \quad \text{--- (1)}$$ where $\beta = \frac{i_c}{i_b}$ - current amplification factor.

5.2 BJT Hybrid model :—

The components of a small-signal low frequency equivalent circuit are called hybrid parameters or h-parameters, the equivalent circuit is called the hybrid model or h-parameter model. these parameters are denoted by h_i, h_r, h_f and h_o. From the two port network representation as shown in figure 5.1, for each port, there are two variables current

and voltage (i.e I and V).

In general, transistor is a current controlled device, thus input current is an independent variable. The input voltage and output current are the functions of input current and output voltage, is given as

$$V_i = f_1(I_i, V_o) \quad \text{—— (2)}$$

$$I_o = f_2(I_i, V_o) \quad \text{—— (3)}$$

Thus, these four variables can be related by the following equation

$$V_i = h_{11} I_i + h_{12} V_o \quad \text{—— (4)}$$

$$I_o = h_{21} I_i + h_{22} V_o \quad \text{—— (5)}$$

where V_i = input voltage, I_i = input current,

V_o = output voltage, I_o = output current.

The parameters, h_{11}, h_{12}, h_{21} & h_{22} which relating the four variables of the two port system are called h-parameters. From equations (4) & (5), h-parameters may be defined by first putting $V_o = 0$ (i.e output terminals are short circuited) and then $I_i = 0$ (i.e input terminals open circuited). Thus

(i) With output short circuited (i.e $V_o = 0$)

from equation (4) $V_i = h_{11} I_i \Rightarrow h_{11} = \frac{V_i}{I_i}$

and from (5) $I_o = h_{21} I_i \Rightarrow h_{21} = \frac{I_o}{I_i}$

$\therefore h_{11} = \left.\frac{V_i}{I_i}\right|_{V_o=0} = h_i$ = Input impedance (Ω)

and $h_{21} = \left.\frac{I_o}{I_i}\right|_{V_o=0} = h_f$ = Forward current transfer ratio or Forward current gain (no units)

(ii) With input open circuited (i.e $I_i = 0$)

from equation (4) $V_i = h_{12} V_o \Rightarrow h_{12} = \frac{V_i}{V_o}$

and from (5) $I_o = h_{22} V_o \Rightarrow h_{22} = \frac{I_o}{V_o}$

$\therefore h_{12} = \left.\frac{V_i}{V_o}\right|_{I_i=0} = h_r$ = Reverse voltage transfer ratio or Reverse voltage gain (no units)

and $h_{22} = \left.\frac{I_o}{V_o}\right|_{I_i=0} = h_o$ = output admittance (Siemen)

It may seen that two of these h-parameters (h_{12}, h_{21} or h_r, h_f) are the ratios and hence they have no units. The other two h_{11}, h_{22} (or h_i, h_o) have dimensions of impedance (ohm) and admittance (Siemen) respectively. They are thus a mixture of different units and hence the name hybrid of h-parameters. These h-parameters have the following advantages:

i) The h-parameters are real numbers at audio frequencies.
ii) They can be measured easily.
iii) They are particularly suitable for circuit analysis and design.
iv) They are specified by the transistor manufacturers.
v) They can be obtained from the transistor characteristics curves.

* h-parameter equivalent circuit for transistor :-

To analyse the performance of transistors, they are conveniently represented by h-parameter equivalent circuit. The h-parameter equivalent circuit can be drawn with the help of two equations ④ and ⑤, as shown in figure 5.6.

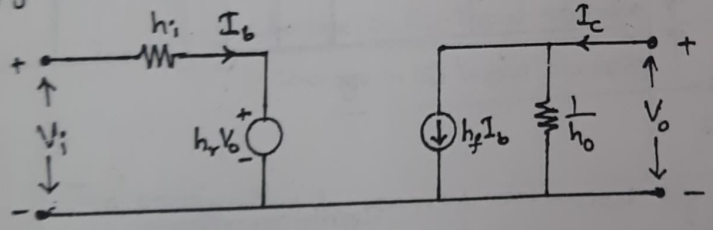


Figure: 5.6

NOTE:- A second subscript is added to the parameters to indicate the particular configuration, for example, for CE configuration the parameters are h_{ie}, h_{fe}, h_{re} and h_{oe}.

* Hybrid models for all the three transistor configurations :-

The basic circuit of hybrid model is same for all the three configurations, only parameters are different.

Table: 5-1

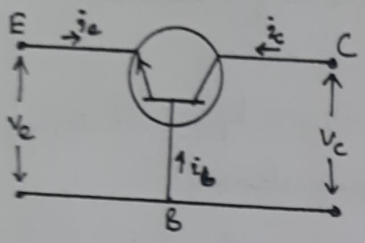
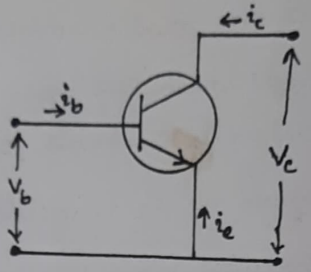
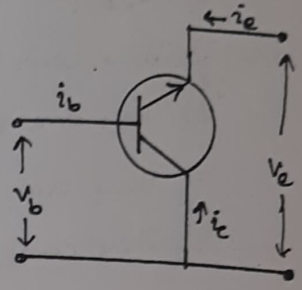
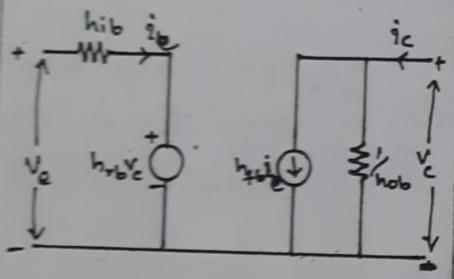
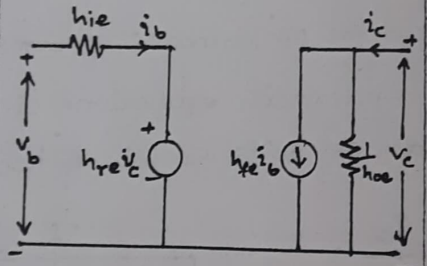
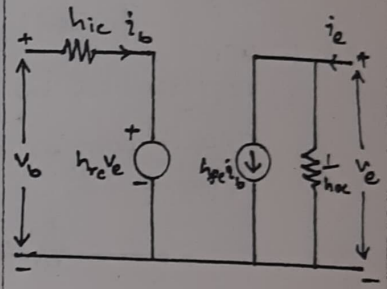
Common-base (CB)	common-emitter (CE)	common-collector (C.C)
$v_e = h_{ib} i_e + h_{rb} v_c$ $i_c = h_{fb} i_e + h_{ob} v_c$	$v_b = h_{ie} i_b + h_{re} v_c$ $i_c = h_{fe} i_b + h_{oe} v_c$	$v_b = h_{ic} i_b + h_{re} v_e$ $i_c = h_{fc} i_b + h_{oe} v_e$
		
		

Table: 5-2

Parameter	Configurations		
	C.B	C.E	C.C
1) Input impedance (h_i)	h_{ib}	h_{ie}	h_{ic}
2) Forward current transfer ratio or gain (h_f)	h_{fb}	h_{fe}	h_{fc}
3) Reverse voltage ratio or gain (h_r)	h_{rb}	h_{re}	h_{rc}
4) Output admittance (h_o)	h_{ob}	h_{oe}	h_{oc}

5.3 Determination of h-parameters from the transistor characteristics:-
(or Graphical determination of h-parameters)

The value of the h-parameters can be found graphically by making use of the transistor's input and output characteristics. The most accurate values of h-parameters can be obtained in this method. The parameters h_i and h_r are determined from the input characteristics whereas the parameters h_f and h_o are determined from the output characteristics. The first and most important step in determining the h-parameters is to obtain the Q-point values of current and voltages i.e I_{CQ} and V_{CEQ}.

To determine h_i value, a line is drawn tangent to the input characteristics curve through the Q-point to establish a line for a constant output voltage. The slope of this line gives the parameter h_i value. In other words, change in the input voltage is determined for a small change in the value of input current around the Q-point. The value of h_i is then determined by the ratio of the change in the value of input voltage to the change in the input current for a constant output voltage

$$\text{i.e } h_i = \left.\frac{\text{Change in the input voltage}}{\text{Change in the input current}}\right|_{\text{at constant output voltage}} = \text{slope of the tangent} \quad \text{——(6)}$$

The parameter h_r can be obtained by drawing a horizontal line through the Q-point for the value of constant input current on the input characteristics. The change in input voltage is determined for a small change in the value of output voltage around the Q-point. The value of parameter h_r is then determined by the ratio of the change in the input voltage to the change in the value of output voltage for a constant input current value.

$$\text{i.e } h_r = \left.\frac{\text{Change in the input voltage}}{\text{Change in the output voltage}}\right|_{\text{at constant input current}} \quad \text{——(7)}$$

The value of parameter h_f is determined by drawing a vertical line corresponding to the Q-point value on the output characteristics. The change in the output current is determined for a small change in the input

current around the Q-point. The value of h_f is then determined by the ratio of the change in the value of output current to the change in the input current for a constant output voltage value.

$$\text{i.e} \quad h_f = \left.\frac{\text{Change in the output current}}{\text{Change in the input current}}\right|_{\text{at constant output voltage.}} \qquad \text{—(8)}$$

Similarly, the value of parameter h_o is determined by drawing a tangent to a output characteristic curve corresponding to the Q-point value the change in the output current is determined for a small change in the output voltage around the Q-point. The value of h_o is then determined by the ratio of change in the value of output current to the change in the output voltage for a constant input current.

$$\text{i.e} \quad h_o = \left.\frac{\text{change in the output current}}{\text{change in the output voltage}}\right|_{\text{at constant input current.}} \qquad \text{—(9)}$$

5.3.1 Determination of h-parameters for a CE transistor circuit :-

As the most frequently employed configuration is the CE configuration. We discuss here the determination of h-parameters of a transistor circuit operating in this mode.

In a common-emitter configuration, the instantaneous total values of the input and output currents are I_B and I_C respectively. The instantaneous total values of input and output voltages are V_B and V_C respectively. figures 5.7 and 5.8 shows the input and output characteristics of a CE transistor circuit.

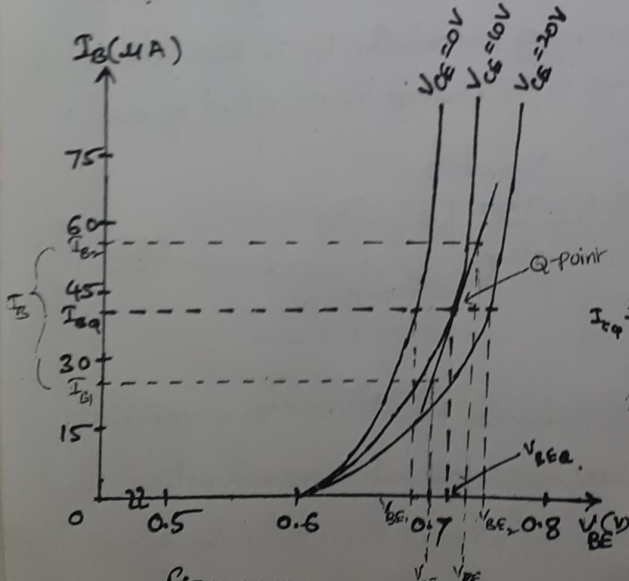


Figure : 5.7

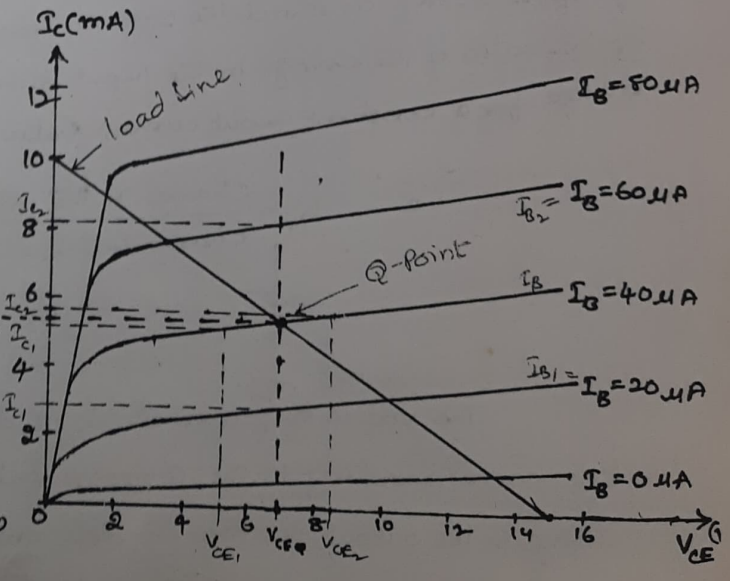


figure : 5.8

The value of h_{ie} is determined by drawing tangent, as shown in the figure: 5-7, to the input characteristic curve through the Q-point to establish a line for a constant V_{CE} value. A small change in the input voltage $V_{BE_2} - V_{BE_1}$ is determined for a small change in the value of input current $I_{B_2} - I_{B_1}$ around the Q-point. The ratio of these values gives the parameter h_{ie}, i.e

$$h_{ie} = \left.\frac{V_{BE_2} - V_{BE_1}}{I_{B_2} - I_{B_1}}\right|_{\text{at const } V_{CE}} \qquad (\because \text{From equation } ⑥)$$

For example, from the figure 5-7, input characteristics

$$h_{ie} = \frac{(720 - 685)\,mV}{(54.5 - 24.5)\,\mu A} = \frac{35\,mV}{30\,\mu A} = 1.167\,K\Omega$$

The value of h_{re} can be obtained by drawing a horizontal line through the Q-point for the value of constant input current i.e $I_B = 40\,\mu A$. The change in the input voltage $V_{BE_2} - V_{BE_1}$ is determined for a small change in the value of output voltage $V_{CE_2} - V_{CE_1}$ around the Q-point from the figure 5-7. Then the ratio of these values gives the parameter h_{re}, i.e

$$h_{re} = \left.\frac{V_{BE_2} - V_{BE_1}}{V_{CE_2} - V_{CE_1}}\right|_{\text{at const } I_B = 40\,\mu A} \qquad (\because \text{From equation } ⑦)$$

for example, from the input characteristics

$$h_{re} = \frac{(725 - 680)\,mV}{20 - 0} = \frac{45 \times 10^{-3}}{20} = 2.25 \times 10^{-3}$$

The parameter h_{fe} can be obtained by drawing a vertical line corresponding to the Q-point value i.e $V_{CEQ} = 7\,V$ on the output characteristics as shown in figure 5-8. The change in the output current $I_{C_2} - I_{C_1}$ is determined for a small change in the input current $I_{B_2} - I_{B_1}$ around the Q-point. Then the ratio of these values gives the value of parameter h_{fe}, i.e

$$h_{fe} = \left.\frac{I_{C_2} - I_{C_1}}{I_{B_2} - I_{B_1}}\right|_{\text{at const } V_{CE} = 7\,V} \qquad (\because \text{From equation } ⑧)$$

For example, $h_{fe} = \frac{(7.4 - 3.1)\,mA}{(60 - 20)\,\mu A} = 110$

The parameter h_{oe} can be obtained by drawing a tangent to the output characteristic curve corresponding to the Q-point. The change in the output current $I_{C_2} - I_{C_1}$ is determined for a small change in the output voltage $V_{CE_2} - V_{CE_1}$ around the Q-point. Then the ratio of these values gives the value of parameter h_{oe}, i.e

$$h_{oe} = \left.\frac{I_{C_2} - I_{C_1}}{V_{CE_2} - V_{CE_1}}\right|_{\text{at const } I_B = 40\,\mu A} \qquad (\because \text{From equation (9)})$$

for example; $h_{oe} = \dfrac{(5.4 - 5.15)\,mA}{(8.75 - 5.45)\,V} = \dfrac{0.25}{3.3} \times 10^{-3}$

$$= 75\,\mu S$$

NOTE/EXERCISE:- Determine the h-parameters of CB and CC transistor circuits from their characteristics. [Hint: Draw the characteristics of the configuration. To determine h-parameters, note down input and output currents and voltages and then corresponding changes. finally use them in the above discussion]

Table: 5.3; Typical h-parameter values for the CB, CE and CC configurations

Parameter	C·B	C·E	C·C
h_i	20 Ω	1 kΩ	1 kΩ
h_r	3×10^{-4}	2.5×10^{-4}	≅1
h_f	−0.98	50	−51
h_o	0.5 μS	25 μS	25 μS
$1/h_o$	2 MΩ	40 kΩ	40 kΩ

5.4 Analysis of transistor amplifier circuit using h-parameters:-

A transistor amplifier circuit can be designed by adding an external load and a signal source along with proper biasing, as shown in the figure 5.9. The two-port network of figure 5.9 represents a transistor in any one of the three possible configurations.

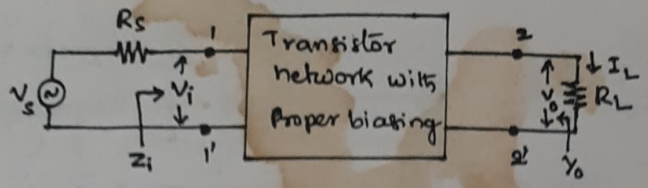


Figure: 5.9

We can replace transistor circuit with its small-signal hybrid equivalent model, as shown in the figure 5.10. This circuit is valid for any type of load i.e whether it be a pure resistance, or an impedance, or another transistor (In case of cascade amplifiers).

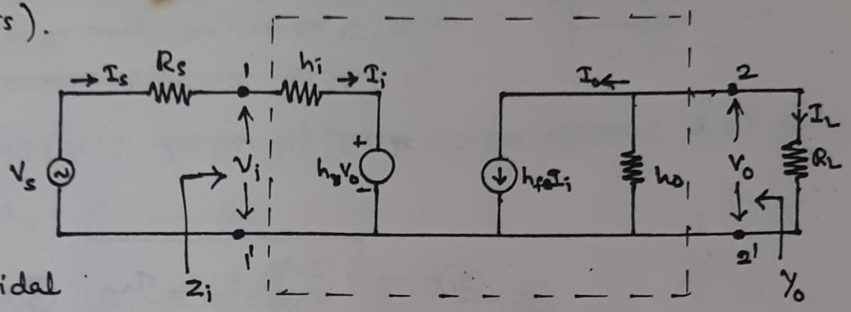


Figure: 5.10

Assuming sinusoidal input signal, let us analyze the circuit to find current gain, voltage gain, input impedance and output impedance or admittance etc.

(1) Current gain (A_I):- It is defined as the ratio of output to input current

i.e $$A_I = \frac{I_L}{I_i} = \frac{-I_o}{I_i} \quad \text{——— (10)}$$

Here I_L (load current) and I_o (output current) are equal in magnitude but opposite in direction, hence $I_L = -I_o$.

From the figure: 5.10, we have

$$I_o = h_f I_i + h_o V_o \quad \text{——— (11)}$$

But $V_o = I_L R_L = -I_o R_L$, substituting this value in the equation (11), we get

$$I_o = h_f I_i + h_o(-I_o R_L)$$

$$\Rightarrow I_o + h_o I_o R_L = h_f I_i$$

or $$I_o(1 + h_o R_L) = h_f I_i$$

$$\Rightarrow \frac{I_o}{I_i} = \frac{h_f}{1 + h_o R_L} \quad \text{——— (12)}$$

$\Rightarrow$ $Z_i = h_i + h_r A_I R_L$ $\qquad$ $\left(\because I = \frac{1}{1+h_o R_L}\right)$

From equations (10) & (12), we get,

$$A_I = \frac{-I_o}{I_i} = \frac{-h_f}{1+h_o R_L} \qquad \text{---(13)}$$

(2) Current gain (A_{Is}) taking into account the source resistance R_s.

The overall current gain A_{Is} is defined as

$$A_{Is} = \frac{I_L}{I_s} = \frac{-I_o}{I_s} = \frac{-I_o}{I_i} \cdot \frac{I_i}{I_s} = A_I \cdot \frac{I_i}{I_s} \qquad \text{---(14)}$$

The ratio I_i/I_s is derived from the input section of the hybrid equivalent circuit. The voltage source is replaced with equivalent current source (i.e Norton's equivalent circuit), then using current divider equation, as shown in the figure 5.11, we get

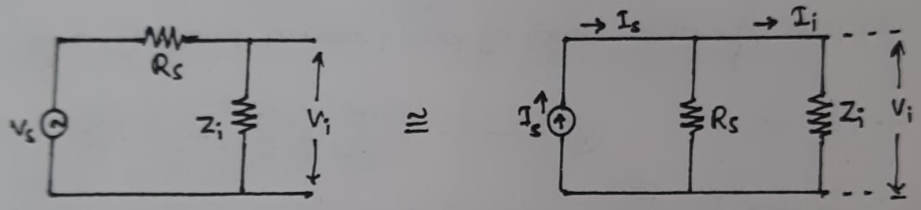
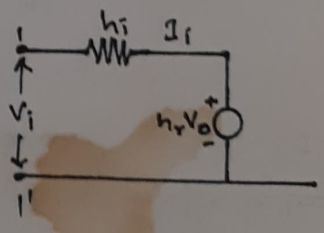


Figure: 5.11

$$I_i = I_s \cdot \frac{R_s}{R_s + Z_i} \Rightarrow \frac{I_i}{I_s} = \frac{R_s}{R_s + Z_i}$$

$\therefore$ From (14) $\qquad$ $A_{Is} = A_I \cdot \frac{R_s}{R_s + Z_i}$ $\qquad$ ---(15)

(3) Input impedance (Z_i) :- Actually, R_s is not an element of the amplifier. It is the signal-source resistance. To find the input impedance of the amplifier, remove the source and its resistance i.e open the terminals 1 and 1'. Then input impedance is given by



$$Z_i = \frac{V_i}{I_i} \qquad \text{---(16)}$$

From the circuit, $V_i = h_i I_i + h_r V_o$ ---(17)

$$\therefore Z_i = \frac{h_i I_i + h_r V_o}{I_i} = h_i + h_r \cdot \frac{V_o}{I_i} \qquad \text{---(18)}$$

substituting $V_o = A_I I_i R_L$ ---(19) in the equation (18), we get

$\left(\because A_I = \frac{-I_o}{I_i}\right.$
$\left. -I_o = A_I \cdot I_i \text{ and } V_o = -I_o R_L\right)$

$$Z_i = h_i + h_r \cdot \frac{A_I I_i R_L}{I_i}$$

$$\Rightarrow \boxed{Z_i = h_i + h_r A_I R_L} \quad \text{—— (20)} \qquad \left(\because A_I = -\frac{h_f}{1+h_o R_L}\right)$$

or

$$Z_i = h_i + h_r\left(-\frac{h_f}{1+h_o R_L}\right) \cdot R_L$$

$$\Rightarrow \boxed{Z_i = h_i - \frac{h_r h_f}{h_o + Y_L}} \quad \text{—— (21)} \qquad \left(\because \frac{1}{R_L} = Y_L\right)$$

From this equation, we can note that the input impedance is a function of the load.

④ Voltage gain (A_V):- It is defined as the ratio of output to the input voltage.

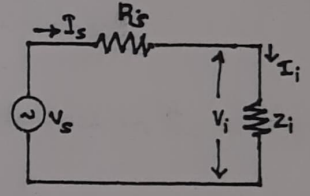
i.e $A_V = \frac{V_o}{V_i}$ —— (22)

From equation (19) $A_V = \frac{A_I I_i R_L}{V_i} = \frac{A_I R_L}{Z_i}$ —— (23) $\left(\because \frac{I_i}{V_i} = \frac{1}{Z_i}\right)$

⑤ Voltage gain (A_{VS}) taking into account the source resistance R_S.

The overall voltage gain A_{VS} is defined as

$$A_{VS} = \frac{V_o}{V_S} = \frac{V_o}{V_i} \times \frac{V_i}{V_S} = A_V \cdot \frac{V_i}{V_S} \quad \text{—— (24)}$$



The ratio $\frac{V_i}{V_S}$ is ~~determ~~ derived from the input section, by applying voltage divider rule

$$V_i = V_S \frac{Z_i}{Z_i + R_S} \Rightarrow \frac{V_i}{V_S} = \frac{Z_i}{Z_i + R_S}$$

Substitute this value in the above equation (24), we get

$$\boxed{A_{VS} = A_V \cdot \frac{Z_i}{Z_i + R_S}} \quad \text{—— (25)} \qquad \because A_V = \frac{A_i R_L}{Z_i}$$

$$\therefore \boxed{A_{VS} = \frac{A_i R_L}{Z_i + R_S}} \quad \text{—— (26)}$$

⑥ Output admittance (Y_o):- It is defined as the ratio of output current to the output voltage. i.e

$$Y_o = \frac{I_o}{V_o}$$

from equation (11) $I_o = h_f I_i + h_o V_o$

$$\therefore Y_o = \frac{I_o}{V_o} = h_f \frac{I_i}{V_o} + h_o \quad \text{—— (27)}$$

From figure, applying KVL, with $V_s = 0$, we get

$$R_s I_i + h_i I_i + h_r V_o = 0$$

$$I_i (R_s + h_i) = -h_r V_o$$

$$\therefore \frac{I_i}{V_o} = \frac{-h_r}{R_s + h_i}$$

Substituting this ratio in the above equation (27), we get

$$Y_o = h_f \left(\frac{-h_r}{R_s + h_i}\right) + h_o$$

$$\Rightarrow \boxed{Y_o = h_o - \frac{h_r h_f}{R_s + h_i}} \quad \text{— (28)}$$

From this equation, we can note that the output admittance is a function of the source impedance.

(7) Power gain (A_p) :- It is defined as the ratio of average power delivered to the load to the input power.

i.e $A_p = \frac{P_o}{P_i}$

The output power $P_o = V_o I_L = -V_o I_o$

and the input power $P_i = V_i I_i$

$$\therefore A_p = -\frac{V_o I_o}{V_i I_i} = \frac{V_o}{V_i} \cdot \left(-\frac{I_o}{I_i}\right) = A_V A_I \qquad \left(\because A_V = \frac{A_I R_L}{Z_i}\right)$$

$$\therefore \boxed{A_p = A_I^2 \frac{R_L}{Z_i}} \quad \text{— (29)}$$

We can summerize the small-signal analysis of a transistor amplifier circuit using h-parameters, as shown in the table

Table: 5.4

Current gain	A_I	$-h_f/(1+h_o R_L)$
Current gain with source	A_{IS}	$A_I R_s/(R_s+Z_i)$
Input Impedance	Z_i	$h_i - h_r h_f/(h_o+Y_L)$
Voltage gain	A_V	$A_I R_L/Z_i$
Voltage gain with source	A_{VS}	$A_I R_L/(Z_i+R_s)$
output admittance	Y_o	$h_o - h_r h_f/(R_s+h_i)$
Power gain	A_P	$A_I^2 R_L/Z_i$

These formulae is applicable to all the three transistor configurations For each configuration, we have to add the appropriate subscript to the h-parameters corresponding to the configuration.

5.5 Guidelines for linear analysis of a transistor circuit :-

So far we discussed the generalized transistor circuit analysis using h-parameters. There are many transistor circuit, they may consists of different configuration, different biasing techniques etc. The analysis of such circuits for its small-signal model can be made by the following guidelines

(1) Draw the actual circuit diagram.

(2) Replace the coupling and bypass capacitors by short circuit.

(3) Replace each individual d.c source by its internal resistance. In case of ideal voltage sources, the sources are simply replaced by a short circuits, while in case of ideal current sources, they are replaced by open circuits.

(4) Mark the points B(base), E(emitter) and C(collector) on the circuit diagram and locate these points at the start of the equivalent circuit. Maintain the same relative positions as in the original circuit.

(5) Now, replace the transistor by its h-parameter model.

(6) Solve the resultant linear circuit for the quantities like current gain, voltage gain, Input impedance and output admittance.

The following example explains the usage of guidelines in the analysis of transistor circuits.

Example: Let us consider a common-emitter transistor amplifier circuit with voltage divider bias.

Step 1 : Draw the actual circuit diagram.

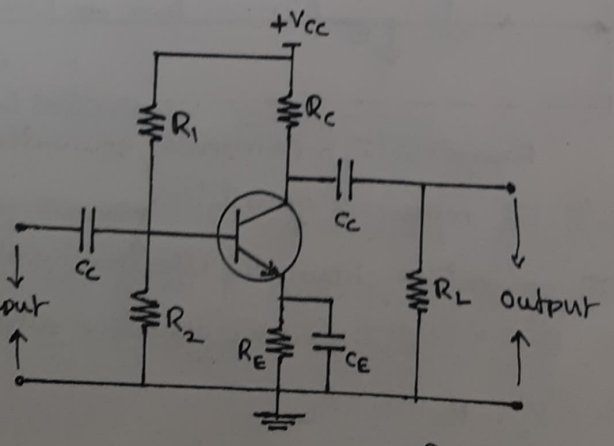


Figure: 5.12

step 2: short the coupling and bypass capacitors.

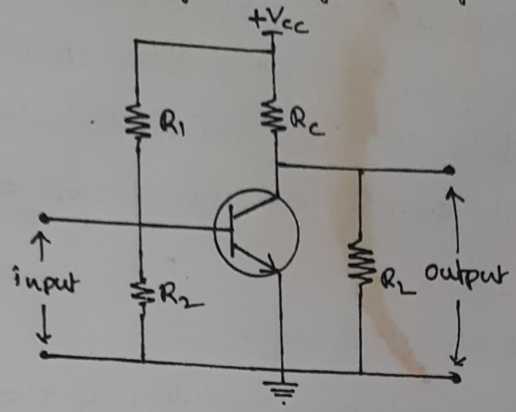


Figure : 5.13

step 3: Assuming V_{cc} is a ideal voltage source, short the V_{cc}.
step 4: mark the points B, E and C

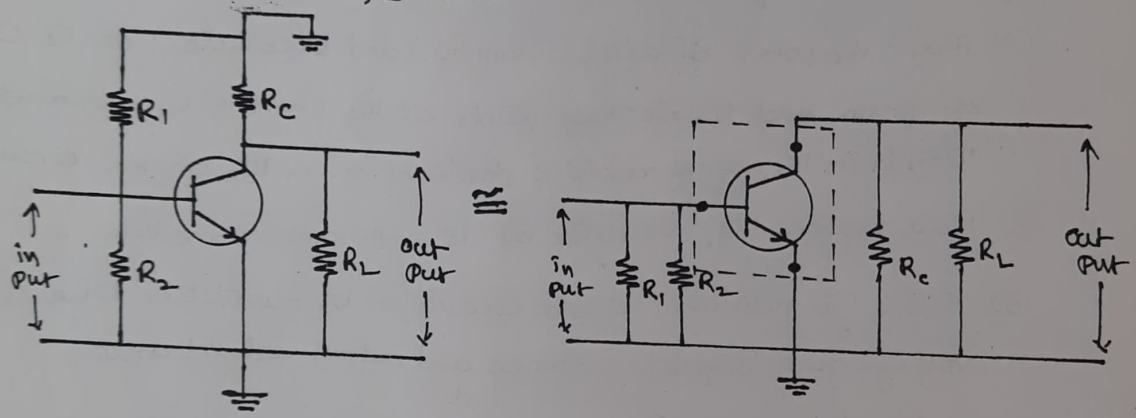


Figure : 5.14 (A)

Figure : 5.14(B)

step 5: Replace the transistor by its h-parameter model.

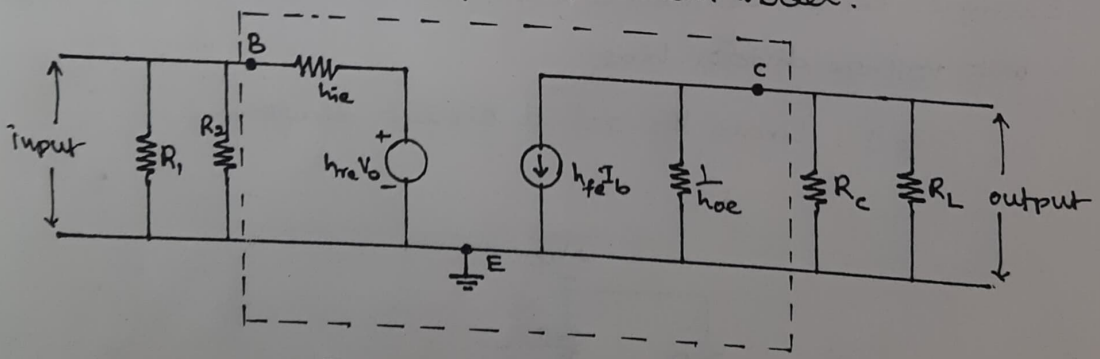


Figure : 5.15, h-parameter equivalent circuit.

step 6: Calculate the required quantities.

From the equivalent circuit, the effective input impedance is $R_i' = R_1 \| R_2 \| Z_i$ and the effective output impedance is $R_o' = R_o \| R_c \| R_L$.

Table 5.5

	C.E	C.B	C.C
Current gain	High	Low	High
Input impedance	Medium	Low	High
voltage gain	high	High	LOW
output impedance	Medium	High	Low

Thus CE configuration is used for a general purpose amplifier where both current gain and voltage gain are at desired level. As we know, the power gain is a product of voltage gain and current gain. The power gain of the CE amplifier is much greater than the power gain provided by the other two configurations (CB and CC).

The CB configuration has only few applications because, A_I-current gain is less than unity, R_i is the lowest and R_o is the highest of the three configuration hence it is used to match avery low impedance source to with a high impedance load. It is also wed as a constant (Ideal)-current source.

for the CC configuration A_I-Current gain is high but A_V-voltage gain is less than unity, R_i is the highest and R_o is the lowest of the three configurations. Hence it is used as a buffer stage between a high-impedance source and a low impedance load.

In a multistage amplifier, the first stage is usually a CC type so that a high input impedance is offered and so the driving source is not loaded. The middle stages are CE type which provide good current and voltage gain. The final stage is again CC type to provide a low output impedance to loaded.

5.6.1 Conversion formulae for h-parameters

Table: 5.6

C.B	C.E	C.C
$h_{ib} = \frac{h_{ie}}{1+h_{fe}}$	$h_{ie} = \frac{h_{ib}}{1+h_{fb}}$	$h_{ic} = h_{ie}$
$h_{fb} = \frac{-h_{fe}}{1+h_{fe}}$	$h_{fe} = \frac{-h_{fb}}{1+h_{fb}}$	$h_{fc} = -(1+h_{fe})$
$h_{rb} = \frac{h_{ie}h_{oe}}{1+h_{fe}} - h_{re}$	$h_{re} = \frac{h_{ib}h_{ob}}{1+h_{fb}} - h_{rb}$	$h_{rc} = 1-h_{re} \simeq 1$
$h_{ob} = \frac{h_{oe}}{1+h_{fe}}$	$h_{oe} = \frac{h_{ob}}{1+h_{fb}}$	$h_{oc} = h_{oe}$

The table 5.6 shows relation of the h-parameters of various configurations. It is to be noted that CE parameters interms of CB are obtained by simply interchanging the subscripts b and c.

5.7 Simplified Hybrid model :—

In the preceding sections, we have seen the detailed lengthy calculations of current gain A_I, voltage gain A_v, input impedance Z_i and output impedance Z_o. In general, in most practical cases it is justifiable to obtain approximate values of the above parameters (A_I, A_v, Z_i & Z_o) rather than to carryout the more lengthy exact values. Moreover, these two of the four h-parameters h_i and h_f are sufficient for the approximate analysis, provided that the load resistance R_L is small enough to satisfy the condition.

$$h_{oe} R_L < 0.1$$

If $h_{oe} \cdot R_L < 0.1$, the error in the calculations of A_I, A_v, Z_i and Z_o is less than 10%. Thus, we can employ the approximate analysis if $h_{oe} \cdot R_L < 0.1$, otherwise proceed for the exact analysis. The figure 5.7 shows equivalent circuit for the simplified hybrid model. this approximate model is common for all the three transistor configurations.

Since the common-emitter configuration is, in general, the most employed configuration, we first discuss the analysis of CE amplifier circuit using simplified hybrid model.

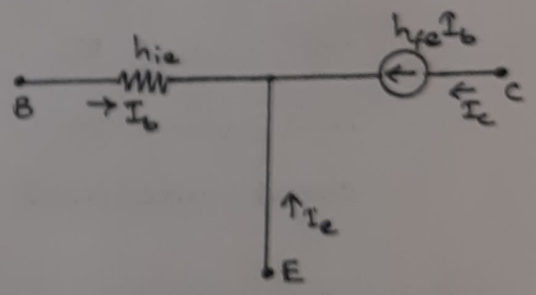


Figure : 5.7

5.7.1 Analysis of CE amplifier circuit using simplified hybrid model :

We now justify the validity of the proposed simplified hybrid model in the analysis of the CE transistor amplifier. Let us consider a CE amplifier and draw the h-parameter equivalent circuit as shown in figure. 5.9

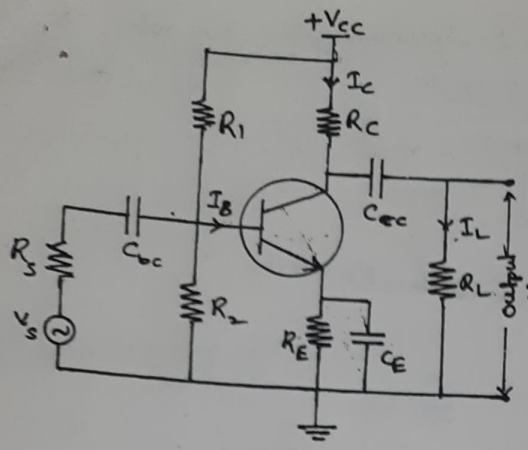


Figure: 5.8

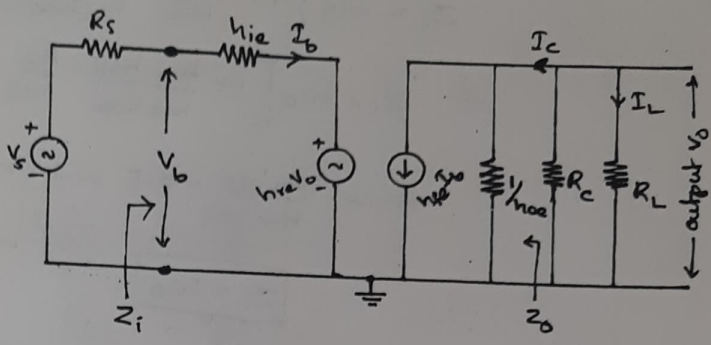


Figure: 5.9

Since $\frac{1}{h_{oe}}$ is in parallel with R_L and R_C, if $\frac{1}{h_{oe}} > R_L \| R_C$ i.e $(R_L \| R_C) h_{oe} < 1$ then h_{oe} may be neglected. If we neglected h_{oe} from the figure 5.9, then the collector current $I_c = h_{fe} I_b$. Under this situation, the magnitude of the voltage of the generator in the emitter-base section is given by

$$h_{re}|V_o| = h_{re}|V_c| = h_{re} I_c (R_L \| R_C) \qquad (\because R_L \& R_C \text{ are in parallel})$$

$$= h_{re} h_{fe} I_b (R_L \| R_C)$$

Since $h_{re} h_{fe} = 2.5 \times 10^{-4} \times 50 = 125 \times 10^{-4} = 0.0125$

$\therefore h_{re}|V_o| \simeq 0.01$ It is very small in comparison with $h_{ie} I_b$.

Hence, this voltage may be neglected. we therefore conclude that if the load $(R_L \| R_C)$ is small, it is possible to neglect the parameters h_{re} and h_{oe} in the h-parameter equivalent circuit. Figure 5.10 shows the resultant simplified approximate hybrid model

Analysis

(1) Current gain(A_I) :-

we know $A_I = \frac{-h_{fe}}{1 + h_{oe} R_L}$

(From the definition $A_I = \frac{I_o}{I_b} = \frac{-I_c}{I_b} = \frac{-h_{fe}}{1 + h_{oe} R_L}$)

Neglecting h_{oe}, $\boxed{A_I \simeq -h_{fe}}$

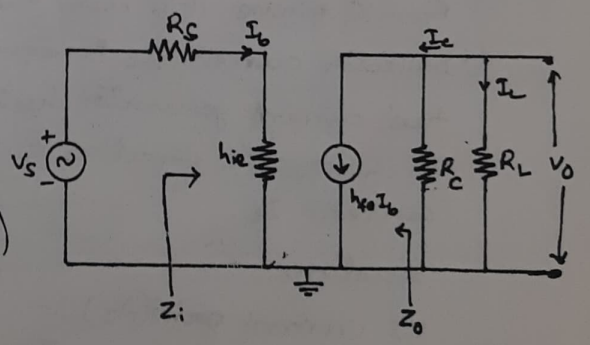


Figure: 5.10

(2) Input impedance (Z_i) :-

$$Z_i = h_{ie} + h_{re} A_I R_L$$

$$= h_{ie} \left[1 + \frac{h_{re}}{h_{ie}} \cdot A_I \cdot R_L \right]$$

adding $h_{fe}h_{oe}$ in the numerator and denominator, we get

$$Z_i = h_{ie}\left[1 + \frac{h_{re}}{h_{ie}} \cdot \frac{h_{fe}h_{oe}}{h_{fe}h_{oe}} \cdot A_I R_L\right]$$

$$\Rightarrow Z_i = h_{ie}\left[1 + \frac{h_{re}h_{fe}}{h_{ie}h_{oe}} \cdot \frac{A_I}{h_{fe}} \cdot h_{oe}R_L\right]$$

Since $\frac{h_{re}h_{fe}}{h_{ie}h_{oe}} = 0.5$ and $|A_I| = h_{fe}$ and $h_{oe}R_L < 0.1$

$$\therefore \boxed{Z_i = h_{ie}}$$

(3) Voltage gain (A_V):-

$$A_V = A_I \cdot \frac{R_L}{Z_i} = A_I \cdot \frac{R_L}{h_{ie}} \qquad (Z_i = h_{ie}).$$

$$\boxed{A_V = \frac{-h_{fe}R_L}{h_{ie}}} \qquad (A_I = -h_{fe})$$

(4) Output impedance (Z_o):-

$$Y_o = h_{oe} - \frac{h_{re}h_{fe}}{h_{ie}+R_s}$$

neglecting h_{oe} & h_{re} $\quad Y_o = 0$

$$\Rightarrow Z_o = \frac{1}{Y_o} = \infty$$

and $Z_o' = Z_o \| R_L \| R_C \Rightarrow Z_o' = \infty \| R_L \| R_C$

$$\Rightarrow \boxed{Z_o' = R_L \| R_C}$$

5-7-2 Analysis of CB amplifier using simplified hybrid model:

Figure: 5.11 shows the equivalent simplified hybrid model for CB amplifier

From the figure it is clear that the collector current I_c is equal to the current generator $h_{fe}I_b$ and it is in the opposite direction to the load current I_L.

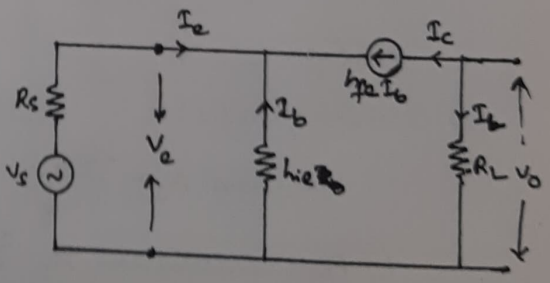


Figure: 5.11

Analysis

(1) Current gain (A_I):-

$$A_I = \frac{I_c}{I_e} = \frac{-I_c}{I_e} = \frac{-h_{fe}I_b}{-(1+h_{fe})I_b}$$

$$\boxed{A_I = \frac{h_{fe}}{1+h_{fe}}}$$

$(\because -I_e = I_b + I_c$
$\& I_c = h_{fe}I_b$
$-I_e = I_b + h_{fe}I_b$
$-I_e = I_b(1+h_{fe})$
$I_e = -I_b(1+h_{fe}))$

i.e the current gain of CB amplifier is always less than unity

(2) Input impedance (Z_i):-

$$Z_i = \frac{V_e}{I_e} = \frac{-h_{ie} I_b}{-(1+h_{fe}) I_b} = \frac{h_{ie}}{1+h_{fe}}$$

$$\boxed{Z_i = \frac{h_{ie}}{1+h_{fe}}}$$

(3) ~~Gain~~ voltage gain (A_v):-

$$A_v = \frac{V_o}{V_e} = \frac{I_L R_L}{I_e Z_i} = A_I \cdot \frac{R_L}{Z_i}$$

$$= \frac{h_{fe}}{(1+h_{fe})} \cdot \frac{R_L}{\frac{h_{ie}}{(1+h_{fe})}} = \frac{h_{fe}}{h_{ie}} \cdot R_L$$

(4) output impedance (Z_o):- It is the ratio of output voltage to the output current at $V_s = 0$

$$Z_o = \frac{V_o}{I_c}\Big|_{V_s = 0}.$$

when $V_s = 0$, i.e there is no source in the input section therefore $I_e = 0$

and current through the h_{ie} is zero i.e $I_b = 0$. $\therefore I_c = I_e - I_b = 0$

$$\therefore Z_o = \infty$$

$$\therefore Z_o' = Z_o \| R_L = \infty \| R_L = R_L$$

5.7.3 Analysis of C.C amplifier using simplified hybrid model:-

Figure: 5.12 shows equivalent simplified hybrid model for CC amplifier

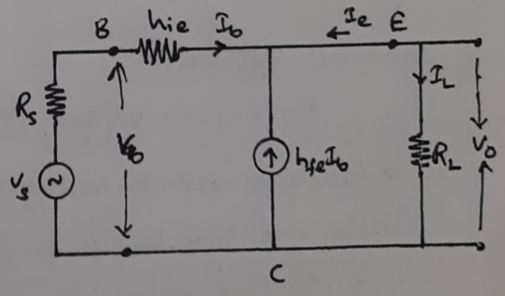


Figure: 5.12

Analysis

(1) current gain (A_I):-

$$A_I = \frac{I_L}{I_b} = \frac{-I_e}{I_b}$$

But $I_e = I_b + I_c$

From figure $-I_e = I_b + I_c$

$$= I_b + h_{fe} I_b = (1+h_{fe}) I_b$$

$$\therefore A_I = \frac{-I_e}{I_b} = \frac{(1+h_{fe}) I_b}{I_b} \Rightarrow \boxed{A_I = 1+h_{fe}}$$

(2) Input impedance (Z_i):- $Z_i = \frac{V_b}{I_b}$

Applying K.V.L, $V_b = h_{ie} I_b + I_L R_L$ or $V_b = h_{ie} I_b - I_e R_L$

$$\frac{V_b}{I_b} = h_{ie} + \frac{I_L}{I_b} \cdot R_L \Rightarrow \boxed{h_{ie} + A_I \cdot R_L = Z_i} \quad (\because A_I = 1+h_{fe})$$

or $\Rightarrow \boxed{Z_i = h_{ie} + R_L (1+h_{fe})}$

(3) voltage gain (A_V):- $A_V = \frac{V_o}{V_b} = \frac{I_L R_L}{I_b z_i} = A_I \frac{R_L}{z_i}$

$\Rightarrow$ ~~$A_V = (1+h_{fe}) R_L$~~

Rearranging the equation, we get ~~$h_{ie} = (1+h_{fe}) R_L$~~

$$A_V = A_I \cdot \frac{R_L}{z_i} - 1 + 1 = \frac{A_I R_L - z_i}{z_i} + 1 \qquad \left(\because z_i = h_{ie} + A_I R_L \Rightarrow z_i - A_I R_L = h_{ie} \right)$$

$$= \frac{-h_{ie}}{z_i} + 1 = 1 - \frac{h_{ie}}{z_i}$$

$$= 1 - \frac{h_{ie}}{h_{ie} + (1+h_{fe}) R_L} \qquad \left(\because h_{ie} < (1+h_{fe}) R_L \right)$$

$$\boxed{A_V \simeq 1}$$

~~NOTE:- for most practical cases, in general, the voltage gain always less than unity~~

NOTE:- for most practical cases, in general, the voltage gain is always less than unity.

(4) output impedance (z_o):- $z_o = \left. \frac{V_o}{I_L} \right|_{V_s = 0}$

$\therefore$ Applying KVL, $V_o = h_{ie} I_b + R_s I_b$

$= I_b (h_{ie} + R_s)$

and $I_L = -I_e = I_b (1 + h_{fe})$

$\therefore \quad z_o = \frac{I_b (h_{ie} + R_s)}{I_b (1 + h_{fe})} = \frac{R_s + h_{ie}}{1 + h_{fe}}$

Now, $z_o' = z_o \| R_L$

5.9 Transistor cut-off frequencies:

Another and most important parameter in the analysis of a transistor amplifier circuit is frequency response. At a constant input voltage, the variation of amplifier gain with respect to its frequency is called the frequency response of the amplifier.

A typical transistor frequency response curve is shown in figure: 5.13. While analyzing this curve, three values of frequency are important

(i) Lower cut-off frequency (f_L)
(ii) Mid-frequency range
(iii) Upper-cut-off frequency (f_H)

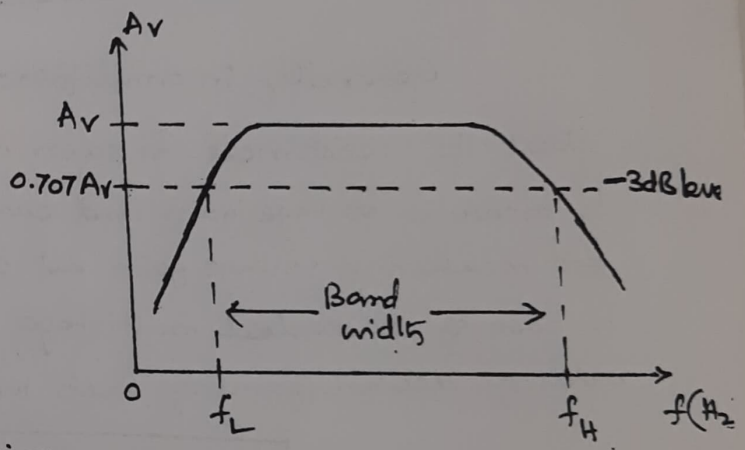


Figure: 5.13

The lower and upper cut-off frequencies are defined as

(a) where, voltage gain of the amplifier decreases to 0.707 times to its maximum gain i.e $\frac{1}{\sqrt{2}} A_V = 0.707 A_V$

(b) where, power gain of the amplifier decreases to (half) 0.5 times to its maximum gain) i.e $\frac{1}{2} A_P = 0.5 A_P$

(c) Interms of decibels, the frequencies corresponding to the -3dB level. Hence they are called as (i) -3dB frequencies, or (ii) half-power point ~~frequencies~~ -frequencies or (iii) down 3dB frequencies.

⁂ JFET Parameters:

The important parameters of JFET are as follows:

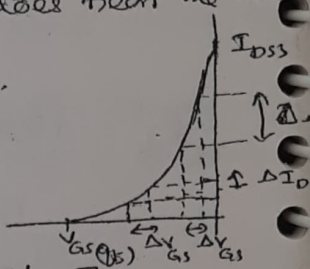
① Transconductance (g_m) ② Input resistance (R_{in})

③ Drain to source resistance (r_d) ④ Amplification factor (μ)

① **Transconductance (g_m):-** It is the change in the drain current for given change in gate-source voltage with the drain-source voltage constant. It is also called as mutual conductance.

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}\text{-const}}$$

from the transfer characteristics, we can say that it is the slope of the transfer characteristics. Since the slope varies, g_m also varies. g_m has a greater value near the top of the curve than it does near the bottom. The practical unit for g_m is millisiemen (mS) or mA/V.



we know that $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$.

Differentiating this eqn w.r.t V_{GS} we get,

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = I_{DSS} \cdot 2\left[1 - \frac{V_{GS}}{V_p}\right] \cdot \frac{-1}{V_p} = \frac{-2I_{DSS}}{V_p}\left[1 - \frac{V_{GS}}{V_p}\right]$$

$$\boxed{g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_p}\right)} \text{ or } \boxed{g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]}$$

where $g_{m0} = \frac{-2I_{DSS}}{V_p}$

By using above eqn we can calculate an approximate value for g_m at any point on the transfer characteristics curve.

② **Input resistance:** JFET operates with its gate-source junction reverse-biased. Therefore the input resistance at the gate is very high. The input resistance can be determined using the following eqn, where the vertical lines indicates an absolute value

$$R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$$

I_{GSS} – Reverse gate current. V_{GS} – Gate to source voltage.

③ Drain to source resistance (r_d):- From the drain characteristics Drain resistance r_d can be calculated. The drain resistance is the a·c resistance between drain and source terminals when the JFET is operating in the saturation region. It is the reciprocal of the slope of the drain-characteristic in the saturation region

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\Big|_{V_{GS}\text{-constant}}$$

④ Amplification factor(μ): It is defined as the ratio between drain-source voltage to the gate-source voltage.

$$\text{Amplification factor } \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}\Big|_{I_D\text{-const}}$$

$$\therefore \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}} = r_d \cdot g_m$$

$$\boxed{\mu = r_d \cdot g_m}$$

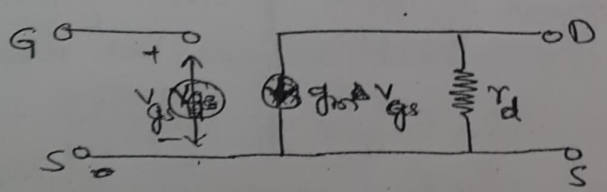
* Small signal model of JFET:-

We know that, drain to source current of JFET is controlled by gate-to-source voltage. From the transconductance [JFET Parameter]

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \Rightarrow \boxed{\Delta I_D = g_m \cdot \Delta V_{GS}}$$

another important JFET Parameter r_d, $r_d = \frac{\Delta V_{DS}}{\Delta I_D}\Big|_{V_{GS}\text{-const.}}$

From these Parameters we can draw the small signal model of JFET as shown below.



The figure shows the small signal low frequency a·c equivalent ckt for n-channel JFET. The relation of I_D by V_{GS} is included as a current source $g_m V_{gs}$ connected from drain to source. The input impedance is represented by the open ckt at its input terminals, since gate current I_G is zero. The output impedance is represented by r_d from drain to source.

7.1.4.

7.2 Common Source FET amplifiers:

The basic circuit and characteristics of a common source FET amplifier are very similar to that of the common emitter BJT amplifier. The common source amplifier can provide both voltage and current gain.

Since the input resistance looking in to the gate is extremely large, the current gain available from the FET amplifier can be quite large. But the voltage gain is generally inferior to that available from a BJT. Thus FET amplifiers are most useful with high output impedance signal sources where a large current gain is primary requirement.

Figure7.4 shows the common source n channel JFET amplifier. The JFET gate voltage V_G is biased through the potential divider network setup by resistors R1 and R2 and is biased to operate in its saturation region which is equivalent to the active region of the BJT.

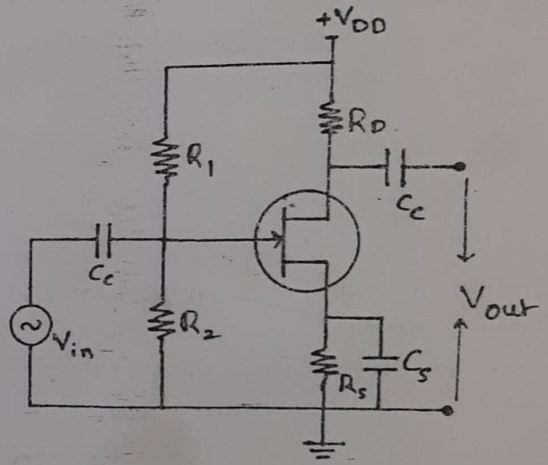


Figure 7.4

The gate biased voltage V_G is given by

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} \qquad \left(\text{Since } V_B = \frac{R_2}{R_1 + R_2} V_{CC} \text{ of BJT}\right)$$

The input signal (Vin) is applied between the gate and source. The out put voltage (Vout) is developed across the load. When the FET is 'ON' a voltage drop $I_d R_s$ is developed across R_s. This voltage drop across R_s, provides the necessary reverse bias in condition across the gate resistor. In order to keep

the Gate-Source junction reverse biased, the source voltage Vs needs to be a higher than the gate voltage VG.

When a negative going signal is applied to the input, the gate bias voltage is increased, due to this voltage the depletion regions are widened, so that the channel width decreased. That is channel resistance increases. Increase in the channel resistance causes the decrease in the drain current. This current flowing through the resistance RD, hence voltage drop across RD is decreased. Consequently, a positive going signal becomes available at the out put.

Since a small voltage variation at the gate produces a large voltage variation across lead RD i.e. an amplification of signal takes place.

It is seen that the output of the common-source FET amplifier, like common-emitter BJT amplifier, is 180 degrees out of phase with the input signal.

We can draw the equivalent circuit by Thevenizing the above circuit, as shown in figures 7.5(a) & 7.5(b).

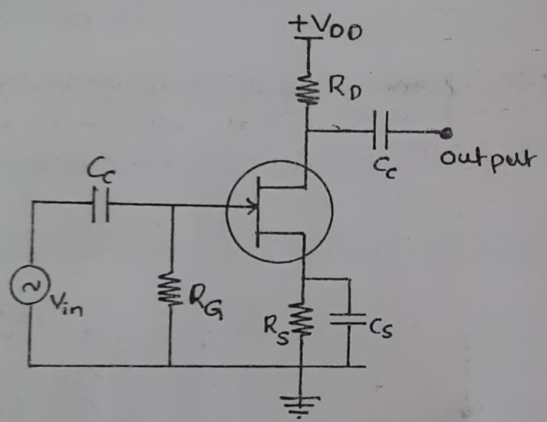


Figure: 7.5(a)

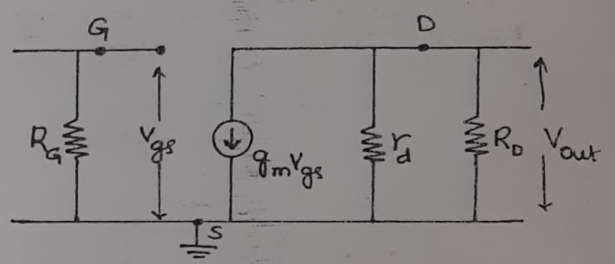


Figure: 7.5(b).

where $R_G = \frac{R_1 R_2}{R_1 + R_2}$

Analysis of the common source amplifier as follows:

1. Input Impedance: From the circuit $Z_{in} = R_G \| R_{GS}$, in an ideal JFET, RGS is infinite (∞) because $I_G = 0$. In an actual device, however, RGS is not actually infinite but extremely high as compared to RG [i.e. $I_G \neq 0$, since there is some minority carriers present, due to these carriers the gate current dose not zero].

$$\therefore Z_{in} \approx R_G$$

2. Output Impedance:

$$Z_O = r_d \| R_D$$

If $r_d >> R_D$, $\therefore Z_O \approx R_D$

3. Voltage gain: The output voltage

$$V_O = I_D * (r_d \| R_D) \qquad \therefore I_D = g_m V_{gs}$$
$$= -g_m V_{gs} * (r_d \| R_D)$$

$$A_V = \frac{V_O}{V_{in}} = \frac{V_O}{V_{gs}} = \frac{-g_m V_{gs} * (r_d \| R_D)}{V_{gs}} \qquad \text{Since } I_D = -g_m V_{gs}$$

$$= \frac{-g_m r_d R_D}{r_d + R_D}$$

$$= \frac{-\mu R_D}{r_d + R_D}$$

Since $r_d >> R_D \qquad \therefore A_V = -g_m R_D$

Note: the potential divider biasing circuit improves the stability of the common source amplifier when being fed from a single DC supply V_{DD}. Both, resistor Rs and capacitor Cs, serves, basically the same function as the R_E and C_E in the C-E amplifier.

7.3 JFET Common Drain Amplifier:

It is similar to the common collector configuration of the BJT amplifier, it is also called source follower. A common-drain JFET amplifier is shown in figure 7.6(a). This configuration is characterized by a voltage gain of the less than unity and features a large current gain as a result of having very large input impedance and small output impedance.

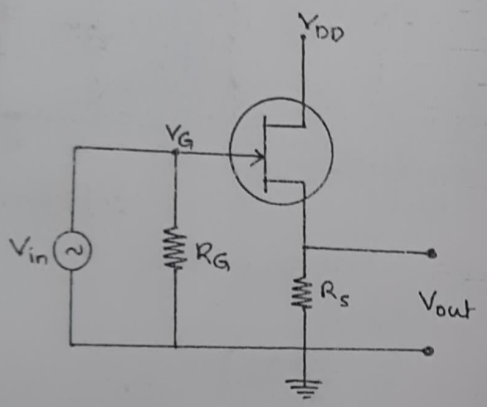


Figure: 7.6(a)

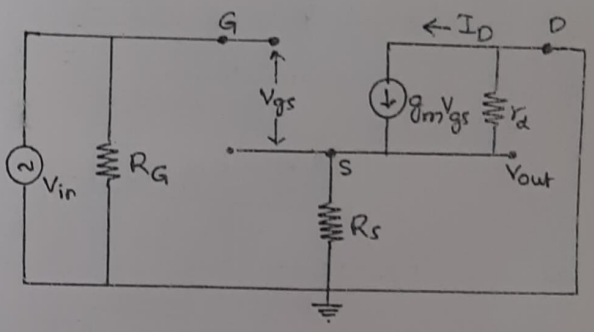


Figure: 7.6(b)

from figure 7.6(b), $V_o = I_D (r_d \| R_s)$ and $I_D = g_m V_{gs}$, $Z_i = R_G$

and $Z_o = r_d \| R_s$.

$\therefore V_o = g_m V_{gs} (r_d \| R_s)$

But $V_{gs} = V_G - V_s = V_i - V_o$

$\therefore V_i = V_{gs} + V_o = V_{gs} + g_m V_{gs} (r_d \| R_s) = V_{gs} [1 + g_m (r_d \| R_s)]$

$\therefore$ gain $A_V = \frac{V_o}{V_i} = \frac{g_m V_{gs} (r_d \| R_s)}{V_{gs} [1 + g_m (r_d \| R_s)]} = \frac{g_m (r_d \| R_s)}{1 + g_m (r_d \| R_s)}$

If $r_d >> R_s$ and $g_m R_s >> 1$, $A_V \approx \frac{g_m R_s}{g_m R_s} = 1$

⁂ MOSFETs :- The MOSFETs differs from the JFET in that it has no p-n junctions structure; instead, the gate of the MOSFET is insulated from the channel by a silicon dioxide (SiO_2) layer. Due to this the input impedance (resistance) of MOSFET is greater than JFET. Because of the insulated gate, MOSFETs are also called IGFETs (Insulated gate field-effect transistors)

* Depletion MOSFET (D-MOSFET) :-

—*— Construction of n-channel MOSFET :- Two highly doped n-regions are diffused into a lightly doped p-type substrate. These two highly doped n-regions represents source and drain. In some cases substrate is internally connected to the source terminal.

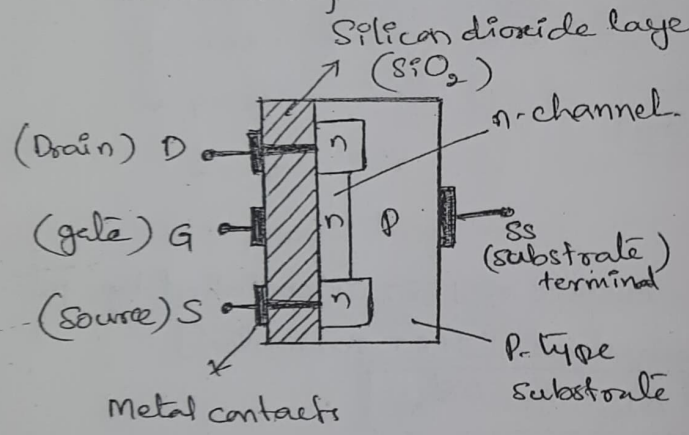


figure-1

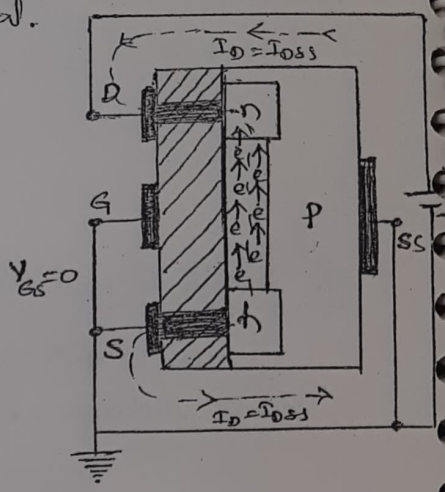
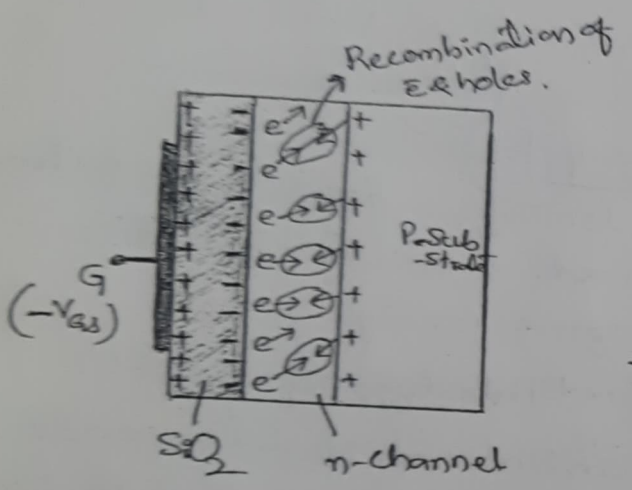


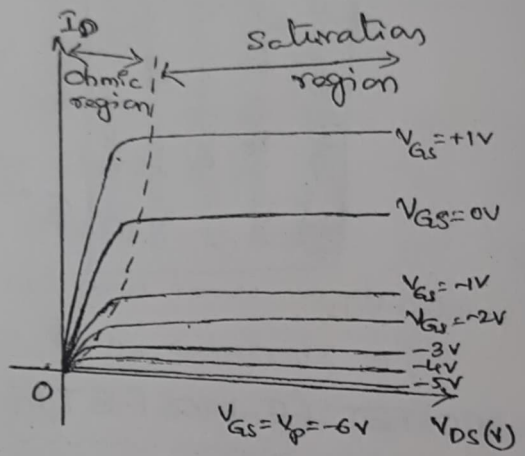
figure-2

The figure-1 shows the basic construction of n-channel D-MOSFE The source and drain terminals are connected through metallic conta to highly doped n-regions linked by an n-channel. The gate is also connected to a metal contact surface but remains insulated f the n-channel by a very-thin layer of dielectric material (SiO_2). Thus, there is no direct electrical connections between the gate ter -nal and the channel of a MOSFET, increasing the input impedance the device.

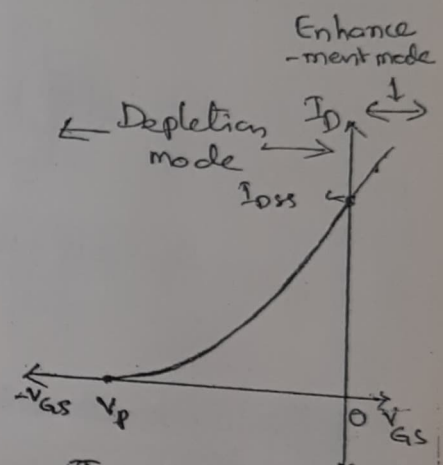
—*— Operation and characteristics of n-channel D-MOSFET :- On the application of drain-source voltage, V_{DS} and keeping gate-source voltage (V_{GS}) to zero by directly connecting gate terminal to the so

free $\bar{e}$s from the n-channel are attracted towards positive potential of drain terminal. This establishes current through the channel to be denoted as I_{DSS} at $V_{GS}=0V$, as shown in the figure-2. If we apply negative gate voltage, the negative charges on the gate, induces positive charges on the SiO_2 layer near the gate terminal and negative charge induces on the opposite side of the layer. This negative charge (induced) repel the conduction $\bar{e}$s from the channel, and attract holes from the P-type substrate. This initiates recombination of repelled $\bar{e}$s and attracted holes. The level of recombination between $\bar{e}$s and holes depends on the magnitude of the negative voltage applied at the gate. This recombination reduces the no of free $\bar{e}$s in the channel for the conduction, reducing the drain current.





Drain-characteristics of n-channel D-MOSFET



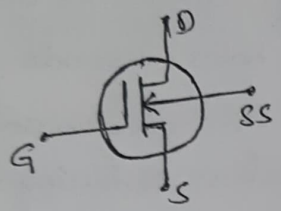
Transfer-characteristics of n-channel D-MOSFET

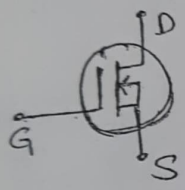
In other words we can say that, due to recombinations, n-channel is depleted of some of its $\bar{e}$s, thus decreasing the channel conductivity. The greater the negative voltage at the gate, the greater the depletion of $\bar{e}$s. The level of drain current will reduce with increasing negative bias for V_{GS} as shown in the transfer-characteristics of D-MOSFET.

For positive values of V_{GS}, the positive gate will draw additional $\bar{e}$s from the p-type substrate due to reverse leakage current and establish new accelerating particles. Because of this, as gate to source voltage increases in positive direction, the drain current also increases as shown in the transfer characteristics. The application of a +ve gate to source voltage has 'enhanced' the level of free carriers in the channel compared to $V_{GS}=0$. For this reason the region of positive gate voltages

on the transfer characteristics is referred to as enhancement region and the region between cut-off and the saturation referred to as depletion region. Another figure shows drain characteristics for an n-channel D-MOSFET. It is similar to that of JFET. The only difference is that it has positive part of V_{GS}.

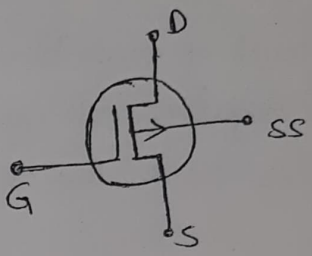
* D-MOSFET symbols:

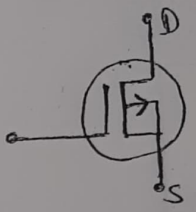




Symbols for n-channel D-MOSFETs.

*In the symbols insulation between gate and channel is represented by a space between the gate and other terminals of the symbol.



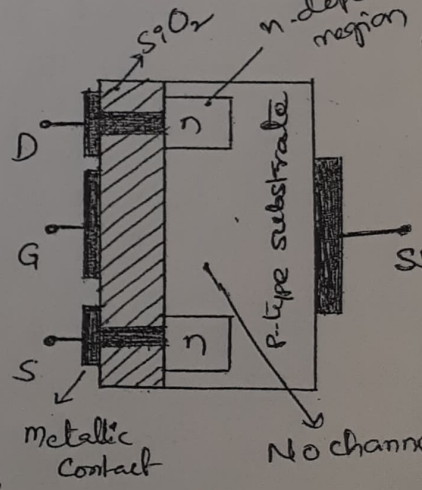


Symbols for p-channel D-MOSFETs.

** Enhancement MOSFET (E-MOSFET):- This type of MOSFET operates only in the enhancement mode and has no depletion mode. It differs in construction from the depletion MOSFET in that it has no physical channel.

* Construction of n-channel E-MOSFET.

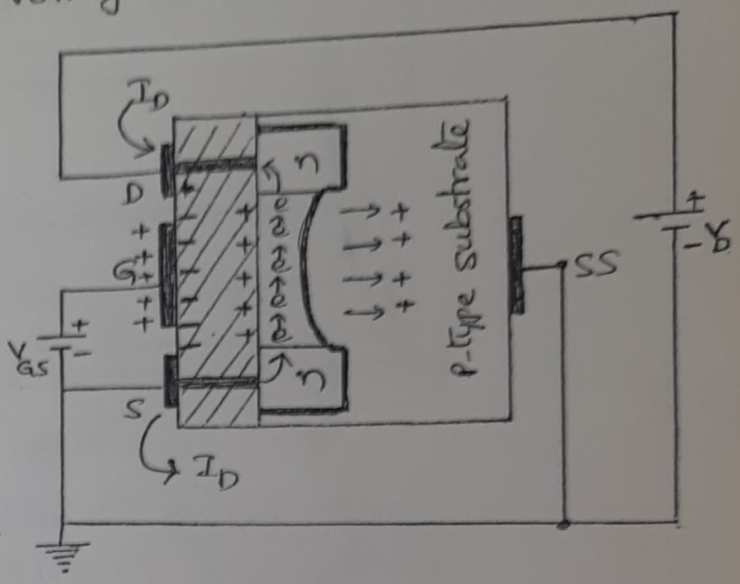
The figure shows the basic construction of n-channel enhancement MOSFET.



Like, depletion-MOSFET, two highly doped n-regions are diffused into a lightly doped p-type substrate. The source and drain are taken out through metallic contacts to n-doped regions. But the channel between two regions is absent in the enhancement MOSFET. The SiO_2 layer is still present to isolate the gate from the region between the drain and source, but now it is simply separated from a section of the p-type material (substrate).

* Operation and characteristics of n-channel E-MOSFET :-

On application of drain to source voltage V_{DS} and keeping gate to source voltage ($V_{GS}=0$) zero by directly connecting gate terminal to the source, Practically zero current flows- quite different from the depletion-MOSFET and JFET. If we apply ~~positive~~ V_{GS} and increase V_{GS} in the positive direction, the concentration of electrons near the SiO_2 layer surface increases. At a particular value of (+ve) V_{GS} there is a measurable current flow between drain and source. This value of V_{GS} is called threshold voltage denoted by V_T. Thus we can say that in an enhancement n-channel MOSFET, a positive gate voltage above a threshold value induces a channel and hence the drain current by creating a thin layer of negative charges in the substrate adjacent to the SiO_2 layer. The conductivity of the channel is enhanced by increasing the gate to source voltage and thus pulling more electrons into the channel. for any voltage below the threshold value, there is no channel.

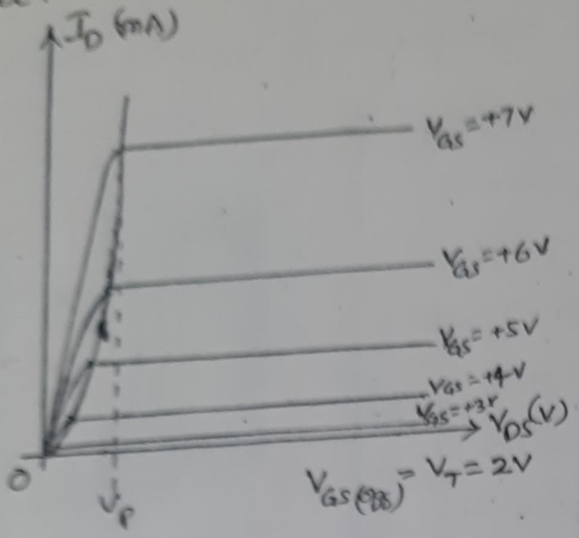


Since the channel does not exist with $V_{GS}=0V$ and 'enhanced' by application of a positive gate to source voltage, this type of MOSFET is called an enhancement-MOSFET.

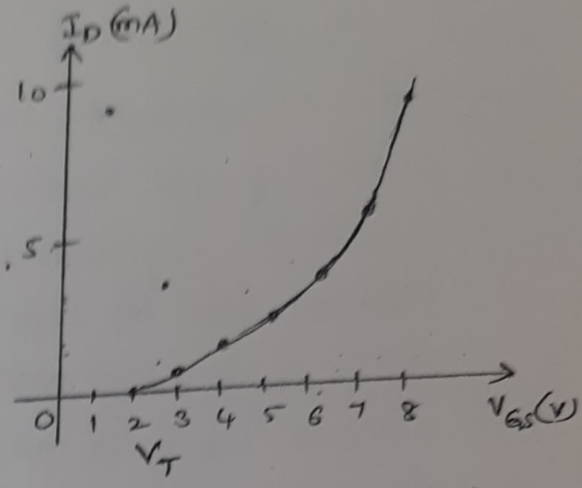
As V_{GS} is increased beyond the threshold level the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if we hold V_{GS} constant and increase the level of V_{DS}, the drain current will eventually reach a saturation level as occured in the JFET. The levelling off of I_D is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel.

The below figure shows the drain characteristics of an n-chann E-MOSFET. Looking at the figure we can say that as V_{GS} increases beyond the threshold level, the density of free carriers (ēs) in the

induced channel increases, increasing the drain current. However, at some point of V_{DS}, for constant V_{GS}, the drain current reaches a saturated level.



Drain characteristics for n-channel E-MOSFET.



Transfer characteristics for n-channel E-MOSFET.

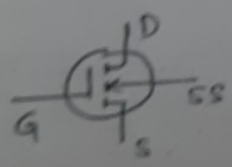
Transfer characteristics is quite different from characteristics that we obtained for JFET and D-MOSFET. for an n-channel E-MOSFET it is now totally in the positive V_{GS} region and as we know I_D does not flow until $V_{GS} = V_T$. for $V_{GS} > V_T$ the relationship between drain current and V_{GS} is non-linear and it is given as

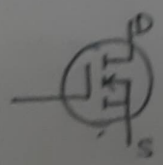
$$I_D = K(V_{GS} - V_T)^2$$

The K is a constant that is a function of the construction of the device. The value of K can be determined from eqn

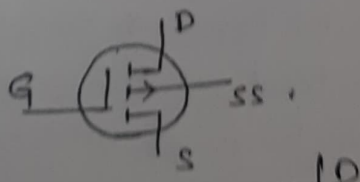
$$K = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}$$

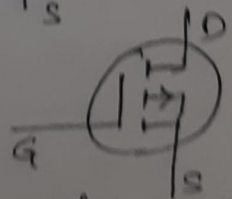
***E-MOSFET Symbols :-** Insulated gate is represented by a space and the dashed line between drain and source represents the fact that a channel does not exists between the two under no bias conditions.





n-channel E-MOSFET





P-channel E-MOSFET.

Applications: MOSFET as a VLSI Device.

MOSFETs are generally used in integrated circuits. These devices have a number of advantages over bipolar transistor as

1. Simpler fabrication process.
2. High packaging density.
3. Lower cost.
4. High impedance and lower power dissipation.
5. Complementary symmetry circuits.

** COMPARISON OF TRANSISTORS:-

Comparison of BJT and FET.

S.No	Parameter	BJT	JFET
1	Device type	Bipolar	Unipolar
2	Control element	current controlled device	voltage controlled device.
3	Types	n-p-n & p-n-p.	n-channel & p-channel.
*	configurations	CB, CE, CC	CS, CG, CD.
5	Input resistance	less compared to JFET	High compared to BJT
6	Size	Bigger than JFET	smaller in Construction.
7	Sensitivity	Higher sensitivity to changes in the applied signals	Less sensitivity to changes in the applied voltage.
8	Thermal runaway	Exists in BJT	Does not exists in JFET.
9	Gain factor	$\beta = \frac{\Delta I_C}{\Delta I_B}$	$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$
10	Gain bandwidth Product	High	Low.

* Comparison of JFET and MOSFET

S.no	Parameter	JFET	MOSFET
1.	Types	n-channel p-channel	n-channel } D-MOSFET p-channel } n-channel } E-MOSFET. p-channel }
2.	operation modes	operated in depletion mode only	operated in depletion and Enhancement modes.
3.	Input impedance	High(≥10 MΩ)	very high (≥10,000 MΩ
4.	Gate	Gate is not insulated from channel	Gate is insulated ~~from~~ fr channel by a layer of Si
5.	channel	channel exists permanently	channel exists permanent in depletion type MOSFET, not in E-MOSFET.

S.no.	Parameters	D-MOSFET	E-MOSFET.
1.	Types	n-channel p-channel	n-channel p-channel.
2.	channel	Exists permanently	channel is physically ab It is induced after applica of reverse gate voltage.
3.	operation mode	can be operated in depletion mode as well as enhancement mode.	can only be operated enhancement mode.

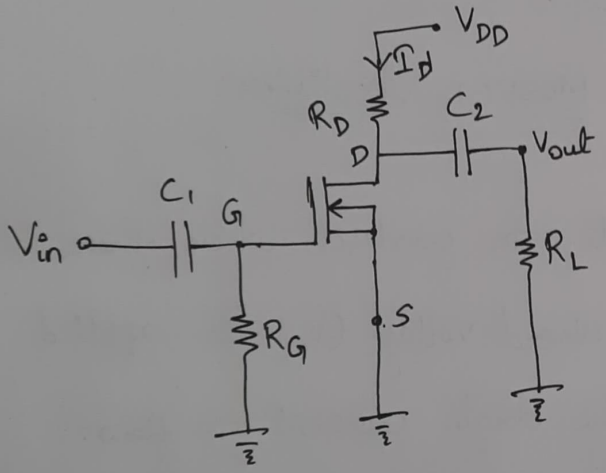
MOSFET Amplifiers

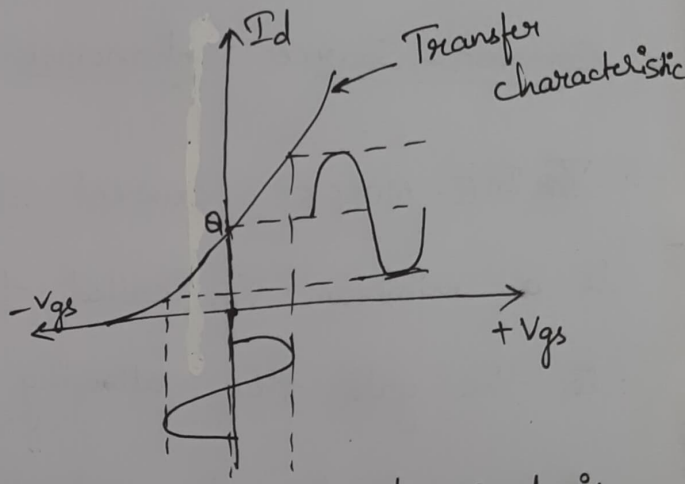
→ To produce linear amplification, MOSFET has to operate in its saturation region.

→ It needs to be biased around a centrally fixed Q-point.

Common-Source Depletion MOSFET Amplifier:

→ Source terminal is common for both input & output.





→ Gate is at approximately 0V dc & the source terminal is grounded, thus making $V_{gs} = 0V$.

→ When V_{in} is applied, V_{gs} swings above & below its zero value, producing a swing in drain current I_d.

→ During +ve half cycle of the signal, the +ve voltage on the gate increases & produces the enhancement mode. This increases the channel conductivity & hence the drain current Id.

→ During -ve half cycle, the +ve voltage decreases & produces depletion mode. This decreases the conductivity & hence I_d.

→ A small change in gate voltage produces a large change in drain current I_d.

→ Large variation in I_d produces a large a.c o/p voltage across R_D.

→ Voltage gain $A_V = g_m R_D$ or $A_V = g_m R_D'$ ($R_D' = R_D \| R_L$)

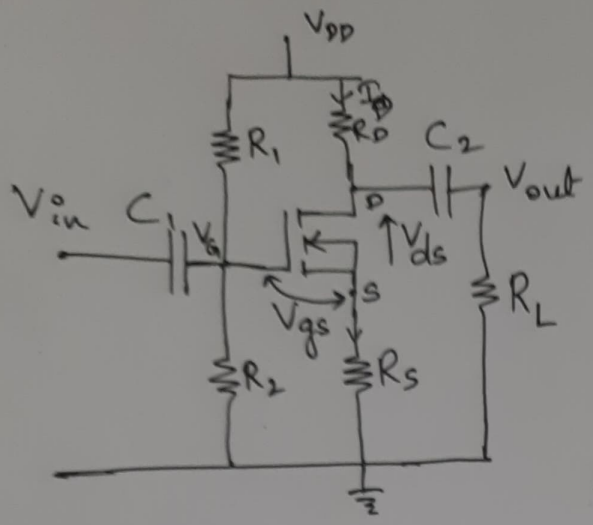
* Common-Source Enhancement MOSFET Amplifier:

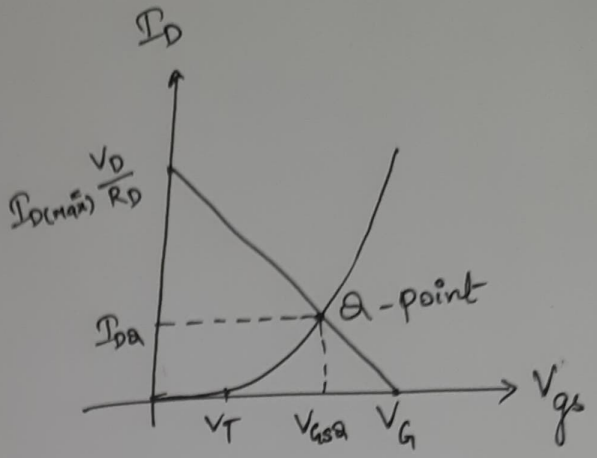
→ In E-MOSFET, current starts to conduct when there is a minimum V_{gs} called threshold voltage (V_T) is applied to the gate thus allowing the drain current to flow.

→ E-MOSFET doesnot conduct until the V_{gs} is less than V_T.

if $V_{gs} \geq V_T$, E-MOSFET starts conducting.

→ If forward bias at the gate increases, I_d will also increase making the E-MOSFET ideal for use in MOSFET amplifier circuits.





$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

$$= I_D (R_D + R_S) + V_{DS}$$

$$\Rightarrow R_D + R_S = \frac{V_{DD} - V_{DS}}{I_D}$$

$$V_{GS} = V_G - I_S R_S$$

→ V_{GS} should be greater than V_T, & $I_S = I_D$

$$V_{GS} = V_G - I_D R_S$$

$$\therefore V_G = V_{GS} + I_D R_S$$

(or) $V_G = V_{GS} + V_S$

→ Since, no current flows into the gate terminal of a MOSFET

$$V_G = V_{DD}\left(\frac{R_2}{R_1 + R_2}\right)$$

Sl. No	Tutorial - I	BTLs	COs	Marks
1	Explain about depletion region	2	1	5
2	Discuss the reverse biasing of PN junction diode	2	1	3
3	Draw and explain the V-I characteristics of a PN Junction diode	2	1	3
4	Explain how does the reverse saturation current of a PN diode vary with temperature	2	1	2
5	Sketch the diode equivalent circuits and mention the various applications of diode	2	1	5

Sl. No	Tutorial – II	BTLs	COs	Marks
1	Discuss the construction of a NPN Transistor in detail	2	2	5
2	Discuss the construction of a PNP Transistor in detail	2	2	5
3	State the two junctions in a transistor.	1	2	3
4	Explain the working principle of NPN transistor	2	2	4
5	Explain the working principle of PNP transistor	2	2	4

Sl. No	Tutorial - III	BTLs	COs	Marks
1	What is Zener diode. Draw and explain the characteristics of Zener diode.	2	3	4
2	Discuss avalanche and Zener breakdown	2	3	4
3	Zener diode can be used as a voltage regulator. Justify.	5	3	3
4	Explain the construction of a SCR	2	3	4
5	Draw and explain the characteristics of tunnel diode. State its applications.	2	3	4

Sl. No	Tutorial - IV	BTLs	COs	Marks
1	Derive the hybrid model for a CE transistor	2	4	5
2	Sketch the h-parameter equivalent circuit for a CE, CC, CB transistor	3	4	5
3	Explain how transistor can be used as an amplifier with the help of a DC load line	2	4	5
4	Derive the expressions for Ai, Ri, Ro, Av for a CC amplifier	2	4	5
5	Derive the expressions for Ai, Ri, Ro, Av for a CE amplifier	2	4	5

Sl. No	Tutorial - V	BTLs	COs	Marks
1	Define amplification factor of JFET	1	5	2
2	Define MOSFET. State its types.	1	5	3
3	Explain the construction of a N-channel depletion type MOSFET.	2	5	4
4	Explain the working of a N-channel depletion type MOSFET.	2	5	4
5	Explain the working of a N-channel enhancement type MOSFET.	2	5	4

Sl. No	Assignment - I	COs
1	Explain VI characteristics of PN diode in forward bias and reverse bias with sketches	1
2	a) Calculate dynamic forward resistance of silicon PN junction diode when applied voltage is 0.25v at T = 27^0C with $I_0 = 2\mu A$. b) Determine forward current in case of PN junction diode with I0 = 10μA, V_f=0.8V, at T = 300k, Assume silicon diode.	1
3	Derive the equation for transition capacitance C_T.	1
4	a) Explain diode equivalent circuits. b) Explain positive clipper circuit with biasing	1
5	Draw and explain the operation of Full wave rectifier with L-section filter and find ripple factor.	1
6	a) Calculate I_{dc}, V_{dc} and ripple factor for an input of V_{in} = 30sin(100πt)v. b) Calculate I_C and I_E for a transistor with $\alpha = 0.99$ and $I_{C0} = 5\mu A$, $I_B = 20\mu A$.	1
7	a) Explain the input and output characteristics of common collector configuration with neat sketches. b) What is early effect? What are the consequences of it?	2
8	Explain the D.C. load line analysis of Transistor.	2
9	What is the need of biasing? Explain voltage divider bias method.	2
10	What is clamping circuit theorem? Explain positive and negative clampers.	1
11	Explain how transistor works as an amplifier and as switch.	2
12	Explain the working of npn and pnp transistors.	2

Electronics Devices and Circuits

Assignment - I

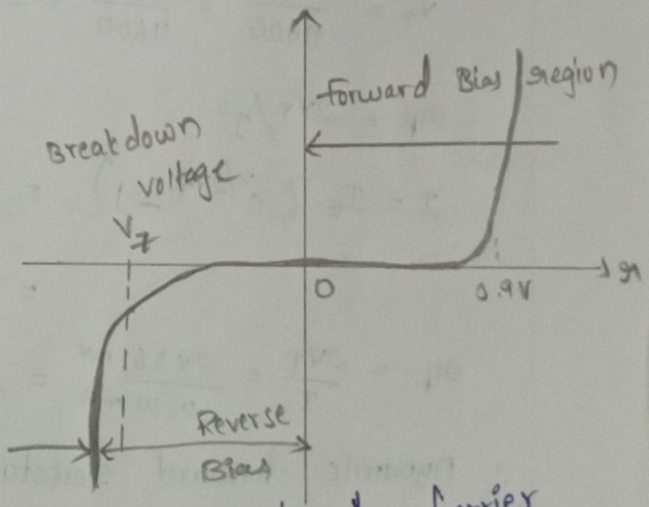
Name: L. Rakesh
Branch: ECE-B
Roll No: 484

1) Explain the V-I characteristics of PN diode in forward bias and Reverse bias with sketches?

Ans:- The diode has non-linear V-I characteristics i.e., relationship between the current flowing through the diode and voltage appearing across it is non-linear.

(i) Forward Bias:

In this P-side of PN junction connected to positive voltage and N side connected to negative voltage supply. Simply, forward bias region is the characteristics of diode for $V>0$. Initially, diode current is very small because the barrier potential presents in the flow of current through it. If applied voltage exceeds the barrier potential, then for a increase in voltage increases in current starts to increase rapidly is called Cut-in-voltage of diode, denoted by V_f, for silicon $V_f = 0.7$, Germinium $V_f = 0.3$.



(ii) Reverse Bias:

In this P-side connected to negative and N-side connected to positive of voltage supply for reverse bias region is characteristics of diode for $V<0$. The diode current is very small, almost equal to zero for all values of voltage less than breakdown voltage V_Z.

this is because in reverse bias the width of P, becomes very high and practically no current flows Circuit.

2)

a) Calculate dynamic resistance of silicon PN junction diode applied voltage forward is 0.25V at $T=27^{\circ}C$ with $I_0 = 2\mu A$

Ans:- Given

$V = 0.25V$, $T = 27^{\circ}C = 300K$, $I_0 = 2\mu A = 2\times10^{-6}$

η = emission factor = 2

$$V_T = \frac{T}{11600} = \frac{300}{11600} = 0.0258 = \frac{0.026\times10^{-3}}{10^{-3}} = 26\,mV$$

$$r_f = 2V_T/I$$

$$I = I_0\left(e^{V/2V_T} - 1\right) = 2\times10^{-6}\left(e^{0.25/2\times26\times10^{-3}} - 1\right)$$

$$= \frac{2.428}{10}\times10^{-4}\times10 = 0.24\,mA$$

$$r_f = \frac{2V_T}{I} = \frac{2\times26\,mV}{0.24\,mA} = 216.66\,\Omega$$

∴ Dynamic forward resistance (r_f) = 216.66Ω

b) Determine forward current in case of PN junction diode with $I_0 = 10\mu A$, $V_f = 0.8V$, at $T = 300K$, Assume silicon diode.

Ans:- Given

$I_0 = 10\mu A$, $V_f = 0.8V$, $T = 300k$, silicon diode (η) = 2

$V_T = 26\,mV$

$I = I_0\left(e^{V/2V_T} - 1\right)$

$I = 10\times10^{-6}\left(e^{0.8/2\times26\times10^{-3}} - 1\right)$

$= 48.00V$ $\boxed{I = 48A}$

∴ forward bias current = 48A.

3) Derive the equation for transition Capacitance (C_T) ?

We know that,

from poisson's Equation

$$Q = eN_A A w \quad \text{—①} \qquad \left[\because C_T = \frac{dQ}{dv}\right]$$

Again

$$\frac{d^2V}{dx^2} = e.\frac{N_A}{\epsilon} \qquad V \propto w \propto x$$

$$d^2V = e.\frac{N_A}{\epsilon} dx^2$$

Taking double integration

$$V = \int_0^w \int e.\frac{N_A}{\epsilon} dx^2$$

$$V = e.\frac{N_A}{\epsilon}\left(\frac{x^2}{2}\right)_0^w \Rightarrow V = e.\frac{N_A}{\epsilon}.\frac{w^2}{2}$$

diff. w.r.t 'V'

$$\frac{dx}{dv} = e\frac{N_A}{\epsilon}\left(\frac{2w}{2}\left|\frac{dw}{dv}\right|\right)$$

$$\frac{dw}{dv} = \frac{\epsilon}{eN_A w} \quad \text{—②}$$

from eq① diff w.r.t 'V'

$$\frac{dQ}{dv} = eN_A.A\frac{dw}{dv}$$

Sub ② in above equation

$$\frac{dQ}{dv} = eN_A.A\left(\frac{\epsilon}{eN_A w}\right) \Rightarrow \frac{dQ}{dv} = \frac{\epsilon A}{w}$$

$$\therefore \boxed{C_T = \frac{\epsilon A}{w}}$$

4)

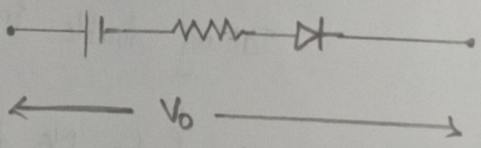
a) Explain diode equivalent Circuits?

Ans:

Equivalent Circuit Consists of a Current with one or two diodes connected in parallel and two resistors, one Connected in parallel and other one series, to take into account amount energy losses in this model.

→ There are three model of diode.

(i) Piece wire linear model:



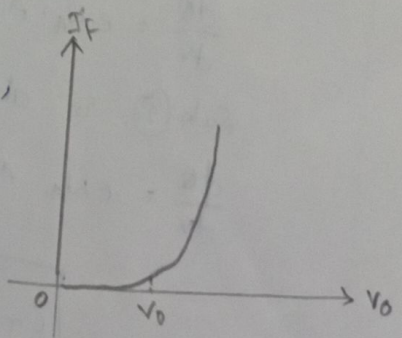
When diode is forward biased by applying +ve voltage V_D across it. The diode will not conduct until V_D is greater than P.B voltage 'V_γ' at junction. While conducting it flowing the diode Causes voltage drop due to forward resistance V_D applied across the diode has to overcome.

(a) P.B 'V_γ' (b) voltage drop $I_F V_F$ $V_D = V_\gamma + I_F V_F$.

VI characteristics of this model are shown in the above.

→ Since the characteristics are linear piece wise, it is Called piece wise linear model. Further, V-I Characteristics are approx equivalent to original V-I characteristics of PN diode. Hence, known as approx equivalent Circuit mode.

V-I characteristics of piece wise linear model.



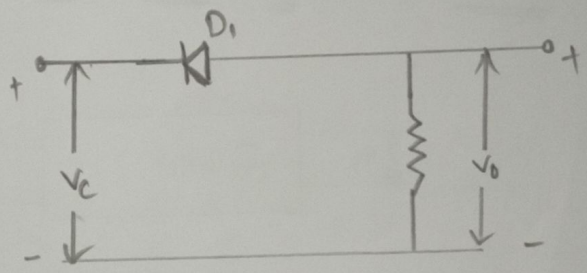
ii) Simplified model:

When the diode is connected in a circuit, it's internal resistance r_f, is very small in comparision with other eliminates in the circuit. Hence, it can be neglected. This results in a simplified model.

→ In this, the positive part of the output is clipped-off i.e., the output contains only negative part of the input.

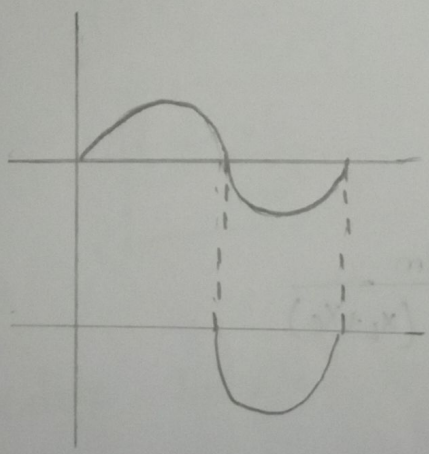
b) Explain positive clipper circuit with biasing?

Positive series clipper:

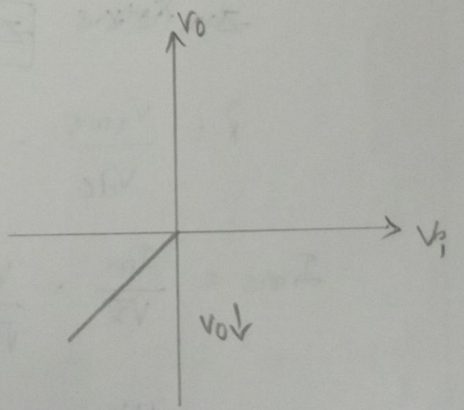


When the input v_i positive, diode does not conduct and the output $V_o = 0$.

→ When the input V_i is negative, diode conducts and the output 'V_o' is a replicable of input. The output contains only negative part of the input.



Input and output wave form



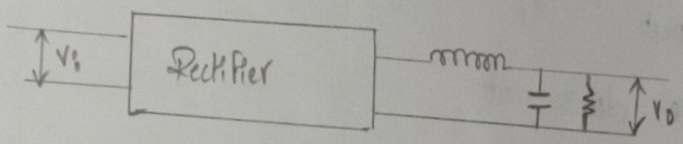
Transfer Characteristics

5) Draw and Explain the operation of full wave L or section filter and find ripple factor?

Ans: Full Wave rectifier:

A full wave rectifier is defined as a rectifier Converts the Complete cycle of alternating Current into pulsating DC. Unlike half wave rectifiers that utilize only the halfwave of the input AC cycle, full wave rectifiers utilize the full cycle.

L- section (or) LC section filter:



$$\gamma_1 = \frac{R_L}{3\sqrt{2}\,\omega L}$$

$$\gamma_c = \frac{1}{4\sqrt{3}\,f_c R_L}$$

$$V_{dc} = \frac{2V_m}{\pi} \Rightarrow V_m = \frac{4V_m}{3\pi}$$

$$\boxed{Z = X_L + X_C}$$

$$\gamma = \frac{V_{rms}}{V_{dc}} = \frac{I_{rms}}{I_{dc}}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{V_m}{\sqrt{2}\,Z} = \frac{V_m}{\sqrt{2}\,(X_L + X_C)}$$

$$I_{rms} = \frac{4V_m}{3\pi\sqrt{2}\,(X_L + X_C)}$$

$$I_{dc} = \frac{2I_m}{\pi}$$

∴ forward

$$V_{rms} = \frac{4V_m}{3\pi\sqrt{2}(X_L + X_C)} X_C$$

$V_{ac} = I X_C$

$V_{ac} = I_{ac} X_C$

$V_{rms} = I_{rms} X_C$.

$$V_{rms} = \frac{4V_m}{3\pi\sqrt{2}X_C\left(\frac{X_L}{X_C}+1\right)} X_C$$

$$V_{rms} = \frac{4V_m}{3\pi\sqrt{2}\left(\frac{X_L}{X_C}+1\right)}$$

$$\gamma = \frac{\frac{4V_m}{3\pi\sqrt{2}\left(\frac{X_L}{X_C}+1\right)}}{\frac{2V_m}{\pi}}$$

$$\therefore \gamma = \frac{2}{3\sqrt{2}}\left[\frac{1}{\left(\frac{X_L}{X_C}+1\right)}\right] \Rightarrow \frac{2}{3\sqrt{2}}\left(\frac{1}{\frac{X_L}{X_C}}\right)$$

$$\therefore \gamma = \frac{3}{2\sqrt{2}} \cdot \frac{X_C}{X_L} \Rightarrow \gamma = \frac{\sqrt{2}}{3}\frac{X_C}{X_L}$$

$$\gamma = \frac{\sqrt{2}}{3}\frac{\frac{1}{2\omega C}}{2\omega L}$$

$$\gamma = \frac{\sqrt{2}}{3}\frac{1}{4\omega^2 LC}$$

$$\therefore \boxed{\gamma = \frac{\sqrt{2}}{12\omega^2 LC}}$$

a) Calculate I_{dc}, V_{dc} and ripple factor for an input of $V_{in} = 30 \sin(100\pi t)$ V.

Ans: Given

$$V_{in} = 30 \sin(100\pi t) V$$

$$V_m = 30V, \quad \omega = 100\pi$$

for half wave rectifier

(i) $V_{dc} = \frac{2V_m}{\pi} = \frac{2 \times 30}{3.14} = 19.10\ V$

$$I_{dc} = \frac{V_{dc}}{R} = \frac{19.10}{1000} = 0.0191$$

Ripple factor $= V_{rms} = \frac{V_m}{\sqrt{2}} = \frac{30}{\sqrt{2}} = 21.21V$

HWR

$$V_{dc} = \frac{V_m}{\pi} = \frac{30}{3.14} = 9.55$$

$$I_{dc} = \frac{V_{dc}}{R} = \frac{955}{1000} = 9.55 \times 10^{-3}$$

$$V_{rms} = \frac{V_m}{2} = \frac{30}{2} = 15$$

$$\gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{15}{19.55}\right)^2 - 1}$$

$$\therefore \boxed{\gamma = 1.21}$$

Calculate I_C and I_E for a transistor with $\alpha = 0.99$ and $I_{CO} = 5\,\mu A$, $I_B = 20\,\mu A$?

Ans: Given

$\alpha = 0.99$, $I_{CO} = 5\,\mu A$, $I_B = 20\,\mu A$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CO}$$

$$I_C = \frac{0.99}{1-0.99} \times 20 \times 10^{-6} + \frac{1}{1-0.99} \times 5 \times 10^{-6}$$

$$\boxed{I_C = 2.48\ mA}$$

$$I_E = I_B + I_C$$

$$= 20 \times 10^{-6} + 2.48 \times 10^{-3}$$

$$\boxed{I_E = 2.5\ mA}$$

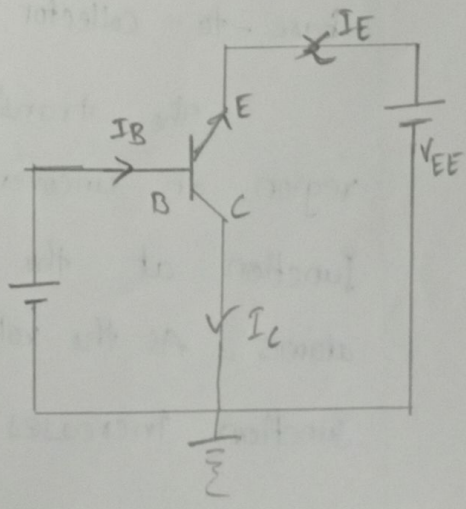
$\therefore I_C = 2.48\ mA$ and $I_E = 2.5\ mA$.

(7)

a) Explain the input and output characteristics of Common Collector Configuration with neat sketches?

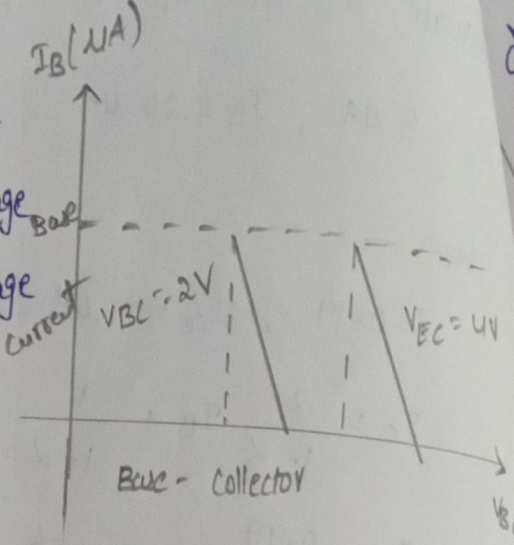
Ans: The Configuration in which Collector is Common to both the input and output is known as Common Collector Configuration.

In this arrangement the base, emitter and collector acts as input, output and common terminals respectively. The collector is at grounded potential. It is also referred as grounded Collector Configuration.



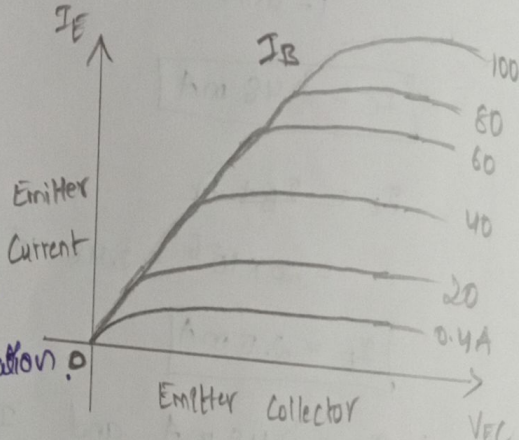
Input characteristics of CC:

The curve plotted between base current 'I_B' and base-collector voltage 'V_{BC}' keeping emitter-collector voltage 'V_{EC}' constant, gives the input characteristics of CC configuration.



output characteristics of CC:

The curve plotted between emitter current 'I_E' and emitter collector voltage 'V_{EC}' keeping base current voltage 'V_{BC}' constant, gives output characteristics of CC configuration.



(b) What is Early effect? What are consequences of it?

Ans: Early effect:

Early effect is also called as base width modulation. The early effect is the variation in the width of the base in a bipolar transistor due to a variation in the applied base-to-collector voltage.

The transistor region at a junction is the region of uncovered charges on both sides of the junction at the positions occupied by the impurity atoms. As the voltage applied across the common-base junction increases, the transition region penetrates

deeper into the collector and base.

→ since the doping in the base is lower than that of the collector, therefore, the penetration of the transition region into the base in much larger than into the collector. As a result the electrical base width of the transistor is reduced in comparision to metallurgical base width. This modulation of the effective base width by the collector voltage is known as the early effect.

This decrease of the base width with increasing reverse collector voltage has some consequences such as;

i) there is less chance for recombination within the base region.

ii) The concentration gradient of minority charge carriers is increased with in the base. Since the hole current injected across the emitter is proportional to the gradient of the minority carriers at the emitter junction, the emitter-current increases with increasing reverse collector voltage.

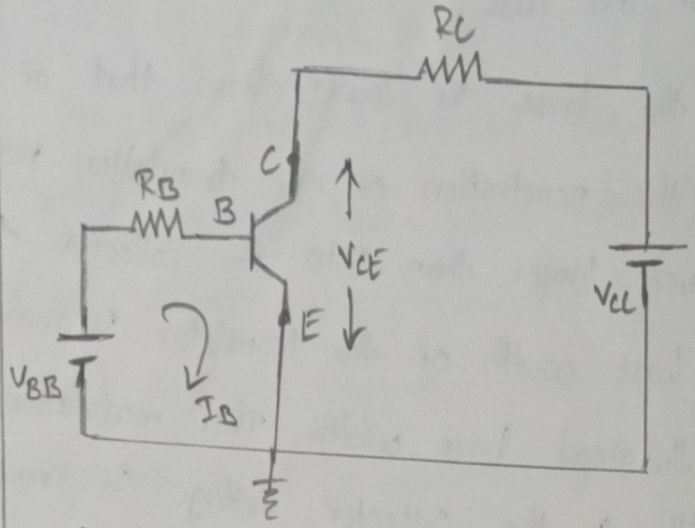
3) for the extremely large voltages, base width may be reduced to zero causing the voltage to breakdown in the transistor. this phenomena is known as punch through or reach through effect.

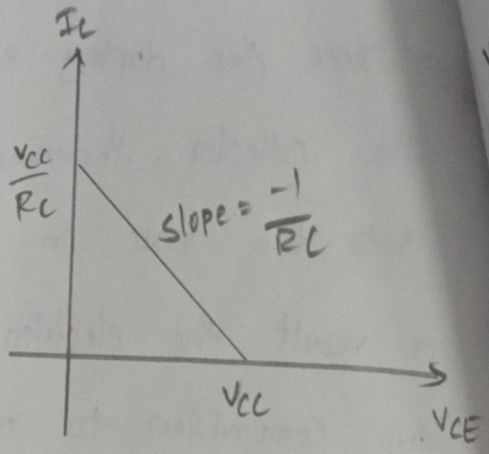
8) Explain the DC load line analysis of transistor?

Ans: DC load analysis:

from KVL

$$V_{CC} = I_C R_C + V_{CE} \quad \text{(1)}$$





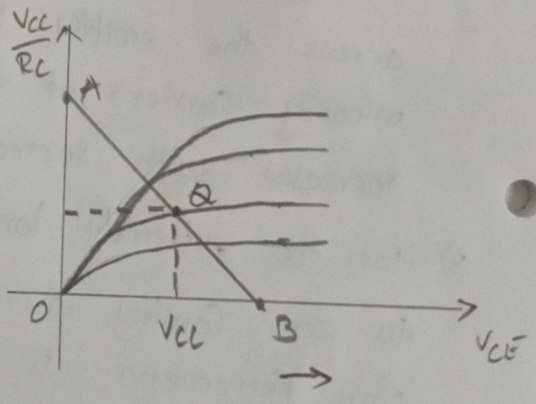
The line drawn in slope is known as DC load line. Since eq① is derived under DC conditions and the slop depends on load RC if it is known as DC-load line.

→ The line is super imposed on output characteristics of transistor to obtain zero signal collectors current 'I_C' and maximum zero signal Collector to emitter voltage 'V_{CE}'.

(i) When $V_{CE} = 0$, eq① becomes

$I_C = \frac{V_{CC}}{RC}$ is using in the region of saturation of transistor.

$\left(0, \frac{V_{CC}}{R_C}\right)$



(ii) When $I_C = 0$, eq①

$V_{CE} = V_{CC}$ Cut off region of the transistor.

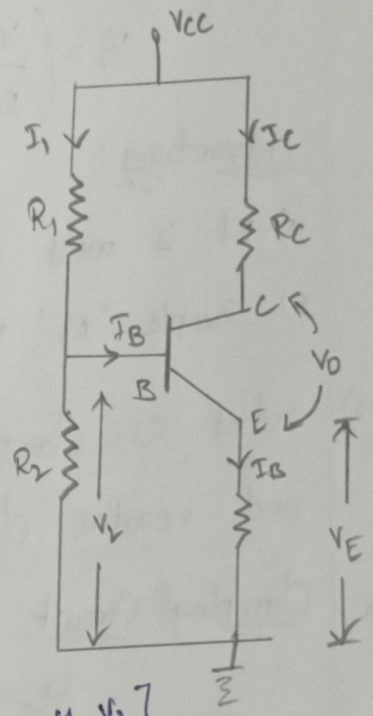
(iii) Except this two point, all other points lie in the active region.

∴ The line encompasses all the points from Saturation to Cut-off active region.

What is need of biasing? Explain voltage divider bias method?

The most extensively used biasing circuit for maintaining stabilization is voltage divider biasing.

→ The circuit contain two resistors R_1 and R_2 connected to V_{CC} in base section of transistors. Voltage drop across R_2 forward bias, the emitter base function. The RE connected to emitter grant stabilization.



$$I_1 = \frac{V_{CC}}{R_1 + R_2}$$

I_1 flowing through R_1 and R_2, where R_1 and R_2 are in series [voltage drop across V_2]

$$V_2 = \left(\frac{R_2}{R_1+R_2}\right) V_{CC} \quad -(2)$$

$$V_2 = V_{BE} + V_E \Rightarrow V_{BE} + I_E R_E$$

$$I_E = \frac{V_2 - V_{BE}}{R_E} \quad -(3)$$

$$I_C = \frac{V_2 - V_{BE}}{R_E} \quad -(4) \qquad [\because I_E \approx I_C]$$

Apply KCL to output side,

$$V_{CC} = I_C R_C + V_{CE} + V_E$$

$$= I_C R_C + V_{CE} + I_E R_E$$

$$V_{CE} = V_{CC} - I_C(R_E + R_E)$$

from eq (4)

$$V_{CC} = I_C R_C + V_{CE} + V_E$$

$$= I_C R_C + V_{CE} + I_E R_E$$

$$V_{CE} = V_{CC} + \quad V_2 = V_{BE} + I_C R_E$$

voltage V_2 is independent of I_C and is given as,

$$V_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2$$

Advantages:

1) It is most popular biasing circuit.

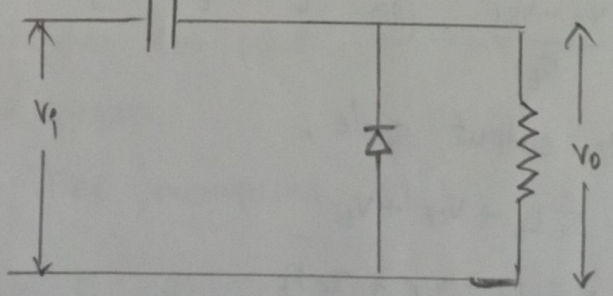
2) Simple 'R_E' resistance provides good stability.

10) What is clamping circuit theorem? Explain positive and negative clampers?

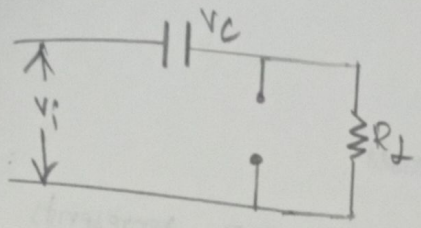
Ans: Clamping Circuit Theorem:

The clamping circuit theorem states that under steady state conditions, for any input wave form the ratio of the area under the output voltage curve in the forward direction to that in the reverse direction is equal to the ratio R_f/R.

(i) Negative clamping:



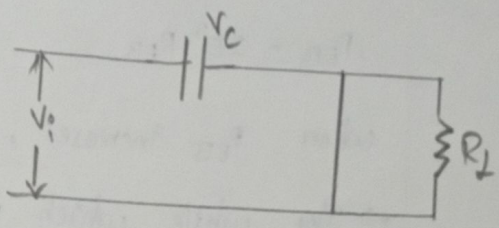
Negative half cycle



$V_i + V_C + V_o = 0$

$\boxed{V_o = -2V_i}$

Positive half cycle

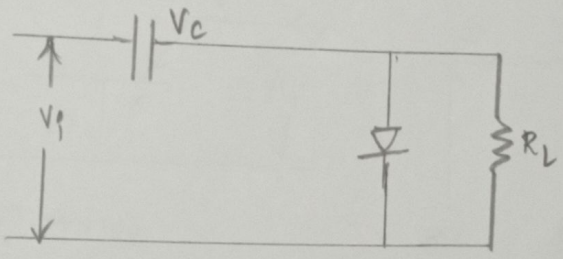


$-V_i + V_C = 0$

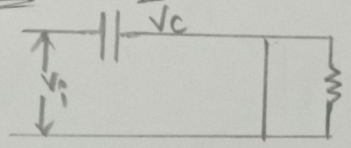
$V_i = V_C$

$\boxed{V_o = 0}$

(ii) positive clamping



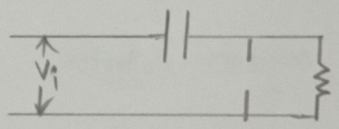
Negative half cycle



$V_i + V_C = 0 \Rightarrow V_i = -V_C$

$\Rightarrow \boxed{V_o = 0}$

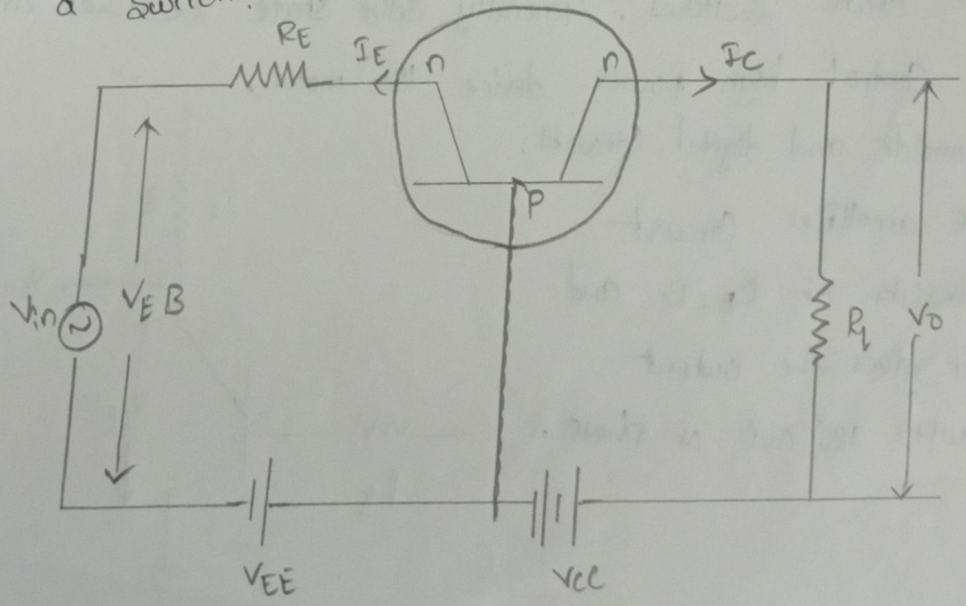
positive half cycle



$V_i + V_C - V_o = 0$

$\boxed{V_o = 2V_i}$

(11) Explain new transistor works as an amplifier and as a switch.



$V = V_{in} + V_{EB}$

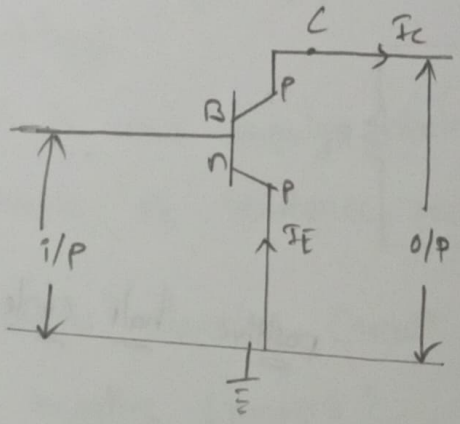
$P_{EB} = I_E^2 R_{EB}$

when P_{EB} increases, R_{EB} increases.

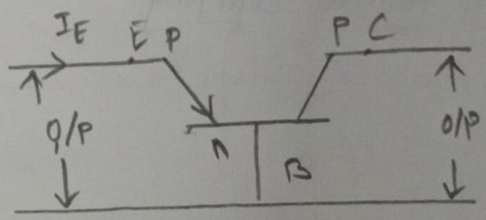
→ The while which present in n-p-n represents neat present in it.

→ It is a configuration of common base.

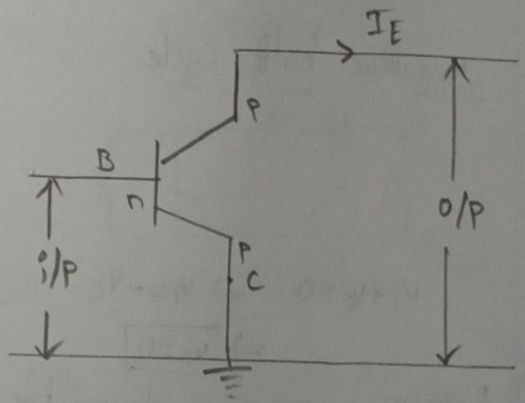
P-n-P:



Common Collector



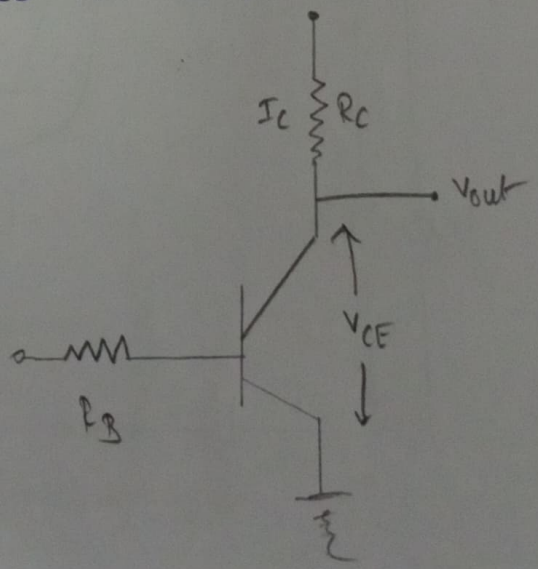
Common Base



Transistor as a Switch:

One of the main applications of transistors are solid state switches. Generally solid state switches are used to control high power device like motor, solonoids and digital circuits.

→ CE amplifier circuit consists of R_B, R_C and it gives the output with 180° out of phase.



Sl. No	Assignment - II	COs
1	Explain with neat sketch the construction and working of FET.	3
2	Explain the drain and transfer characteristics of N-channel JFET.	3
3	a. Define all JFET parameters. b. Explain biasing methods of JFET.	3
4	a. Explain the characteristics of Zener diode. b. Explain different types of breakdown mechanisms.	3
5	With neat sketches explain the working of Tunnel diode along with its characteristics.	3
6.	Explain the construction and working principle of Silicon Controlled Rectifier (SCR).	3
7	Explain how to determine h-parameters from transistor characteristics (CE).	4
8	a. Explain transistor amplifying action. b. Design CE amplifier and explain its working.	4
9	Explain small signal analysis of transistor (h-parameter model).	4
10	a. Give the typical values of h-parameters for CB, CC and CE configurations. Also give conversion formulae between them. b. Explain Simplified Hybrid model and derive the parameters for CB configuration.	4

Electronics Circuits And Devices

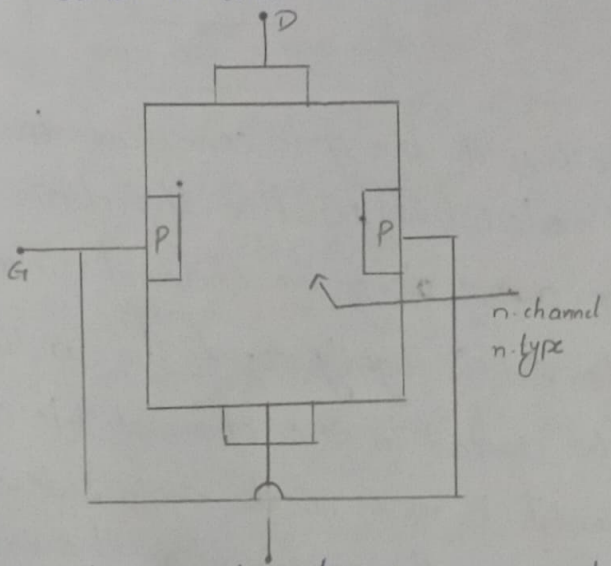
P. Sneha Sree
20VE1A0429
ECE-II-A

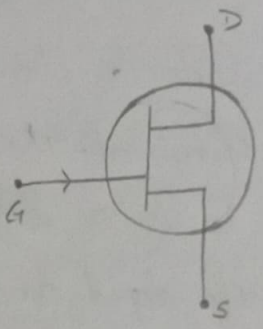
Assignment II (5)

1. Explain with neat sketch the construction and working of FET?

Construction of FET:-

Actually JFET is classified into two types n-channel and P-channel JFET. So let us discuss about n-channel JFET.





A small bias of Extrinsic semiconductor material, n-type is taken and at its two ends, two ohmic contacts are made they are drain(D) & source(S) terminals of FET.

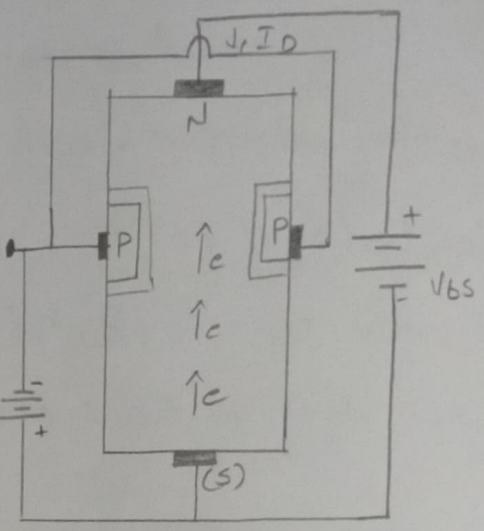
Heavily doped electrodes of P-type material form P-n junctions on each side of the bar.

→ The e^s Enter the channel through the terminal called source and leave through the terminal drain. The terminals taken out from heavily doped electrodes of P-type material are called gates.

Working:-

The P-n junction between gate and source is always kept in reverse biased condition since the current in reverse biased P-n junction is extremely small, It can be assumed as zero;

Let us assume that $V_{GS} = 0$. The voltage V_{DD} is applied between Drain and Source. Due to applied voltage the majority carriers start flowing from Source to drain through the space b/w the gates region.



Now consider n-channel JFET with the gate connected to Source terminal. The n-type material is resistive the drain current causes a voltage drop across along the channel. Since gate is heavily doped and the channel is lightly doped. The width of depletion region will mainly be spread in the channel. We can observe that the depletion width is more at the drain side and as compared to source side because the new junction the voltage at drain side is more and the voltage at source side is less. So reverse bias is not uniform i.e, it gradually increases from Source to drain.

2. Explain the drain and transfer characteristics of N-channel JFET

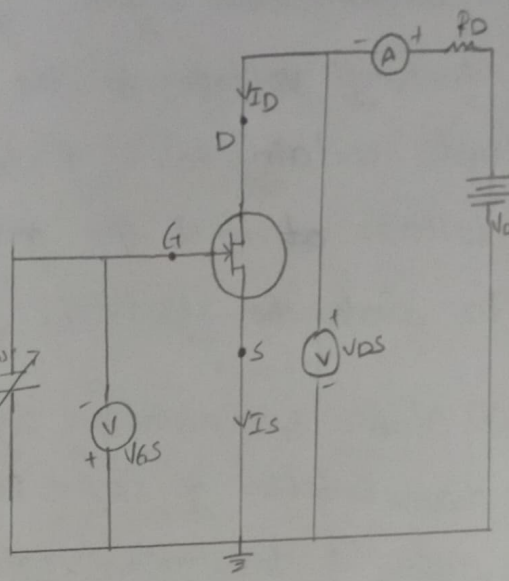
Drain V-I characteristics for n-channel JFET:-

The circuit shows the Experimental setup required to plot the drain characteristics.

(1) V_{GS} & V_{DS} both = 0

When $V_{GS} = 0$ the channel is Entirely open but $V_{DS} = 0$, so there is no force for the majority charge carries and hence drain current does not flow.

(2) $V_{GS}=0$, $V_{DS}\neq 0$;



At $V_{GS}=0$, in response to small applied voltage V_{DS}, the n-type bar acts as a simple semi-conductor resistor and the current I_D increases linearly with V_{DS}. As V_{DS} increases the voltage drop along the channel also increases. This increases the reverse bias on gate-source junction and causes the depletion region to penentrate into the channel, reducing channel width. The effect of reduction in channel width provides more opposition to increase in drain current I_D. Thus rate of increase in I_D w.r.t V_{DS} is now reduced.

The voltage V_{DS} at which the current I_D reaches to its constant saturation level is called pinch-off voltage.

* The pinch off voltage $V_p = \frac{N_D}{2\epsilon} a^2$

$\epsilon \rightarrow$ Dielectric constant of channel material

$a \rightarrow$ Half the region of n-type material without channel width

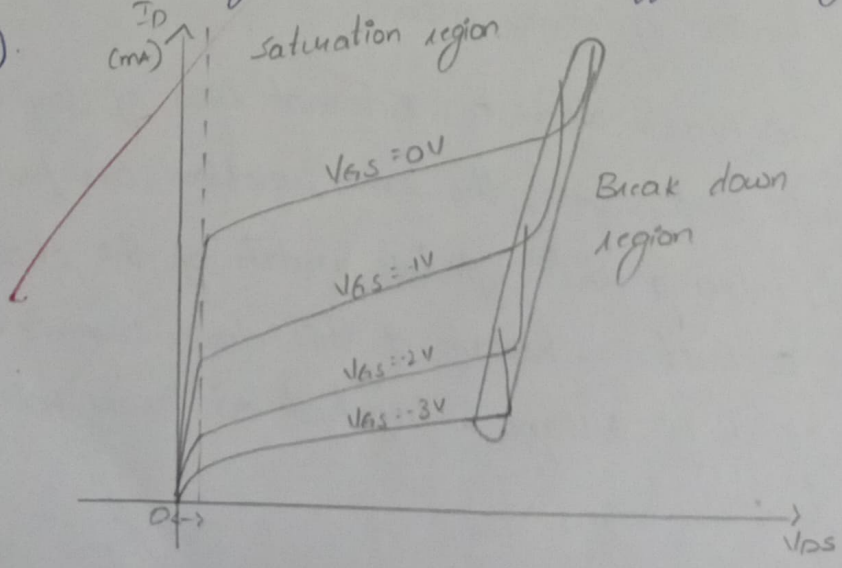
$N_D \rightarrow$ concentration of donor atoms.

(3) V_{GS} with -ve bias :- When an external bias of say V is applied b/w gate and source, the gate junction are further reverse biased, reducing the effective width of the channel available for conduction. Because of this drain current is reduced and pinch off voltage is reached at lower point on drain current then when $V_{GS}=0$.

(4) Break down region:- If we increase value of V_{DS} beyond Pinch-off voltage V_p, the drain current I_D remains constant upto certain value of V_{DS}. If we further Exceeds, V_{DS}. The voltage at with the gate channel junction breaks down, due to avalanche effect. The drain current increases very rapidly.

(5) Ohmic & Saturation region:- It is seen that the drain characteristics of JFET is divided into two regions ohmic region & saturation region. In ohmic region the drain current I_D varies with V_{DS} and the JFET is said to be voltage variable resistance. In the saturation region the drain current I_D remains fairly constant and does not vary with V_{DS}.

(6) cut-off :- For an n-channel JFET, the more -ve V_{GS} causes drain current to reduce and pinch off voltage to reach at a lower drain current. When V_{GS} is made sufficiently -ve, I_D is reduced to zero. This is caused by the widening of the depletion region to ∞ point where it completly closes the channel. The value of V_{GS} at the cut-off is designated as $V_{GS(off)}$.

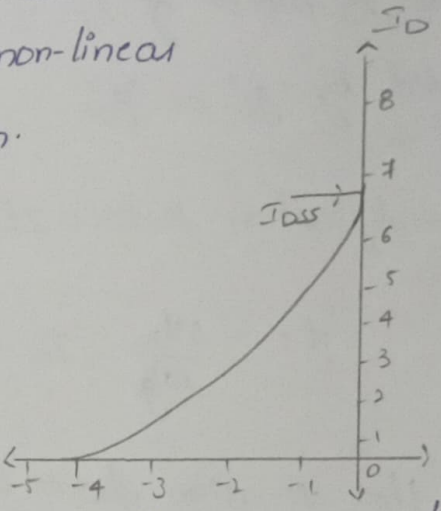


Transfer characteristics for N-channel JFET:-

It represents drain current I_D and gate to source voltage V_{GS} are known as transfer characteristics of JFET. The figure shows the transfer characteristics of n-channel JFET.

(1) The relationship between the drain current I_D and gate-source voltage V_{GS} is non-linear. This is defined by shockley's Equation.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$



(2) A point 'A' at the bottom end of the curve on the V_{GS} axis represents V_{GS} and point V_{GS} "B" at the top end of the curve on the I_D axis represents I_{DSS}. Thus this curve shows the operating point of a JFET.

$I_D = 0$ when $V_{GS} = V_{GS}(off)$

$I_D = I_{DSS}$ when $V_{GS} = 0$

3. (a) Define all JFET parameters

(1) Transconductance (g_m):- It is the change in the drain current for given change in gate-source voltage with the drain-source voltage constant. It is also called as mutual conductance.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}\Bigg|_{V_{DS}=\text{const}}$$

(2) Drain resistance (r_d) :- It is the reciprocal of the slope of the drain characteristics and is defined by

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ , } V_{GS} \text{ held constant}$$

→ The reciprocal of r_d is called the drain conductance. It is denoted by "g_d" or "g_{ds}".

(3) Amplification factor :- It is defined by

$$\mu = -\frac{\Delta V_{DS}}{\Delta V_{gs}} \text{ , } I_D \text{ held constant.}$$

Here, the -ve sign shows that when V_{gs} is increased, V_{DS} must be decreased for I_D to remain constant.

(b) Explain biasing methods of JFET

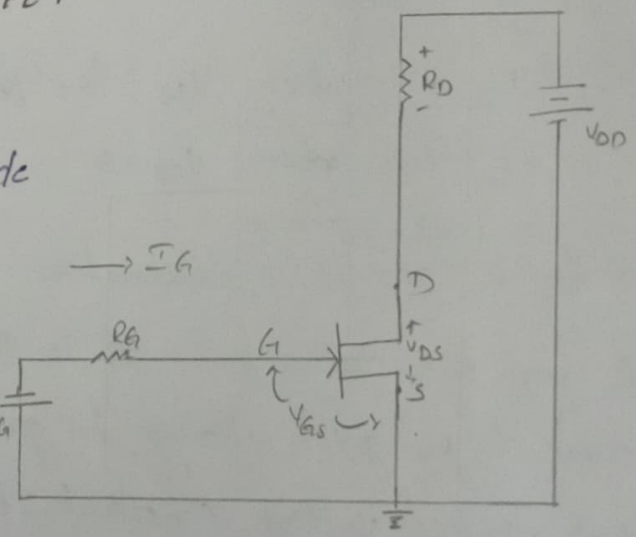
(1) Fixed bias :-

By applying KVL to input side

$\Rightarrow -V_{GG} - I_G R_G - V_{GS} = 0$

$-V_{GG} - V_{GS} = 0$

($\because I_G = 0$ because no majority charge carriers)



→ The main disadvantage in fixed bias is here we are using two external voltages.

(2) Source dcy bias :-

apply KVL to input side

$V_G = V_{GS} + V_S$

WKT

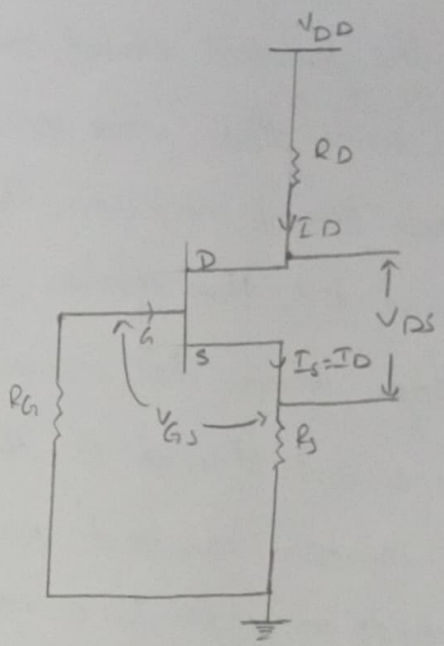
$V_{GS} = V_G - V_S$

$= V_G - I_S R_S \quad (\because V_S = I_S R_S)$

$= V_G - I_D R_S \quad (\because I_D = I_S)$

$V_{GS} = 0 - I_D R_S$

$\therefore V_{GS} = -I_D R_S$



(3) Voltage divider bias :-

Here R_1 & R_2 Provides biasing

$V_G = \frac{R_1}{R_1 + R_2} V_{DD} \quad -①$

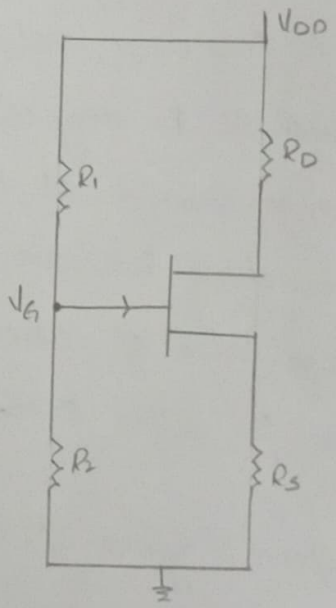
$V_S = I_D R_S$

$V_G = V_{GS} + V_S$

$V_{GS} = V_G - V_S$

$= V_G - I_S R_S$

$V_{GS} = V_G - I_D R_S \quad -③$

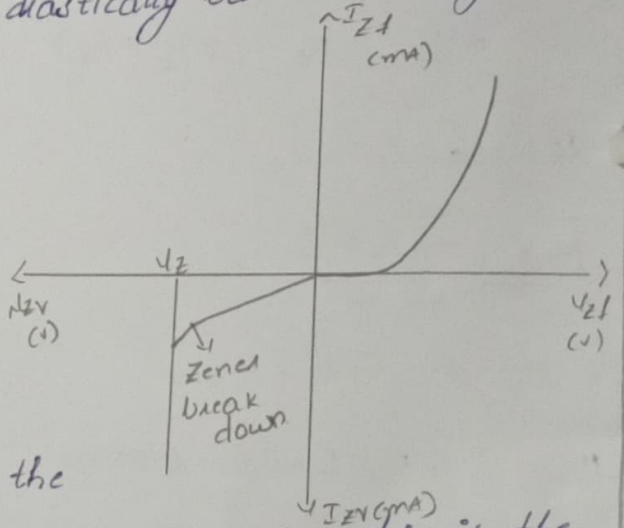


$\boxed{V_{GS} = \left(\frac{R_1}{R_1 + R_2}\right) V_{DD} - I_D R_S}$ ($\because$ by sub ① in ③)

$R_{TH} << R_S$

4. (a) Explain the characteristics of Zener Diode?

In the forward biased condition, the normal P-n diode and the zener diode work (or) operate in the same way. In the reverse biased condition, the zener diode carriers reverse saturation current till the reverse voltage applied is less than the reverse voltage when the reverse voltage Exceeds breakdown voltage, the current through it changes drastically but the voltage across it remains constant such a breakdown region is a normal operating region of a zener diode.



When the reverse voltage to a zener diode is increased, initially the current through it is very small, order of few μA. This is the reverse leakage current. At a certain reverse voltage current through zener diode increases rapidly. The change from a low value to large value of current is very sharp and well-defined. this voltage is called zener breakdown voltage (V_z).

(b) Explain different types of breakdown mechanisms?

Avalanche Breakdown :- The applied reverse bias causes a small reverse current I_o to flow in the current diode. This is due to movement of minority charge particles as the applied reverse bias voltage becomes larger, the minority carriers increasingly accelerate.

These are collisions between these carriers and e^-s involved in the covalent bonds of the crystal structure.

If the applied voltage is such that the travelling e^-s do not have high velocity, then the collisions take some energy away from them, alternating their velocity. If the applied voltage is increased, the velocity and hence the kinetic energy of e^-s increases. If such an e^- dashes against an e^- involved in covalent bond, then the collision gives bond valance e^- enough energy to enable it to break its covalent bond. Thus one e^- by collision creates an e^- hole pair. This phenomenon is known as carrier-multiplication.

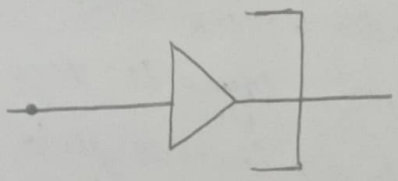
(2) Zener breakdown:- When a p-n junction is heavily doped the depletion region is very narrow. So under reverse bias condition, the electric field across the depletion layer is very intense, of the order 10^8 v/m or 10^6 v/cm. Such an intense field is enough to pull the e^-s out of the valance bonds of the stable atoms. These minority carriers constitute very large current and mechanism is called zener breakdown.

5. With neat sketch explain the working of tunnel diode along with its characteristics.

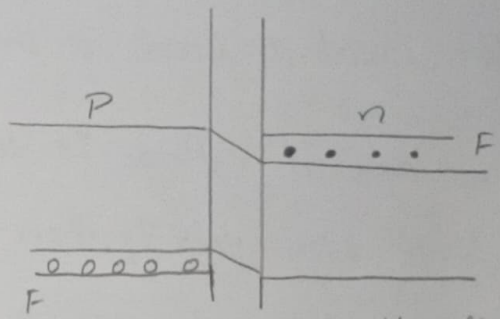
→ The other name for tunnel diode is Esaki diode.

→ Tunnel diode is a normal p-n junction but doping is 1000 times more.

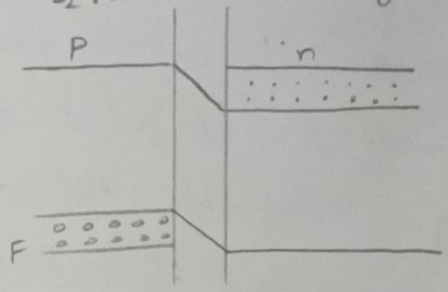
→ 100 times narrower
→ Negative resistances
→ They are used in oscillators
→ In high switching speed
→ It is a voltage control device
→ In unbiased condition the conduction band of n-type and valance band of p-type overlap
→ Fermilevel of p-type closer to valency band and Fermilevel of n-type closer to conduction band



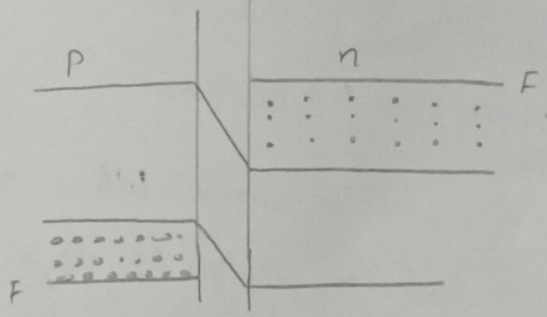
S_1 : unbiased condition



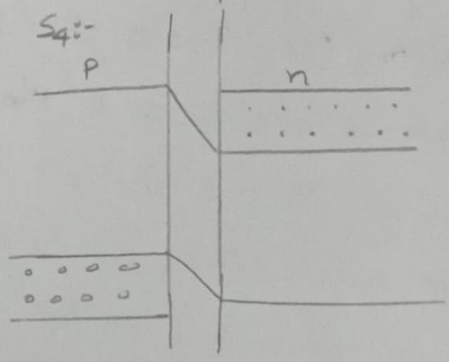
S_2 : when small voltage is applied



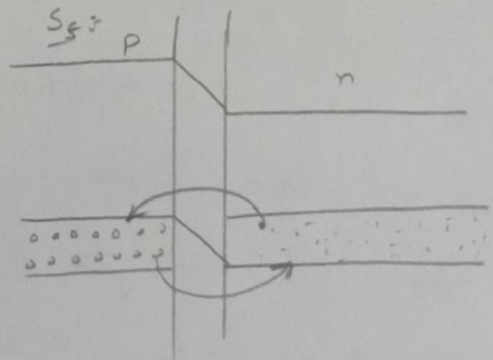
S_3 :



S_4 :-

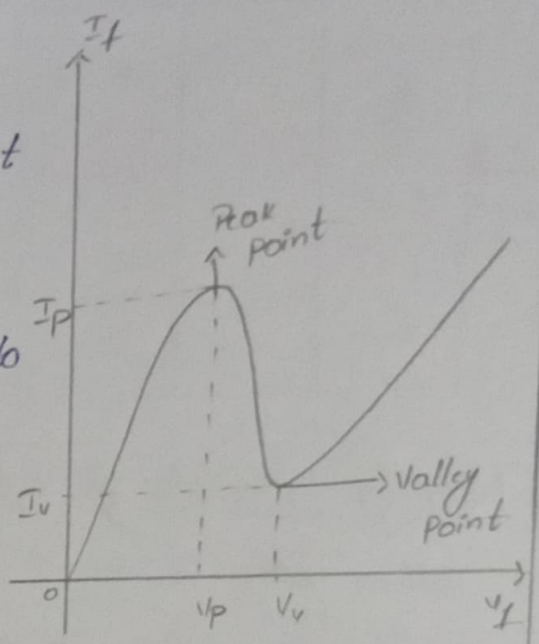


S_5 :



V-I characteristics of tunnel diode :-

The shape of the V-I characteristics curve of a tunnel diode is quite different from that of a normal diode.



When a reverse bias voltage is applied to a tunnel diode it conducts. It is an account of the heavy doping. The diode appears to be breakdown for any reverse voltage.

As soon as forward bias is applied the tunnel diode passes a considerable current which quickly reaches to its peak value I_p at a low value voltage V_p. As the applied voltage is increased the diode current starts decreasing and achives a maximum value I_v.

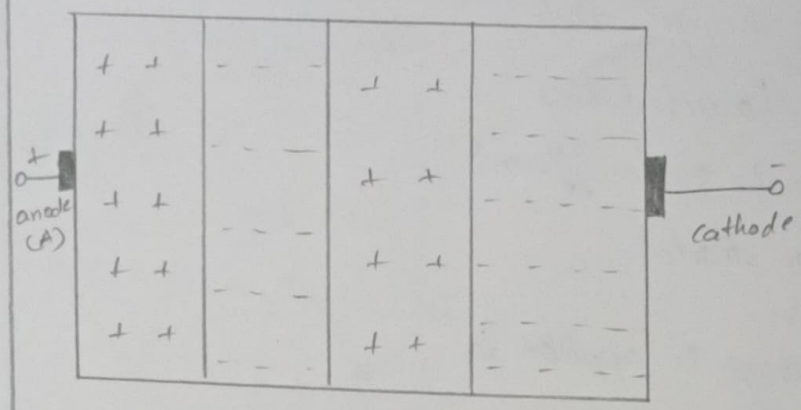
6. Explain the construction and working principle of Silicon Controlled rectifier.

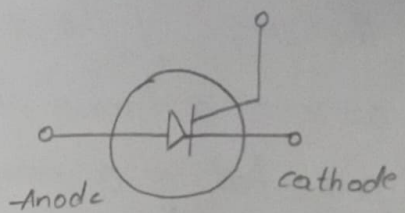
Construction :-

→ The SCR is a four layer P-n-P where P and n layers are alternately arranged. The outer layers are heavily doped and inner layers are lightly doped.

→ There are three P-n junctions called J_1, J_2, J_3

→ The outer P-layer is called anode while outer n layer is called cathode middle P-layer is called gate.





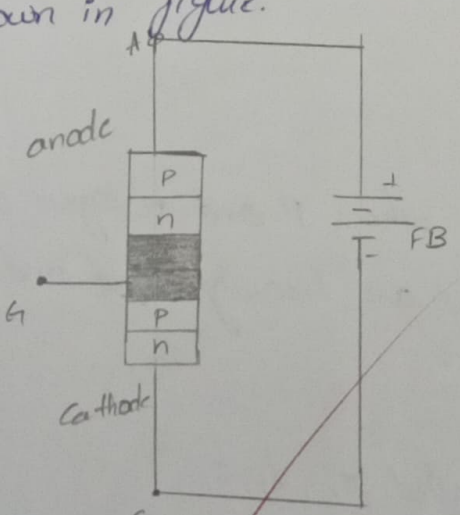
symbol of SCR

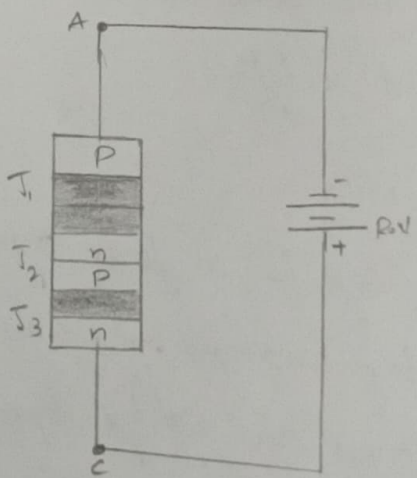
Working Principle of SCR:-

(1) When gate is open:-

→ The Junctions J_1 & J_3 are forward biased and Junction J_2 is reverse biased. There is depletion region around J_2 and only leakage current flows which is negligibly small.

→ Practically the SCR is said to be off and this is called forward blocking state of SCR voltage applied to anode & cathode with anode +ve is called forward voltage. This is shown in figure.





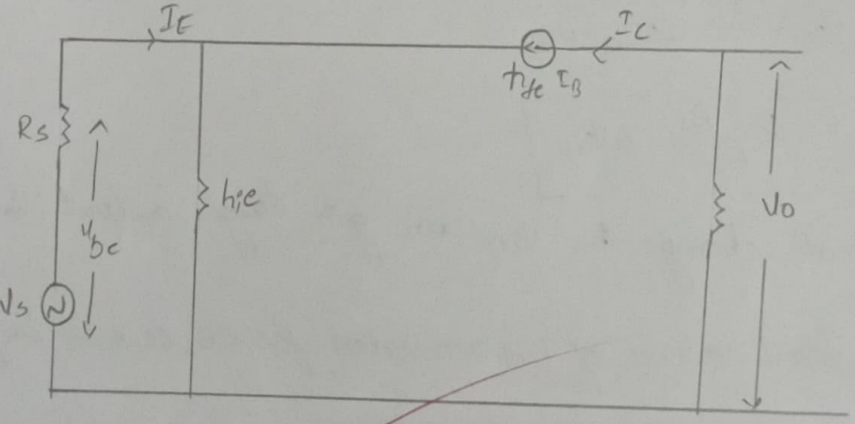
→ In forward blocking state, if the forward voltage is increased and made sufficiently large, the p-n junction J_2 breaks down and SCR conducts heavily.

CB	CE	CC
$h_{ib} = \frac{h_{ie}}{1+h_{fe}}$	$h_{ie} = \frac{h_{ib}}{1+h_{fb}}$	$h_{ic} = h_{ie}$
$h_{fb} = \frac{-h_{fe}}{1+h_{fe}}$	$h_{fe} = \frac{-h_{fb}}{1+h_{fb}}$	$h_{fc} = -(1+h_{fc})$
$h_{rb} = \frac{h_{ie}h_{oe}}{1+h_{fe}} - h_{re}$	$h_{re} = \frac{h_{ib}\cdot h_{ob}}{1+h_{fb}} - h_{rb}$	$h_{rc} = 1-h_{re}$
$h_{ob} = \frac{h_{oe}}{1+h_{fe}}$	$h_{oe} = \frac{h_{ob}}{1+h_{fb}}$	$h_{oc} = h_{oe}$

10 (b) Explain simplified hybrid model and derive the parameters for CB configuration.

If $h_{oe} R_L < 0.1$

If the above condition is satisfied we can use this in simplified hybrid model.



(1) current gain :- $A_I = \frac{I_L}{I_c} = \frac{-I_c}{I_c} = \frac{-h_{fc} I_B}{-(1+h_{fc}) I_b}$

$= \frac{h_{fc}}{1+h_{fc}}$

(2) Input Impedence :-

$Z_i = \frac{V_{be}}{I_c} = \frac{h_{ic}\cdot I_b}{-(1+h_{fc}) I_b} = \frac{h_{ic}}{1+h_{fc}}$

→ When input signal is applied to base current I_B varies sinusoidally

I_B max = 30 μA

I_B min = 10 μA

$\Delta I_B = 20\ \mu A$

Due to change in I_B the I_C also changes.

$$\Delta I_C = 4\ mA - 3mA = 2\ mA.$$

$$\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{2\ mA}{20\ \mu A} = 100$$

→ The current amplification is given by $\frac{\Delta I_C}{\Delta I_B} = 100$

→ Small change in input voltage

$$\Delta V_{in} = \Delta I_B \cdot R_B$$

$$V_{in} = V_{cc} - I_B R_B$$

→ Small change in output voltage

$$\frac{\Delta V_o}{\Delta V_{in}} = \frac{\beta \cdot \Delta I_B R_c}{\Delta I_B \cdot R_B}$$

$$\boxed{\Delta V_o = \frac{R - R_L}{R_B} \cdot \Delta V_{in}.}$$

Thus, for small change in V_{in} we get larger output V_o.

9. Give the typical values of h-parameters for CB, CC & CE configuration also give conversion formulae b/w them?

Parameter	CB	CE	CC
h_i	20 Ω	1 kΩ	1 kΩ
h_u	30×10^{-4}	2.5×10^{-4}	1
h_f	-0.98	50	-51
h_o	0.5 μU	25 μU	25 μU
$1/h_o$	2 UΩ	40 kΩ	40 kΩ

$h_{ie} = \frac{V_{be}}{i_b}\Big|_{V_{ce}}$ → Tangent line

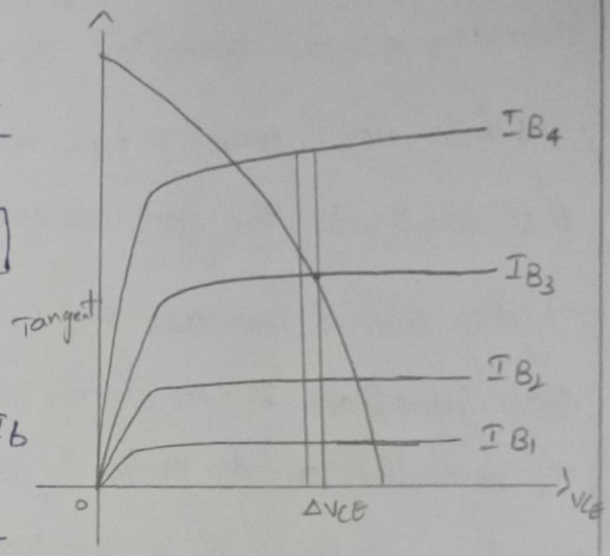
$h_{re} = \frac{V_{be}}{V_{ce}}\Big|_{i_b}$ → Horizontal line.

$h_{ie} = \frac{1.1}{(50-30)\times 10^{-6}}$

$\boxed{h_{ie} = 5K\Omega}$

$h_{re} = \frac{1-0.85}{4.2}$

$\boxed{h_{re} = 0.075}$



$h_{fe} = \frac{i_c}{i_b}\Big|_{V_{CE}}$ $\quad h_{oe} = \frac{i_c}{V_{CE}}\Big|_{I_b}$

$h_{fe} = \frac{(4.2-4.1)\times 10^{-3}}{4.9-3.6} = 76.9\mu\upsilon$

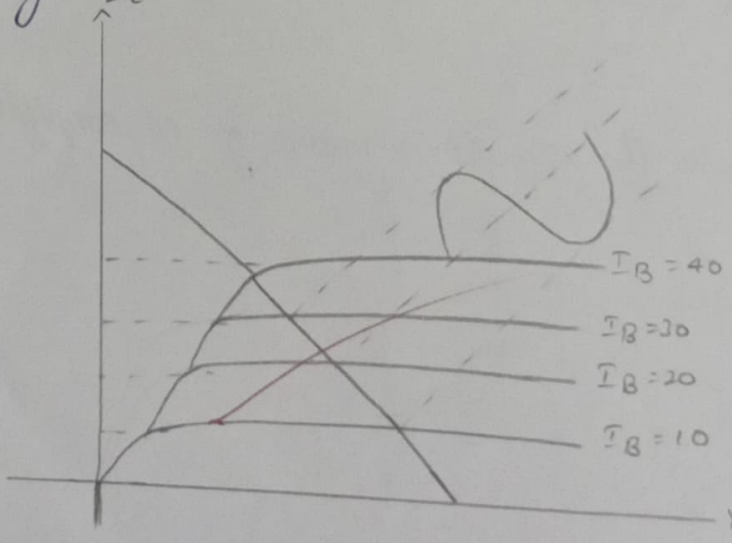
$\boxed{h_{oe} = 76.9\mu\upsilon}$

8. (a) Explain transistor amplifying action?

→ Amplifier is a device which increases the power level of the signal without changing frequency and shape of the signal.

→ Transistor is used as amplifier in active region.

→ Small changes in input voltage creates large change in output voltage.



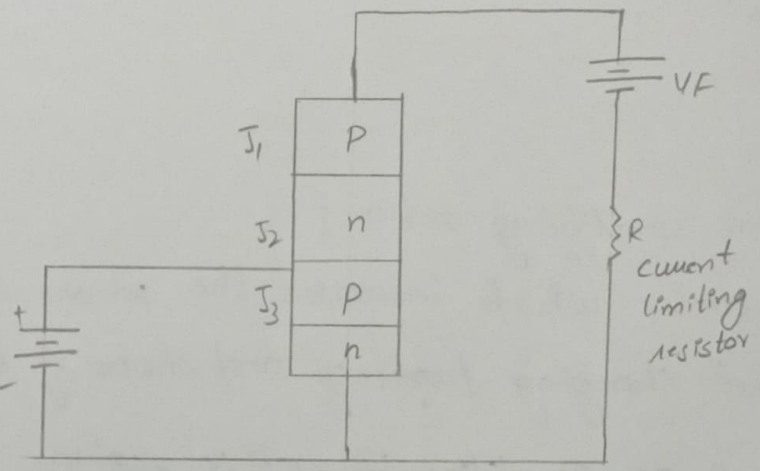
(2) When gate is closed :-

→ The electrons from n-type cathode which are majority in number, across junction J_3 to reach to +ve of battery.

→ While holes from p-type move towards the -ve of battery this constitutes the gate current.

→ This current increases the anode current as some of electrons cross junction J_2. As anode current increases more e^{-s} cross the J_3 and the anode current further increases.

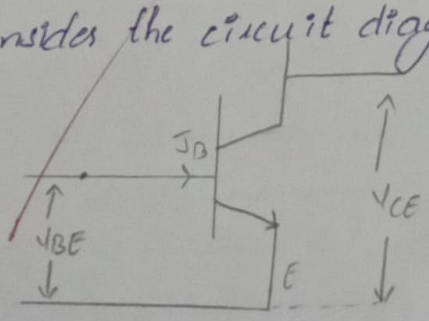
→ The resistance 'R' is required to limit the current.



→ Once SCR conducts gate looses its control.

7. Explain how to determine h-parameters from transistor characteristics.

→ Let us consider the circuit diagram of CE amplifier.



(3) Voltage gain (A_V):-

$$A_V = \frac{V_o}{V_i} = \frac{I_L R_L}{V_{be}} = \frac{I_L R_L}{I_c Z_i}$$

$$= A_I \cdot \frac{R_L}{Z_i} = \frac{h_{fe}}{1+h_{fe}} \cdot \frac{R_L}{\frac{h_{ic}}{1+h_{fe}}} = \frac{h_{fe}}{h_{ic}} = R_L$$

(4) Output admittance :-

$$Z_o = \frac{V_o}{I_L}\Big|_{V_s=0}$$

$Z_o = \infty$, $Z_o' = R_L$

$(\because Z_o \| R_L)$

Pavani

LIST OF WEAK STUDENTS

	Hall Ticket No.	Name	CGPA
1	20VEIA0412	K. Kaushik	
2	20VEIA0422	N. Muni Sai	
3	20VEIA0432	Police Patel Ravinder Reddy	
4	20VEIA0439	Rajnish Chaubey	
5	20VEIA0446	Ramavath Abhinay	
6	20VEIA0452	T. Swapna Reddy	
7	20VEIA0457	V. Naveen Reddy	
8	20VEIA0458	B. Kumar	
9	20VEIA0472	D. Akshay Yadav	
10	20VEIA0475	D. Mani Krishna Goud	
11	20VEIA0476	G. Veerababu	
12	20VEIA0482	K. Rajesh	
13	20VEIA0487	M. Sai Harshith	
14	20VEIA0488	M. Nithin	
15	20VEIA04A0	R. Bhargav Reddy	
16	20VEIA04A4	S. Chandra Shekar Reddy	
17	20VEIA04B5	C. Vamshidhar Reddy	
18			
19			
20			

ELECTRONIC DEVICES AND CIRCUITS II YEAR I SEM ECE



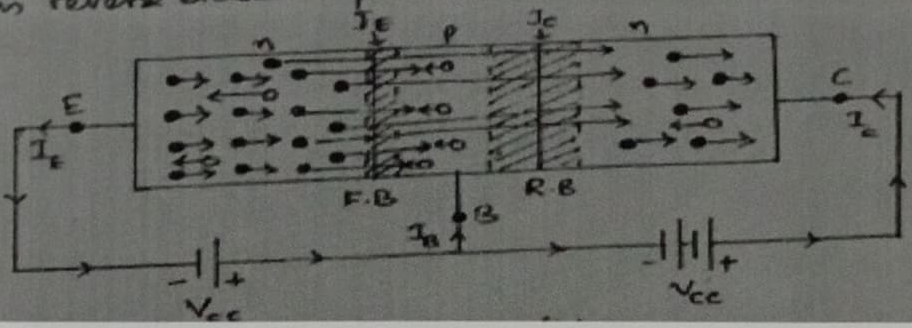
SCHEDULE FOR TUTORIAL/REMEDIAL CLASSES

Date	Period	No of students attended	Theory/test

Sl.No	MID -I Question paper	BTLs	COs	Marks
1a	With the neat sketch explain VI characteristics of pn junction diode.	2	1	2
1b	With a neat sketch explain working of npn transistor	2	2	2
1c	Classify FETs	4	3	1
2a	Define clipper and describe positive clipper	2	1	2
2b	Derive the relation between α, β and γ	2	2	2
2c	Differentiate between BJT and FET	2	3	1
3a	A HWR has a load of 3.5kΩ. If the diode resistance and secondary coil resistance together have a resistance of 800Ω and the input voltage has a signal voltage of peak value240V. Calculate i. peak average and rms value of current ii. dc power output iii. ac power input iv. efficiency of the rectifier.	3	1	2
3b	Draw the common base circuit and sketch the input characteristics and explain about early effect	2	2	2
3c	Explain the meaning of field effect in FET	2	3	1
4a	Define filter. Explain FWR with capacitor filter	2	1	2
4b	Explain how transistor works as a switch	2	2	2
4c	Define JFET parameters	1	3	1

1b. With a neat sketch explain working of npn transistor

Working of npn transistor:- The basic operation of the transistor will now be described using the npn transistor. The figure 3.5 shows a npn transistor with its emitter junction forward biased by a dc source V_{EE} and the collector junction reverse biased by another dc source V_{cc}.



Due to the forward bias between emitter and base the width of the depletion layer at the emitter junction is reduced i.e the electrons of n-region (Emitter) are repelled by the negative (terminal) potential of the external source and the potential barrier at this junction is reduced and hence electrons cross the junction and diffuse into p-region i.e base. This constitutes the emitter current I_E. The width of the base is very thin and is lightly doped. As these (emitted) electrons flow through the p-type base, they tends to combine with holes in base region. Only two to five percent of the emitted electrons will recombine with the holes of the p-type base region. This constitutes the base current I_B, which is, of course, is very small. The remaining large number of electrons (95% to 98%) are able to drift across the base and enter the collector region And then electrons are sweep by the positive potential of external source V_{cc}. This constitutes collector current I_c.

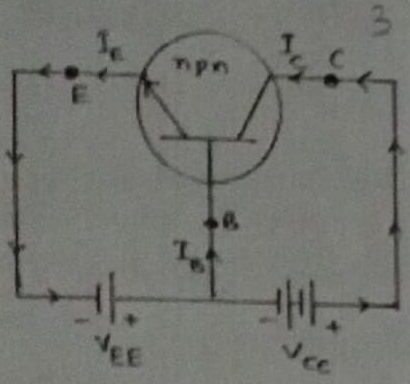
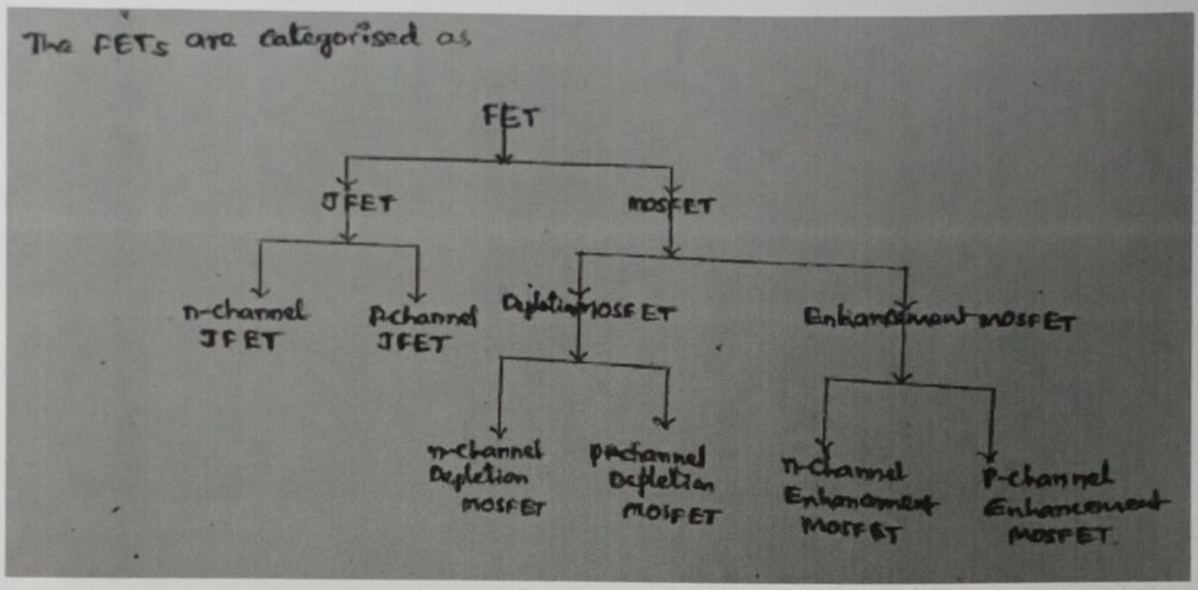


Figure: 3.5(B)

For every electron flowing out and entering the positive terminal of the source V_{cc}, an electron from the negative terminal of the source V_{EE} enters the emitter region. These new electrons then move immediately toward the emitter junction and the process is thus repeated. In this way electrons conduction take place continuously as long as the two p-n junctions are properly biased. Thus the current conduction in an npn transistor is predominently by electrons.

1c. Classify FETs



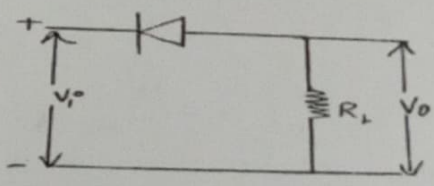
2a. Define clipper and describe positive clipper

7) Clipper circuits

The circuits which are used to clip off unwanted portion of the waveform, without distorting the remaining part of the waveform are called clipper circuits or clippers

When the diode is connected in series with the load, such circuit is called series clipper. When the diode is connected in a branch which is parallel to the load, it is called Parallel clipper

i) Series Positive clipper circuit

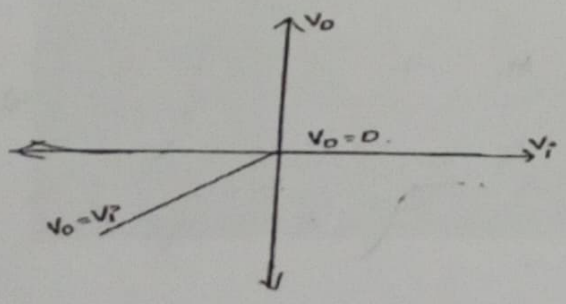


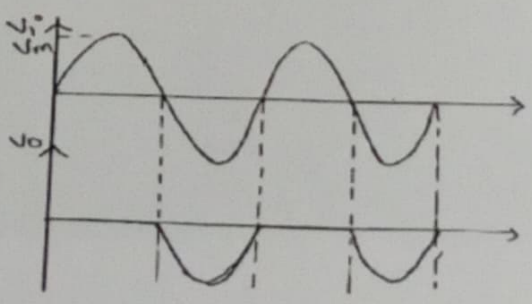
Case-1 : considering the diode is ideal

$V_N = V_i$, $V_P = 0$

i) $V_P > V_N$, $V_i < 0$, $V_o = V_i$ → Diode - ON

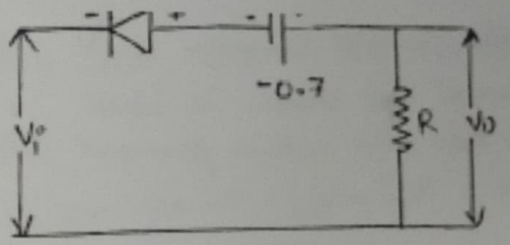
ii) $V_P < V_N$, $V_i > 0$, $V_o = 0$ → Diode - OFF





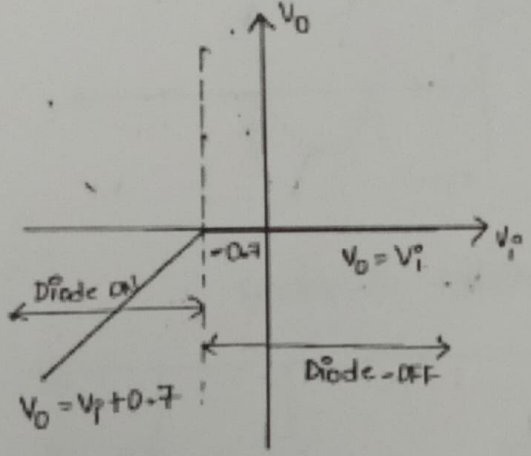
(34) Case-II : Considering V_γ

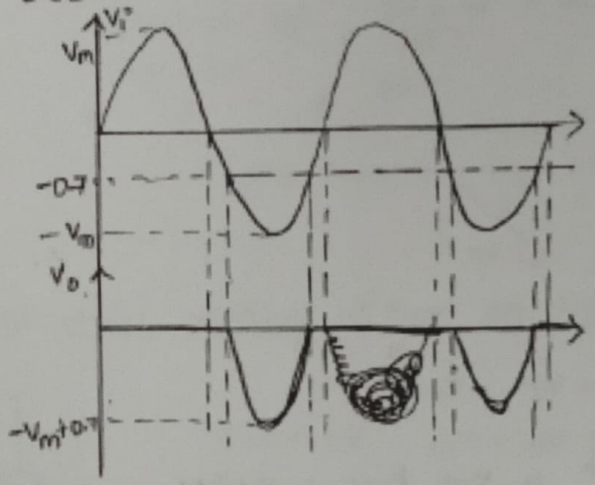
Effect of V_γ on positive clipper circuit $V_N = V_i^\circ$, $V_P = -0.7$



i) $V_P > V_N$, $V_i^\circ < -0.7$, $V_o = V_i^\circ + 0.7$ - Diode ON

ii) $V_P < V_N$, $V_i^\circ > -0.7$, $V_o = 0$ - Diode OFF



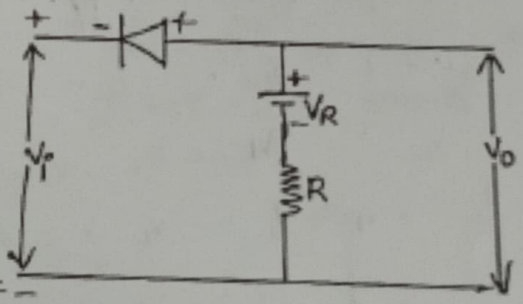


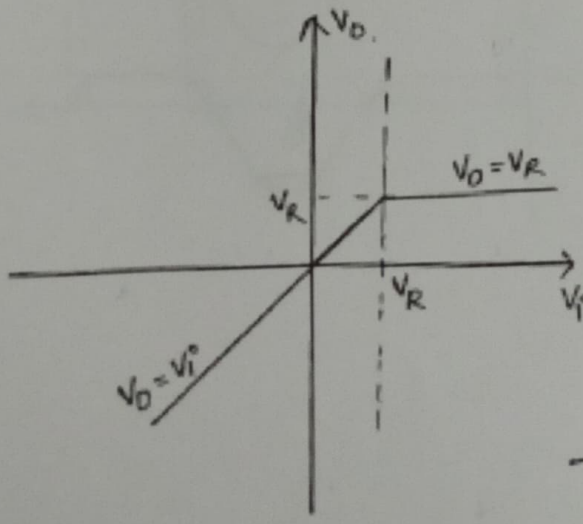
Case-III : clipping above V_R

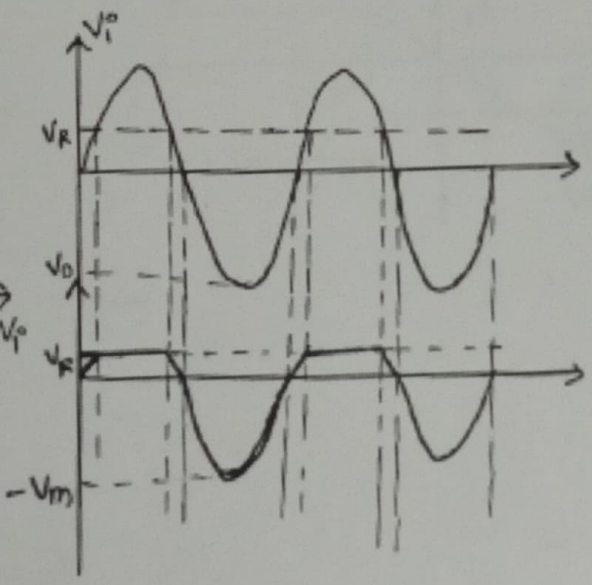
$V_N = V_P$, $V_P = V_R$

i) $V_P > V_N$, $V_i^\circ < V_R$, $V_o = V_i^\circ$ - Diode ON

ii) $V_P < V_N$, $V_i^\circ > V_R$, $V_o = V_R$ - Diode OFF







1) Basic parallel clipper with positive clipping

Assume the diode is ideal

acts as S.C when forward biased

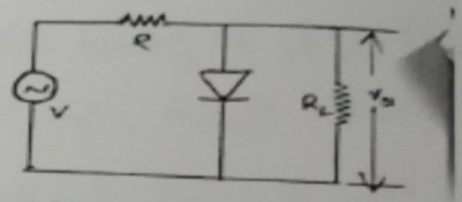
case-1 : $V_P > V_N$, $V_i > 0$ Diode-ON

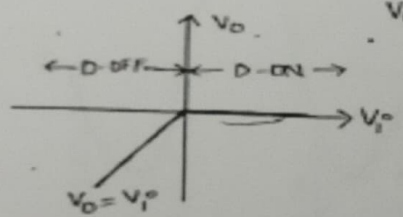
$V_O = 0$

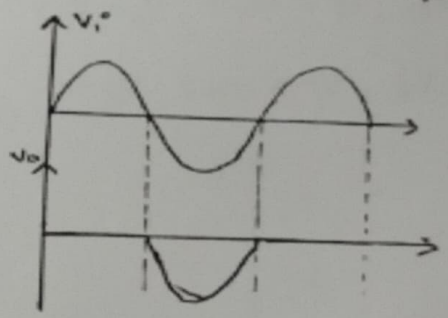
case-II : $V_P < V_N$, $V_i < 0$ Diode off

$V_O = \frac{V_i \times R_L}{R}$ iff $R << R_L$

$V_O = V_i$







2) Effect of cut-in voltage with positive clipping

$V_P = V_i$, $V_N = 0.7$

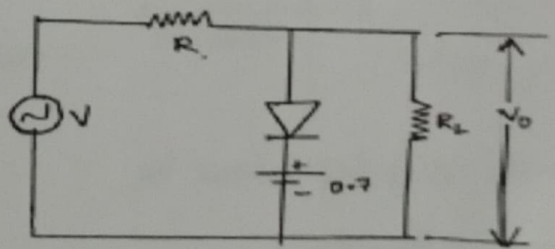
case-1 : $V_P > V_N$, $V_i > 0.7$

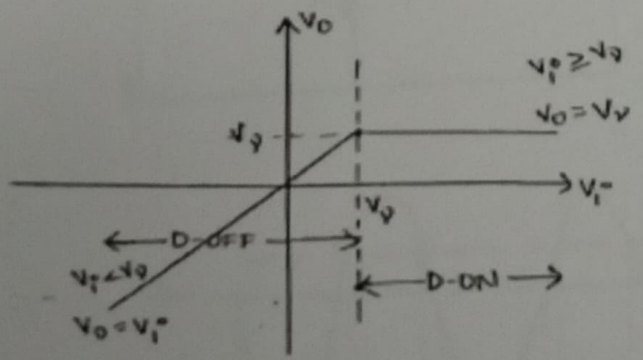
D-ON , $V_O = 0.7$

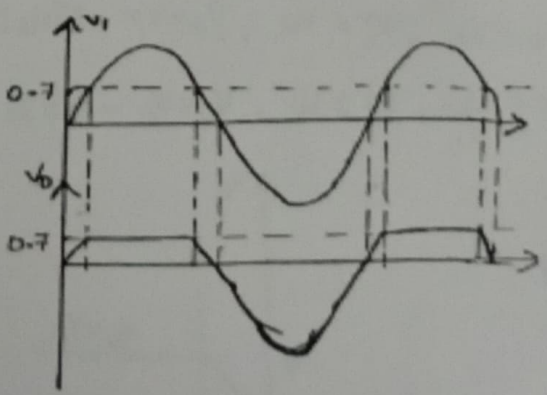
Case-II : $V_P < V_N$, $V_i < 0.7$

D-OFF $V_O = V_i \times \frac{R_L}{R}$

$R << R_L$ $V_O = V_i$







2c. Differentiate between BJT and FET

COMPARISON OF TRANSISTORS

Comparison of BJT and FET

S.no	Parameter	BJT	JFET
1	Device type	Bipolar	Unipolar
2	Control element	Current controlled device	voltage controlled device
3	Types	n-p-n & p-n-p	n-channel & p-channel
4	configurations	CB, CE, CC	CS, CG, CD
5	Input resistance	less compared to JFET	High compared to BJT
6	Size	Bigger than JFET	Smaller in Construction
7	Sensitivity	Higher sensitivity to changes in the applied signals	Less sensitivity to changes in the applied voltage.
8	Thermal runaway	Exists in BJT	Does not exists in JFET
9	Gain factor	$\beta = \frac{\Delta I_C}{\Delta I_B}$	$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$
10	Gain bandwidth Product	High	Low.

3b. Draw the common base circuit and sketch the input characteristics and explain about early effect

3.7.2.1) V-I characteristics of CB configuration :-

Figure 3.15 shows the circuit arrangements to determine the V-I characteristics of a pnp transistor connected in common base configuration. Here a pnp transistor is connected in C-B configuration with the help of variable d.c sources V_{EE} and V_{CC}. Millimeters are connected in series with Emitter and collector to measure the I_E and I_C respectively. Similarly voltmeters are connected in parallel across E and B to measure the voltages V_{BE} and across C and B to measure V_{CB} respectively. The electrical behaviour of a common base transistor can be described by stating the relationship between different voltages and respective currents. This relationship can be plotted graphically and the curves thus obtained are known as V-I characteristics. Here we shall consider the input and output characteristics.

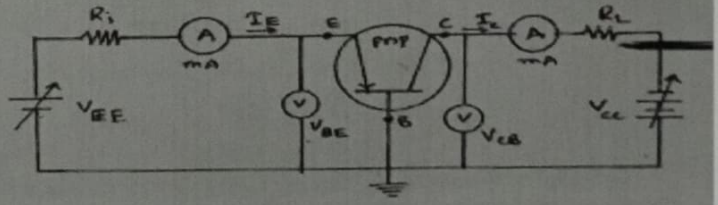
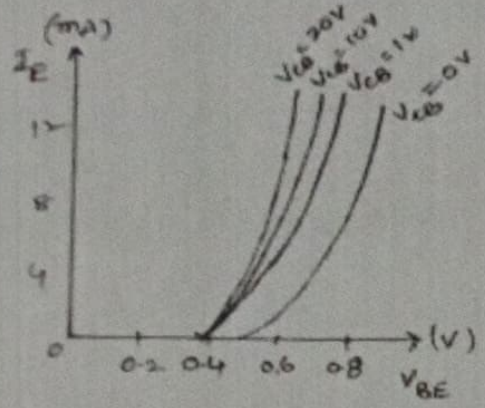


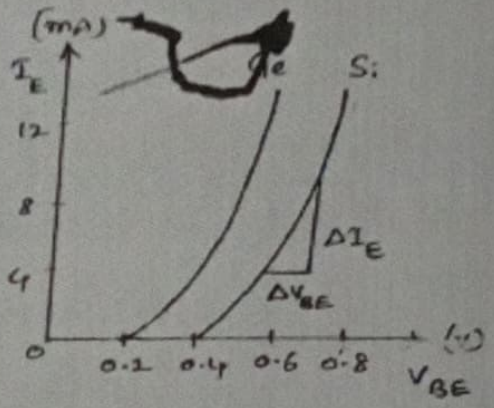
Figure: 3.15

3.7.2.2 Input characteristics :- The curves showing the variation of the (I_E) emitter current with emitter-base voltage V_{EB} at constant collector voltage V_{CB}, are called the input characteristics of the C.B Transistor.

For plotting the input characteristics, the collector-base voltage V_{CB} is kept fixed. The cct emitter-base voltage V_{BE} is varied with the help of variable d.c source V_{EE} and the emitter current I_E is noted for each value of V_{BBE}. The procedure is then repeated for other fixed values of V_{CB}. Then curves are plotted between V_{BE} and I_E, as shown in Fig 3.16.

It may be seen that these curves are exactly similar to the forward characteristics of a p-n diode.





A study of these curves reveals the following facts :

(i) There exists a cut-in or threshold voltage of V_{BE} below which the I_E is very small.

(ii) The I_E increases rapidly with increasing value of V_{BE}. This shows that the input resistance R_{in} is very small

$$\text{i.e } R_{in} = \left.\frac{\Delta V_{BE}}{\Delta I_E}\right|_{V_{CB}=\text{constant}}$$

The Figure 3.17 shows the input characteristics of Si and Ge. These characteristics are hardly affected by changes either in V_{CB} or in temperature

Early effect (Base-width modulation):- In the C-B configuration, as the collector voltage V_{cc} is made to increase the reverse bias, the space charge (depletion region) width between the collector and base tends to increase, with the result that the effective width of the base decreased. This dependency of base-width on collector-to-base voltage V_{CB} is known as the base-width modulation or Early effect. This decrease in the base width has three consequences:

(i) There is less chance for recombination with in the base region. Hence α increases with V_{CB}.

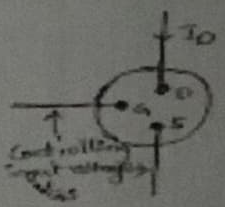
(ii) the charge gradient is increased with in the base, and consequently, the current of minority carriers injected across the emitter junction increases.

(iii) for extremely large voltages, the effective base-width may be reduced to zero, causing voltage breakdown in the transistor. this phenomenon is called the punch through effect.

3c. Explain the meaning of field effect in FET

* Field Effect Transistor (FET) :-

The field effect transistor abbreviated as FET is another semiconductor device like a BJT. Like BJT, FET is also a three terminal device, however, the principle of operation of FET is completely different from that of BJT. The three terminals of FET are named as Drain(D), Source (S) and gate (G) out of these three terminals gate acts as a controlling terminal.



→ Voltage Controlled device

The voltage applied between gate and source V_{GS} controls the drain current I_D. Therefore, FET is a voltage controlled device. The name field effect is derived from the fact that the output current flow is controlled by an electric field setup in the device by an externally applied voltage.

→ Unipolar device

In FET, current is carried by only one type of charge particles, either electrons or holes. Hence FET is called Unipolar device.

→ Other important features

- FET is more temperature stable as compared to the BJT.
- FET has very high input impedance. FETs are preferred in amplifiers where high input impedance is required.
- FETs require less space than that for BJTs, hence they are preferred in

4a. Define filter. Explain FWR with capacitor filter.

8.4 Filters -

It is seen that the output of various rectifiers is not a pure d.c. but contains a.c harmonics (ripples). To remove or minimize the ripples in the output of the rectifier, filters are used. "A circuit that converts a pulsating output of a rectifier into a very steady dc is known as filter", because it filters out or smoothens out the pulsations in the output.

A filter minimize ripples either by-passing or blocking the a.c components and provides a regulated and constant dc output. We will consider the following popular filter circuits.

(1) Series Inductor filter
(2) Shunt capacitor filter
(3) L- section or LC filter
(4) π - section, or CLC filter

2.4.2 Shunt Capacitor filter :-

To achieve the filtering action, a suitable capacitor (reactance $X_c = \frac{1}{\omega C}$) is connected across the rectifier and in parallel with the load R_L. This type of filter is known as "shunt capacitor filter". The action of the filter depends upon the fact that the capacitor stores energy during the conduction period (i.e charging) and delivers this energy to the load (into the circuit) during the non-conduction period (discharges).

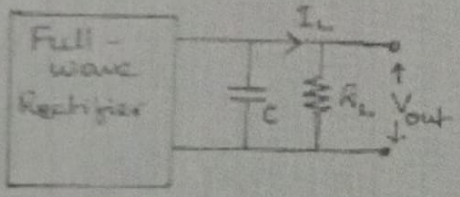


Fig: 2.9(A)

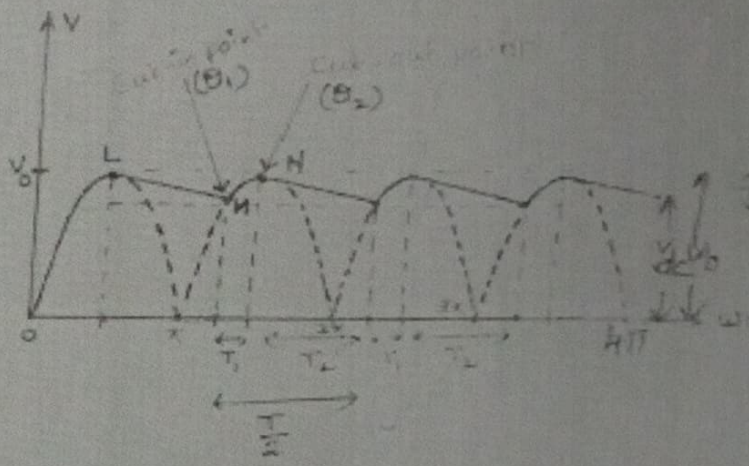
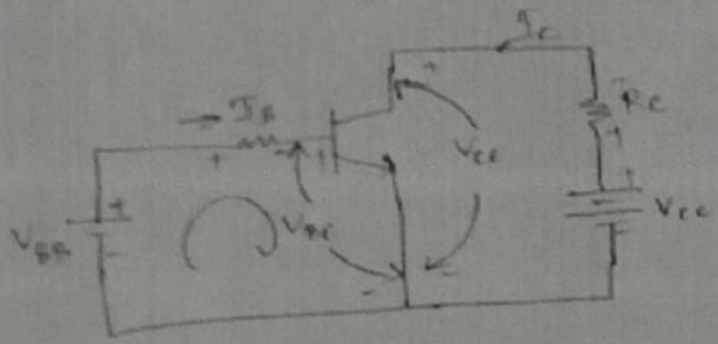


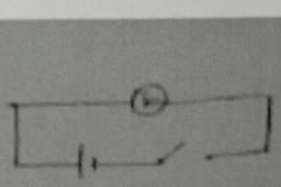
Figure: 2.9(B)

When the output voltage of the rectifier increases, the capacitor charges up almost equal to the peak value of the rectifier output i.e at the end of the first quarter cycle (L) and stores energy in its electric field. During the subsequent half-cycle, when the output of the rectifier drops to zero and then rises again the capacitor discharges exponentially through the load (i.e delivers its stored energy) and maintains a voltage across it at a higher value. In comparision with the case of the rectifier without filter (i.e. no capacitor C) it is represented by the line curve LM. At point M the capacitor begins to recharge to the peak (i.e to the point N) and then discharges again. This cycle is repeated again and again. The variations (ripples) being much less than in the rectifier output. The extent of these variations depends on the time constant 'RC' of the capacitor and load. If the time constant RC is large in comparision with the time period of the applied a.c, then the capacitor discharges slowly

4b. Explain how transistor works as a switch

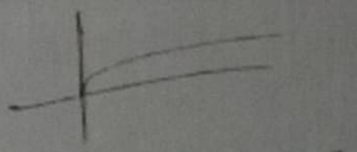
Transistor as switch





I

I



R = 5Ω

30V

I = 30/5

Apply KVL at i/p

$+V_{BB} - I_B R_B - V_{BE} = 0$

$V_{BB} = I_B R_B + V_{BE}$

$V_{BE} = V_{BB} - I_B R_B$

V_i

Apply KVL at o/p

o/p

$V_{CC} - I_C R_C - V_{CE} = 0$

$V_{CC} = V_{CE} + I_C R_C$

$V_{CE} = V_{CC} - I_C R_C$

$V_o = V_{CC} - I_C R_C$

When

$V_i < V_t$

$I_B = 0$

$I_C = 0$

$V_o = V_{CC}$

↓

off state

(current is 0)

when

$V_i > V_t$

$I_B \uparrow$

$I_C \uparrow$

$V_o = V_{CC} - I_C R_C$

$V_o = 0$

↓

on state

(current is max)

transistor's

4c. Define JFET parameters

JFET Parameters:

The important parameters of JFET are as follows:

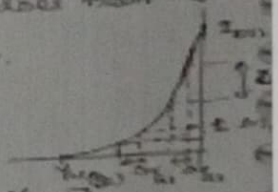
① Transconductance (g_m) ② Input resistance (R_{in})

③ Drain to source resistance (r_d) ④ Amplification factor (μ)

① **Transconductance (g_m):** — It is the change in the drain current to given change in gate-source voltage with the drain-source voltage constant. It is also called as mutual conductance

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}\Big|_{V_{DS}\ \text{const}}$$

From the transfer characteristics, we can say that it is the slope of the transfer characteristics. Since the slope varies, g_m also varies. g_m has a greater value near the top of the curve than it does near the bottom. The practical unit for g_m is millisiemen (mS) or mA/V.



we know that $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$.

Differentiating this eqn w.r.t V_{GS} we get,

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = I_{DSS} \cdot 2\left[1 - \frac{V_{GS}}{V_P}\right] \cdot \frac{-1}{V_P} = -\frac{2I_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right]$$

$$\boxed{g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right)} \quad \text{or} \quad \boxed{g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_{GS(OFF)}}\right]}$$

where $g_{mo} = -\frac{2I_{DSS}}{V_P}$

By using above eqn we can calculate an approximate value for g_m at any point on the transfer characteristics curve

② **Input resistance:** JFET operates with the gate-source junction reverse-biased. Therefore the input resistance at the gate is very high. The input resistance can be determined using the following eqn, where the vertical lines indicates an absolute value

$$R_{in} = \left|\frac{V_{GS}}{I_{GSS}}\right|$$

I_{GSS} — Reverse gate current. V_{GS} — Gate to source voltage.

③ **Drain to source resistance (r_d):** — From the drain characteristics Drain resistance r_d can be calculated. The drain resistance is the a.c resistance between drain and source terminals when the JFET is operating in the saturation region. It is the reciprocal of the slope of the drain-characteristic in the saturation region.

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\Big|_{V_{GS}\ \text{constant}}$$

④ **Amplification factor (μ):** It is defined as the ratio between drain source voltage to the gate-source voltage

$$\text{Amplification factor } \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}\Big|_{I_D\ \text{const}}$$

$$\therefore \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D} \cdot \frac{\Delta I_D}{\Delta V_{GS}} = r_d \cdot g_m$$

$$\boxed{\mu = r_d\, g_m}$$

College Code : VE

BOOKLET NUMBER : 25252

SREYAS

INSTITUTE OF ENGINEERING AND TECHNOLOGY

Nagole, Hyderabad - 500 068.

MID TERM EXAMINATION ANSWER BOOKLET

Course : B.Tech / M.Tech

Branch : ECE, Section A,

Year : II, Semester : I, Mid Term Examination : I, Month & Year : 12/21.

Hall Ticket No : 2 0 V E 1 A 0 4 1 4

Name of the Student : K. shivanandh

Signature of the Student with date : shivanandh

Name of the Subject : Electronic Devices and circuits

Date of the Exam : 15/12/21

Signature of the Invigilator with date : 15/12/21

MARKS AWARDED FOR QUESTIONS

Q. No.	*		Marks Awarded	Sub Total
1.		a		
		b		
		c		
2.		a		
		b		
		c		
3.	✓	a	2	5
	✓	b	2	
	✓	c	1	
4.	✓	a	2	5
	✓	b	2	
	✓	c	1	
			Total	10

* Student must indicate ✔ mark against the attempted question

Marks	Maximum	Awarded
Subjective	10	10
Objective	10	8
Assignment	05	5
Total	**25**	23

Signature of the Evaluator with date : Parani 16/12/21

INSTRUCTIONS TO THE CANDIDATES :

1. Students must be present in the examination hall 15 minutes before the commencement of the examination.
2. Write H.T. No. Name etc., correct & legible and must be signed on the main answer book and attendance sheet.
3. Student must adhere to all instructions given by an Invigilator prior to, during and immediately after an examination.
4. Students are required to ensure submission of answer scripts at the end of the examination, failure to submission of answer script would be treated as absent.

START WRITING FROM HERE

3a) Diode capacitance:- There are two types of diode capacitance.

1) Transition capacitance
2) Diffusion capacitance

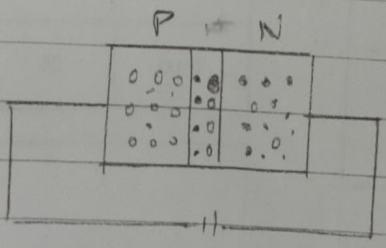
Transition capacitance:- Transition capacitance will be occur in reverse bias condition.

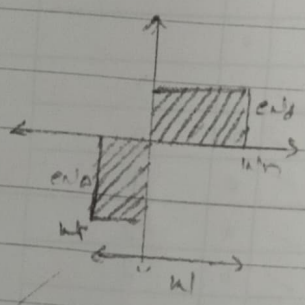
Transition capacitance is defined as, the ratio of change in immobile ions in depletion region to the change in reverse voltage

$$C_T \frac{dQ}{dv} = \frac{\epsilon A}{W} \text{ (mathematically)}$$

To get mathematical equation we consider a step graded junction in which concentration of acceptor atoms and donor atoms are different

$N_A >> N_d \qquad W_p >> W_N$





According to poisson's ratio.

$$\frac{d^2V}{dx^2} = \frac{N_A q}{\epsilon}$$

integrating above equation twice

$$\int \frac{d^2V}{dx^2} dx = \int \frac{N_A q}{\epsilon} dx$$

$$\frac{dv}{dx} = \frac{N_A q}{\epsilon} x$$

$$\int \frac{dv}{dx} dx = \int \frac{N_A q}{\epsilon} x \, dx$$

$$V = \frac{N_A q}{2\epsilon} x^2$$

Now, $V = V_B$ and $x = w$ from diagram

$$V_B = \frac{N_A q}{2\epsilon} w^2$$

$$w^2 = \frac{V_B 2\epsilon}{N_A q}$$

diff w.r.to V_B

$$\frac{dw^2}{dv} = \frac{d}{dv} \frac{V_B 2\epsilon}{N_A q}$$

$$2w \frac{dw}{dv} = \frac{2\epsilon}{N_A q}$$

$$\frac{dw}{dv} = \frac{\epsilon}{N_A q w} \rightarrow (1)$$

charge density $Q = N_A (\text{volume}) \times q$

$$Q = N_A q A$$

$$Q = N_A q w A$$

diff w.r.to v

$$\frac{dQ}{dv} = A N_A q \frac{dw}{dv} \rightarrow (2)$$

$$\frac{dQ}{dV} = \frac{AN\cancel{A}\cancel{q}\epsilon}{N\cancel{A}\cancel{q}Nl}$$

$$\boxed{\frac{dQ}{dV} = \frac{A\epsilon}{Nl}}$$

A = Area of cross section of potential barrier

l = width of potential barrier

ϵ = permitivity = $\epsilon_0 \epsilon_r$

Diffusion capacitance:- It occurs in forward bias, The change in amount of inject ions to applied voltage is called diffusion capacitance.

$$C_D = \frac{dQ}{dV} = \frac{I_F T}{\eta V_T}$$

W.K.T $C_D = dQ/dV$

There will be current in the p.n. junction

$$I = \frac{Q}{T}$$

T = life time of charge carriers

W.K.T diode equation = $I = I_0(e^{V/\eta V_T} - 1)$

$$I = I_0 e^{V/\eta V_T} - I_0$$

$$I + I_0 = I_0 e^{V/\eta V_T}$$

$$TI = Q$$

$$Q = T(I_0 e^{V/\eta V_T} - I_0)$$

$$Q = TI_0 e^{V/\eta V_T} - TI_0$$

diff w.r.to V

$$\frac{dQ}{dV} = \frac{dTI_0 e^{V/\eta V_T}}{dV} - \frac{d}{dV} TI_0$$

$$\frac{dQ}{dv} = \gamma I_0 \frac{d e^{v/\eta T}}{dv} - 0$$

$$\frac{dQ}{dv} = \gamma I_0 \frac{e^{v/\eta T}}{\eta T}$$

$$\frac{dQ}{dv} = \frac{\gamma (I + I_0)}{\eta T} \qquad (I >>>> I_0)$$

$$\boxed{\frac{dQ}{dv} = \frac{\gamma I_0}{\eta T}}$$

3b) Given $I_B = 100\mu A$ and $I_C = 2mA$

W.K.T $\alpha = \frac{I_C}{I_E}$, $\beta = \frac{I_C}{I_B}$, $\gamma = \frac{I_E}{I_B}$

i) $\beta = \frac{I_C}{I_B} = \frac{2 \times 10^{-3} A}{100 \times 10^{-6} A} = \frac{10^{-3} \times 10^{6}}{50} = 20$

ii) $\alpha = \frac{1+\beta}{1-\beta} = \frac{\beta}{1+\beta} = \frac{20}{1+20} = \frac{20}{21} = 0.9523$

iii) $\beta / \gamma \Rightarrow \gamma = \beta / \alpha = \frac{20}{20} \times 21 = 21$

$\gamma = \frac{I_E}{I_B} \Rightarrow I_E = \gamma I_B$

$I_E = 21 \times 100 \times 10^{-6} A$

$I_E = 0.0021 A$

$I_E = 2.1 mA$

iv) Given $\Delta I_B = (100\mu + 25\mu) A$, $\Delta I_C = (2mA + 0.6mA)$

$\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{(100 + 25) 10^{-6}}{[2 + 0.6) \times 10^{-3}} = \frac{125}{2.6} \times 10$

$$= \frac{(2406)10^{-3}}{(100+25)10^{6}} = \frac{2.6}{125} \times 10^{3}$$

$$= 0.0208 \times 10^{3}$$

$$\boxed{\beta = 20.8}$$

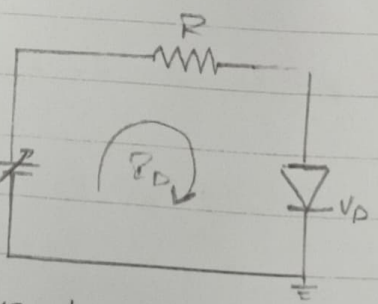
c) FET :- FET is called field effect transistor because the output current depends on generating electric field in input voltage

I_D depends on V_{GS}.

d) Load line analysis :-

The point of intersection of load line and characteristics curve of a diode is called 'Q' point of diode. 'Q' point is the point at which efficiency of working of diode is maximum

consider a equivalent diode circuit



Let current flowing through diode is I_D

and voltage across diode is V_D

Now apply K.V.L to above loop

$$V_S - I_D R - V_D = 0$$

$$V_S = I_D R + V_D$$

characteristic curve of diode is drawn blw voltage across diode and current through diode

we have to get the points on the graph to draw load line

So, By making $V = 0$, we get I

By making $I = 0$, we get V

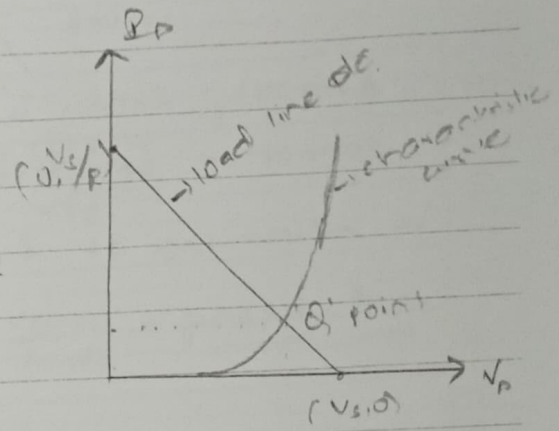
case-1:- If $V_D = 0$

$$V_S = I_D R + V_D$$

$$V_S = I_D R + 0$$

$$I_D = V_S / R$$

$V_D = 0$, $I_D = V_S / R$



case-2:- If $I_D = 0$

$$V_S = I_D R + V_D$$

$$V_S = (0) R + V_D$$

$$V_D = V_S$$

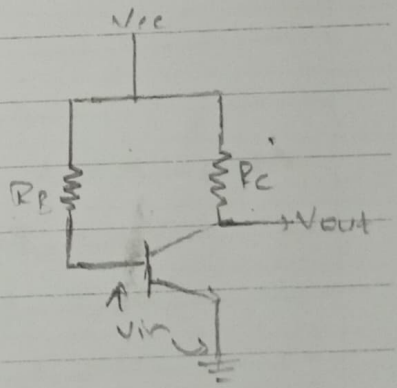
(b) Fixed bias:-

Apply KVL to loop

$$V_{CC} = I_B R_B + I_C R_C + V_{BE}$$

$$V_{CC} = I_C R_C + V_{BE}$$

$$I_C = \frac{V_{CC} - V_{BE}}{R_C}$$



$V_{BE} \ll V_{CC}$ (due to cut in voltage)

$$I_C = \frac{V_{CC}}{R_C}$$

w.r.t stability factor $S = \frac{1+\beta}{1-\beta\left(\frac{dI_B}{dI_D}\right)}$

$$S \approx \frac{1+\beta}{1-\beta \frac{d\frac{V_{cc}}{R_C}}{dR_B}}$$

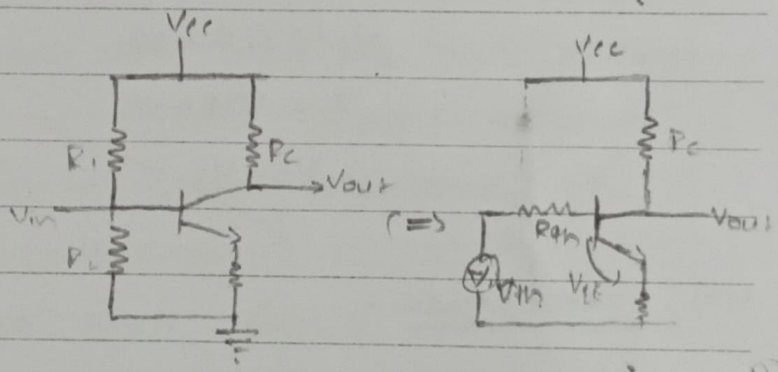
$$S = \frac{1+\beta}{1-\beta(0)}$$

$$S = 1+\beta$$

stability factor is large. The fixed bias method cannot be considered for stabilization

→ advantage of fixed bias is easy to construct

Self Biasing :-



Apply K.V.L to loop.

$$V_{th} = R_{th} I_B + V_{BE} + I_E R_E$$

$$V_{th} = R_{th} I_B + V_{BE} + (I_B + I_C) R_E$$

$$V_{th} = R_{th} I_B + V_{BE} + I_B R_E + I_C R_E$$

$$V_{th} = (R_{th} + R_E) I_B + V_{BE} + I_C R_E$$

$$V_{BE} = V_{th} - (R_{th} + R_E) I_B + I_B R_E$$

$$I_C R_E = \frac{V_{th} - V_{BE} - (R_{th} + R_E) I_B}{}$$

$$I_C = \frac{V_{th} - V_{BE} - I_B(R_{th}+R_E)}{(R_{th}+R_E)}$$

We know that $S = \frac{1+\beta}{1-\beta\left(\frac{dI_C}{dI_B}\right)}$

$$S = \frac{1+\beta}{1-\beta\left(0 - \frac{dI_B V_{BE}}{d I_B (R_{th}+R_E)}\right)}$$

$$S = \frac{1+\beta}{1-\beta\left(0 - \frac{V_{BE}(1)}{R_{th}+R_E}\right)}$$

$$S = \frac{1+\beta}{1-\beta\frac{V_{BE}}{R_{th}+R_E}}$$

$$S = \frac{1+\beta}{1-\frac{\beta}{R_{th}+R_E}}$$

$$S = \frac{1+\beta(R_{th}+R_E)}{R_{th}+R_E-\beta}$$

$$S = \frac{R_{th}R_E + \beta(R_{th}+R_E)}{R_{th}+R_E-\beta}$$

$$S = \frac{1+\beta}{1-\beta}$$

If $R_{th} \ll R_E$

stability factor is less

so fixed biasing can be used for stabilization tech-

4(c)

parameter	BJT	FET
element control	current	voltage
Thermal run away	exist	does not exist
sensitivity	Highly sensitive to temperature	low sensitive to temperature
Types	NiPiN, PNP	n-channel, p-channel

College Code : VE

BOOKLET NUMBER : 6122

SREYAS

INSTITUTE OF ENGINEERING AND TECHNOLOGY

Nagole, Hyderabad - 500 068.

MID TERM EXAMINATION ANSWER BOOKLET

Course : B.Tech / M.Tech

Branch : ECE, Section A,

Year : II, Semester : I, Mid Term Examination : 1, Month & Year : 15/12/21

Hall Ticket No : 2 0 V E 1 A 0 4 3 2

P. Ravi 15/12/21
Signature of the Student with date

Name of the Student : Patel Ravinder

Name of the Subject : Electonic devices and circuits

Date of the Exam : 15/12/21

Signature of the Invigilator with date

MARKS AWARDED FOR QUESTIONS

Q. No.	*		Marks Awarded	Sub Total
1.		a	0	0
		b		
		c		
2.		a		
		b		
		c		
3.		a		
		b		
		c		
4.		a		
		b		
		c		
			Total	0

* Student must indicate ✔ mark against the attempted question

Marks	Maximum	Awarded
Subjective	10	0
Objective	10	2 1/2
Assignment	05	3
Total	**25**	5 1/2

Pavani 17/12/21
Signature of the Evaluator with date

INSTRUCTIONS TO THE CANDIDATES :

1. Students must be present in the examination hall 15 minutes before the commencement of the examination.
2. Write H.T. No. Name etc., correct & legible and must be signed on the main answer book and attendance sheet.
3. Student must adhere to all instructions given by an Invigilator prior to, during and immediately after an examination.
4. Students are required to ensure submission of answer scripts at the end of the examination, failure to submission of answer script would be treated as absent.

START WRITING FROM HERE

Answers

1]g] filter is an filter which purified the water that is no as filter when purified the capacitor filter and which take it objectives of Rock salt is no as filter

$I_B = 100\mu A$ $I_C = 2mA$

i B of the transistor

College Code : VE

BOOKLET NUMBER : 6134

SREYAS

INSTITUTE OF ENGINEERING AND TECHNOLOGY

Nagole, Hyderabad - 500 068.

MID TERM EXAMINATION ANSWER BOOKLET

Course : B.Tech / M.Tech

Branch : ECE, Section B,

Year : 2nd, Semester : 1st, Mid Term Examination : 1, Month & Year : 12 & 21

Hall Ticket No : 2 0 V E 1 A 0 4 7 1

B Nandini 15/12/21
Signature of the Student with date

Name of the Student : BODDUPALLY NANDINI

Name of the Subject : EDC

Date of the Exam : 15/12/2021

Signature of the Invigilator with date

MARKS AWARDED FOR QUESTIONS

Q. No.	*		Marks Awarded	Sub Total
1.		a		
		b		
		c		
2.		a	2	4½
		b	2	
		c	½	
3.		a	2	4½
		b	2	
		c	½	
4.		a		
		b		
		c		
			Total	9

Marks	Maximum	Awarded
Subjective	10	9
Objective	10	7½
Assignment	05	5
Total	**25**	21½

Pavani 20/12/21
Signature of the Evaluator with date

* Student must indicate ✔ mark against the attempted question

INSTRUCTIONS TO THE CANDIDATES :

1. Students must be present in the examination hall 15 minutes before the commencement of the examination.
2. Write H.T. No. Name etc., correct & legible and must be signed on the main answer book and attendance sheet.
3. Student must adhere to all instructions given by an Invigilator prior to, during and immediately after an examination.
4. Students are required to ensure submission of answer scripts at the end of the examination, failure to submission of answer script would be treated as absent.

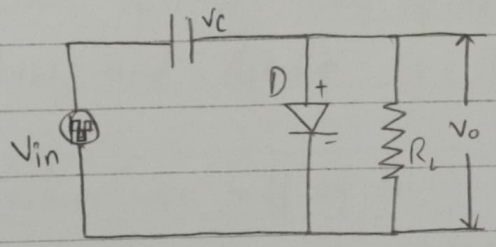
START WRITING FROM HERE

2 a) Clamplers

Clamper circuits are used to add DC value to the output.

We have 2 types of clampers positive clampler and Negative clamper.

i) Negative clampers



When the input is allowed into the circuit as capacitor allows only ac current to flow. the voltage at capacitor is equals to input voltage

$V_{in} = V_c$

When +ve half cycle the diode is in forward bias and and diode is short circuited.

No output is recieved.

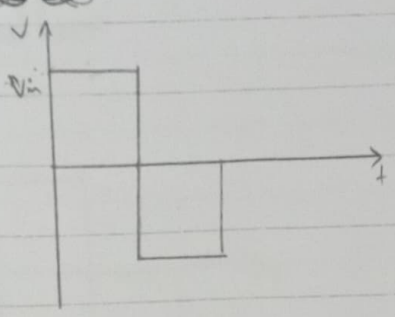
For -ve half cycle the diode is in reverse bias By KVL and the diode is Open ckt.

The given input voltage will be recieved by the Output.

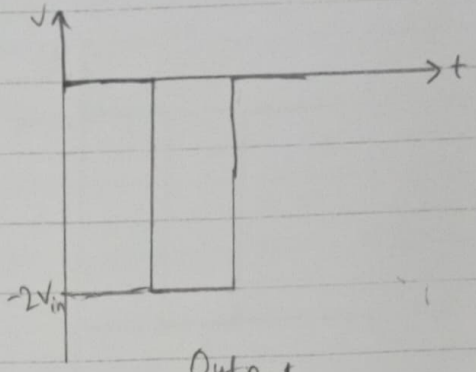
$V_{in} + V_c + V_o = 0$

$V_{in} + V_{in} = -V_o$

$V_o = -2V_{in}$



input

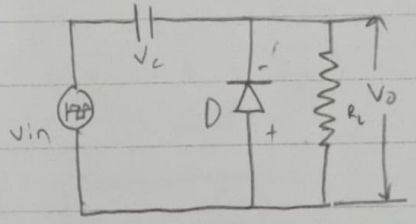


Output

Positive clampers.

When positive half cycle, the diode is in Reverse bias and diode is open circuit

When -ve half cycle, the diode is in forward bias and diode is short circuited



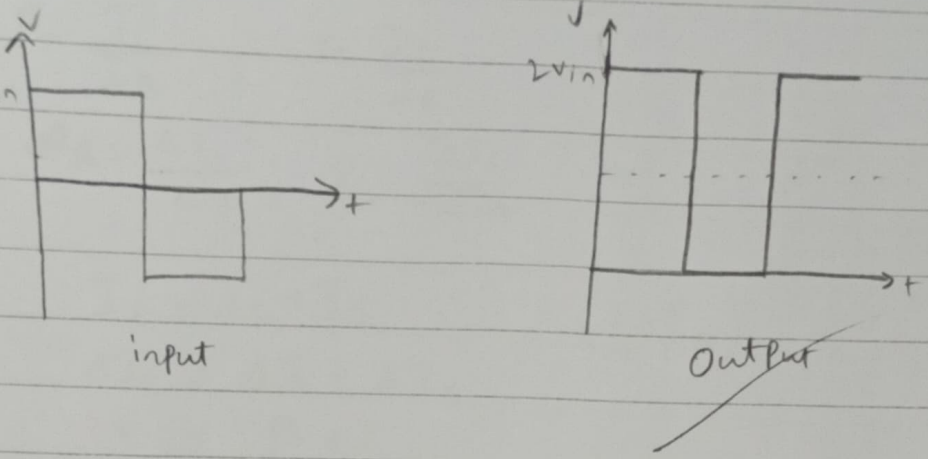
BY KVL

$V_{in} + V_c - V_o = 0$

$V_o = V_c + V_{in}$ $(V_c = V_{in})$

$V_o = V_{in} + V_{in}$

$\boxed{V_o = 2V_{in}}$



b) α , β, γ

α, β

$$\alpha = \frac{I_C}{I_E} \qquad \beta = \frac{I_C}{I_B}$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \qquad \beta = \frac{\Delta I_C}{\Delta I_B}$$

$$I_E = I_C + I_B$$

$$\Delta I_E = \Delta I_C + \Delta I_B \qquad \div \text{ by } \Delta I_C$$

$$\frac{\Delta I_E}{\Delta I_C} = 1 + \frac{\Delta I_B}{I_C} \qquad = \frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\frac{1}{\alpha} = \frac{1+\beta}{\beta}$$

$$\boxed{\alpha = \frac{\beta}{1+\beta}}$$

α, γ

$$\alpha = \frac{I_C}{I_E} \qquad \gamma = \frac{I_E}{I_B}$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \qquad \gamma = \frac{\Delta I_E}{\Delta I_B}$$

$$I_E = I_C + I_B$$

$$\Delta I_E = \Delta I_C + \Delta I_B \qquad \div \text{ by } \Delta I_E$$

$$1 = \frac{\Delta I_C}{\Delta I_E} + \frac{\Delta I_B}{\Delta I_E}$$

$$1 = \alpha + \frac{1}{\gamma} \qquad \frac{1}{\gamma} = 1 - \alpha$$

$$\boxed{\gamma = \frac{1}{1-\alpha}}$$

β, γ

$\beta = \frac{I_C}{I_B}$ $\quad \gamma = \frac{I_E}{I_B}$

$\beta = \frac{\Delta I_C}{\Delta I_B}$ $\quad \gamma = \frac{\Delta I_C}{\Delta I_B}$

$I_E = I_C + I_B \quad (\div \Delta I_B)$

$\Delta I_E = \Delta I_C + \Delta I_B$

$\gamma = \beta + 1$

$\boxed{\beta = \gamma - 1}$

γ, β α

$I_E = I_C + I_B \quad \div \Delta I_C$

$\Delta I_E = \Delta I_C + \Delta I_B$

$\frac{\Delta I_E}{\Delta I_C} = \frac{\Delta I_C}{\Delta I_C} + \frac{\Delta I_B}{\Delta I_C}$

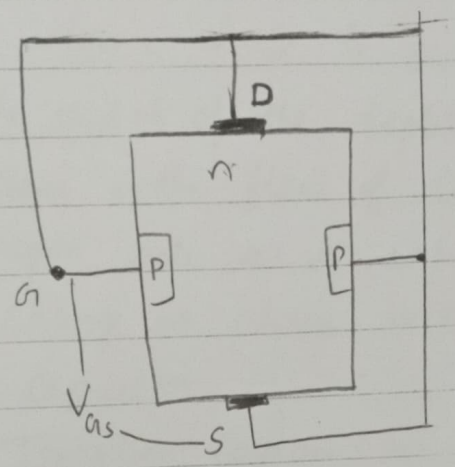
$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$

$\frac{1}{\alpha} = \frac{\beta + 1}{\beta}$

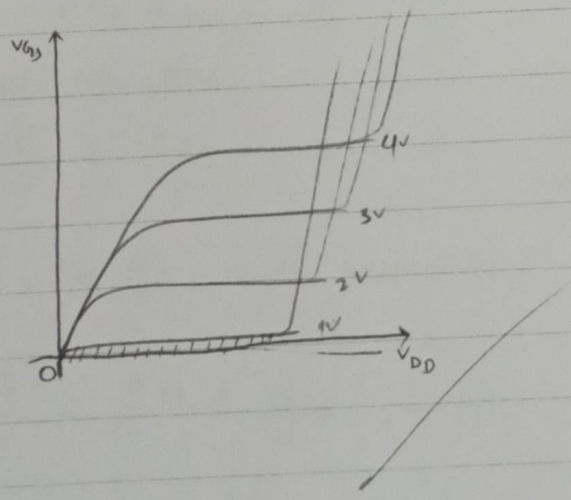
$\alpha = \frac{\beta}{\beta + 1}$ But $\boxed{\gamma = \beta + 1}$

$\boxed{\alpha = \frac{\beta}{\gamma}}$

c) n channel J FET



FET is a High impedence device.
N-type semiconductor strip is taken and two Ohmic contacts are placed at top & bottom of the strip.
2 n-type Semi Conductors are injected into the n type region. forms n channel J FET

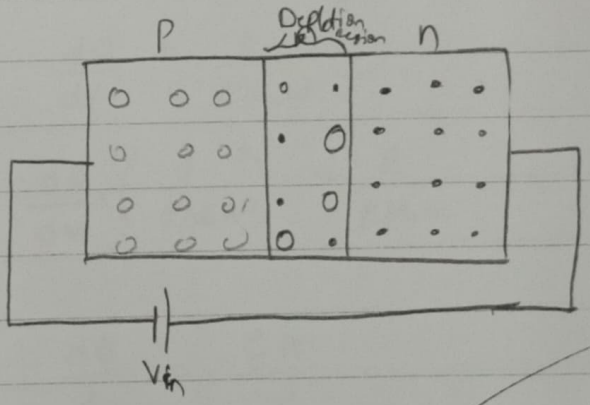


3 a) Transition Capacitance

When a diode is connected in Reverse bias The width of the depletion region increases and No chance in the flow of Current. So there the depletion region acts as a Capactor

Change in chare with respect to given voltage is capacitor.

Transition Capacitor is also known as Depletion Capacitor



$$Q = eN_a A W \quad \text{—} ①$$

Poissons equation

$$\frac{d^2V}{dx^2} = \frac{eN_a}{\varepsilon} \quad \text{—} ② \qquad \& \qquad \frac{dQ}{dV} = C_T \quad \text{—} ③$$

diff Eq ① with respect to V

$$\frac{dQ}{dV} = eN_a A \frac{dW}{dV} \quad \text{—} ④$$

Double integrate Eq (2)

$$\int\int \frac{d^2V}{dx^2}\,dx = \int\int \frac{eN_a}{\varepsilon}\,dx$$

$$V = \frac{eN_a}{\varepsilon}\,\frac{x^2}{2} \qquad (x \approx w)$$

$$V = \frac{eN_a}{\varepsilon}\,\frac{w^2}{2} \quad \text{— (5)}$$

Diff Eq 5

$$1 = \frac{eN_a}{\varepsilon}\,\frac{2w}{2}\,\frac{dw}{dV}$$

$$\frac{dw}{dV} = \frac{\varepsilon}{eN_a w}$$

$$\frac{dQ}{dV} \times \left(\frac{1}{eN_a A}\right) = \frac{\varepsilon}{eN_a w}$$

$$\frac{dQ}{dV} = \frac{\varepsilon A}{w}$$

$$\boxed{C_T = \frac{\varepsilon A}{w}}$$

width increases

Capacitance decreases

$$\boxed{C_T \propto \frac{1}{w}}$$

Diffusion Capacitance

When diode is connected in forward bias the the length of the depletion region is decreases the flow of current is easy. But there a very small depletion region acts as a capacitor called as diffusion capacitance

$$\frac{dQ}{dV} = C \qquad Q = \frac{I}{\tau}$$

$$I = \frac{Q}{\tau}$$

$$Q = I\tau \quad - (1)$$

According to diode equation

$$I = I_0 \left(e^{V/\eta V_T} - 1\right)$$

$$= I_0 e^{V/\eta V_T} - I_0 \quad - (2)$$

(2) sub in (1)

$$Q = I_0 e^{V/\eta V_T} \tau - I_0 \tau$$

Diff w.r.to V

$$\frac{dQ}{dV} = I_0 e^{V/\eta V_T} \tau \left(\frac{1}{\eta V_T}\right) - 0$$

$$\frac{dQ}{dV} = \frac{(I + I_0)\tau}{\eta V_T}$$

$I >> I_0$.

neglect I_0

$$\frac{dQ}{dV} = \frac{I\tau}{\eta V_T}$$

$$\frac{dQ}{dv} = C_D$$

$$\boxed{C_D = \frac{I\tau}{\eta V_T}}$$

$V_T \rightarrow$ Thermal voltage

$I \rightarrow$ Current

$\eta \rightarrow$ Efficied factor

$\tau \rightarrow$ lifetime of the holes

b) $I_B = 100\,\mu A$

$I_C = 2\,mA$

$I_E = I_C + I_B$

$I_E = 2\times10^{-3} + 100\times10^{-6}$

$= 2.1\times10^{-3}$

$\boxed{I_E = 2.1\,mA}$

$\beta = \frac{I_C}{I_B} = \frac{2\times10^{-3}}{100\times10^{-6}}$

$\frac{2\times10^{-3}}{50} = 20$

$\boxed{\beta = 20}$

$\alpha = \frac{I_C}{I_E} = \frac{2\times10^{-3}}{2.1\times10^{-3}} = 0.95$

$\boxed{\alpha = 0.95}$

$I_B = 100 + 25\ \mu A = 125\ \mu A$

$I_C = 2 + 0.6\ mA = 2.6\ mA$

$\beta = \frac{2.6 \times 10^{-3}}{125 \times 10^{-6}} = 20.8$

~~$\beta = 20$~~

20.8

C. FET

Field effect Transistor.

The Output Current is Controlled by input Voltage by some external field. so FET known as Voltage Controlled device.

It is also having high impence

Smaller in Size Compared to BJT.

College Code : VE

BOOKLET NUMBER : 46591

SREYAS

INSTITUTE OF ENGINEERING AND TECHNOLOGY

Nagole, Hyderabad - 500 068.

MID TERM EXAMINATION ANSWER BOOKLET

Course : B.Tech / M.Tech

Branch : ECE, Section B,

Year : IV, Semester : 1st, Mid Term Examination : 1st, Month & Year : 12 - 2021

Hall Ticket No : 2 0 V E 1 A 0 4 F 8

Signature of the Student with date

Name of the Student : M. Nithin

Name of the Subject : EDC

Date of the Exam : 15 - 12 - 2021

Signature of the Invigilator with date

MARKS AWARDED FOR QUESTIONS

Q. No.	*		Marks Awarded	Sub Total
1.		a		
		b		
		c		
2.		a		
		b		
		c		
3.		a		
		b	0	0
		c		
4.		a		
		b		
		c		
			Total	0

* Student must indicate ✔ mark against the attempted question

Marks	Maximum	Awarded
Subjective	10	0
Objective	10	4½
Assignment	05	0
Total	**25**	4½

Parvathi 20/12/21

Signature of the Evaluator with date

INSTRUCTIONS TO THE CANDIDATES :

1. Students must be present in the examination hall 15 minutes before the commencement of the examination.
2. Write H.T. No. Name etc., correct & legible and must be signed on the main answer book and attendance sheet.
3. Student must adhere to all instructions given by an Invigilator prior to, during and immediately after an examination.
4. Students are required to ensure submission of answer scripts at the end of the examination, failure to submission of answer script would be treated as absent.

START WRITING FROM HERE

3b) A transistor has $I_B = 100\mu A$ and $I_C = 2mA$.

(i) β of the transistor (ii) α of the transistor

(iii) emitter current I_E (iv) If I_B changes by $+25\mu A$ and I_C by $+0.4mA$

SREYAS
INSTITUTE OF ENGINEERING AND TECHNOLOGY
EXAMINATION BRANCH

8

Set No. 2

9-39, Sy No.107, Tattiannaram (V), GSI, Bandlaguda, Nagole, Hyderabad-500 068.

II B.TECH I SEM I MID TERM EXAMINATIONS - OBJECTIVE QUESTION PAPER - DECEMBER, 2021

Subject: **ELECTRONIC DEVICES AND CIRCUITS** Branch: **ECE**

Duration: **20 Minutes** Date: 15-12-2021 (FN) Max Marks: **10**

Name of the Student: K. shivanandh Hall Ticket No | 2 | 0 | V | B | 1 | A | 0 | 4 | 1 | 4 |

Answer All Questions. All Questions Carry Equal Marks.

I. Choose the correct alternative.

1. The most commonly used transistor arrangement is _____ arrangement [a]
   a. common emitter
   b. common base
   c. common collector
   d. none of the above
2. A JFET is a _____ driven device [b]
   a. current
   b. voltage
   c. both current and voltage
   d. none of the above
3. The collector of a transistor is _____ doped [c]
   a. Heavily
   b. Lightly
   c. Moderately
   d. None of the above
4. Which of the following statement is true about FET? [b]
   a. It has high output impedance
   b. It has high input impedance
   c. It has low input impedance
   d. It does not offer any resistance
5. The reverse current in a diode is of the order of _____ [c]
   a. kA
   b. mA
   c. μA
   d. A
6. For a clipper circuit if biasing value is same as input value, what happens to the output? [b]
   a. The total signal will be clipped off
   b. The output will be same as input
   c. The desired signal is obtained
   d. All of the above
7. If the voltage of potential barrier is V_t, a voltage V_{in} is applied at input, at what moment the barrier will disappear? [ ]
   a. $V_t < V_{in}$
   b. $V_t = V_{in}$
   c. $V_t > V_{in}$
   d. $V_t << V_{in}$

8. Transition capacitance and Diffusion capacitance occurs when the diode is connected in [d]
   a. Forward bias and Reverse bias
   b. Reverse bias and Reverse bias
   c. Forward bias and Forward bias
   d. Reverse bias and Forward bias
9. In a transistor, collector current is controlled by [b]
   a. Collector voltage
   b. Base current
   c. Collector resistance
   d. All of the above
10. Efficiency of Half wave rectifier and Full wave rectifier [d]
   a. 81.2% and 40.6%
   b. Both 40.6%
   c. Both 81.2%
   d. 40.6% and 81.2%

II Fill in the blanks:

11. Reverse voltage at which the junction breakdown occurs is known as Break down voltage.

12. Saturation drain current I_{DSS} = _____.

13. The output frequency of Full wave rectifier is same as the input frequency.

14. The diode current I_D = $I_o(e^{V/V_{TH}} - 1)$.

15. Transistor works as a switch in cut off region and saturation regions.

16. The collector junction in a transistor should be in reverse bias condition

17. Relation between α, β, γ = $\alpha = \beta/\gamma$.

18. The value of α of transistor is less than unity.

19. The function of filter is clip remove unwanted Ac signal

20. In ohmic region FET is used as voltage.

SREYAS
INSTITUTE OF ENGINEERING AND TECHNOLOGY
EXAMINATION BRANCH

Set No. 1

9-39, Sy No.107, Tattiannaram (V), GSI, Bandlaguda, Nagole, Hyderabad-500 068.

II B.TECH I SEM I MID TERM EXAMINATIONS - OBJECTIVE QUESTION PAPER - DECEMBER, 2021

Subject: **ELECTRONIC DEVICES AND CIRCUITS**

Duration: **20 Minutes** Date: 15-12-2021 (FN) Branch: **ECE**

Name of the Student: Patel Ravinder Hall Ticket No 20VE1A0432 Max Marks: **10**

Answer All Questions. All Questions Carry Equal Marks.

I. Choose the correct alternative.

1. The reverse current in a diode is of the order of _____ [c]
   a. kA
   b. mA
   c. μA
   d. A
2. The most commonly used transistor arrangement is _____ arrangement [a]
   a. common emitter
   b. common base
   c. common collector
   d. none of the above
3. A JFET is a _____ driven device [b]
   a. current
   b. voltage
   c. both current and voltage
   d. none of the above
4. Which of the following statement is true about FET? [a]
   a. It has high output impedance
   b. It has high input impedance
   c. It has low input impedance
   d. It does not offer any resistance
5. The collector of a transistor is _____ doped [c]
   a. Heavily
   b. Lightly
   c. Moderately
   d. None of the above
6. If the voltage of potential barrier is V_t, a voltage V_{in} is applied at input, at what moment the barrier will disappear? [d]
   a. $V_t < V_{in}$
   b. $V_t = V_{in}$
   c. $V_t > V_{in}$
   d. $V_t << V_{in}$
7. In a transistor, collector current is controlled by [a]
   a. Collector voltage
   b. Base current
   c. Collector resistance
   d. All of the above

8. Transition capacitance and Diffusion capacitance occurs when the diode is connected in[a]
   a. Forward bias and Reverse bias
   b. Reverse bias and Reverse bias
   c. Forward bias and Forward bias
   d. Reverse bias and Forward bias
9. Efficiency of Half wave rectifier and Full wave rectifier [d]
   a. 81.2% and 40.6%
   b. Both 40.6%
   c. Both 81.2%
   d. 40.6% and 81.2%
10. For a clipper circuit if biasing value is same as input value, what happens to the output?[c]
   a. The total signal will be clipped off
   b. The output will be same as input
   c. The desired signal is obtained
   d. All of the above

II Fill in the blanks:

11. The function of filter is _____.
12. Reverse voltage at which the junction breakdown occurs is known as _____.
13. The output frequency of Full wave rectifier is _____ the input frequency.
14. The diode current I_D = _____.
15. The collector junction in a transistor should be in _____.
16. Transistor works as a switch in _____ and _____ regions.
17. Relation between α, β, γ = _____.
18. The value of α of transistor is _____.
19. In ohmic region FET is used as _____.
20. Saturation drain current I_{DSS} = _____.

SREYAS
INSTITUTE OF ENGINEERING AND TECHNOLOGY
EXAMINATION BRANCH

Set No. 4

9-39, Sy No.107, Tattiannaram (V), GSI, Bandlaguda, Nagole, Hyderabad-500 068.

II B.TECH I SEM I MID TERM EXAMINATIONS - OBJECTIVE QUESTION PAPER - DECEMBER, 2021

Subject: **ELECTRONIC DEVICES AND CIRCUITS** Branch: **ECE**

Duration: **20 Minutes** Date: 15-12-2021 (FN) Max Marks: **10**

Name of the Student: B. Nandini Hall Ticket No | 2 | 0 | V | E | 1 | A | 0 | 4 | 7 | 1 |

Answer All Questions. All Questions Carry Equal Marks.

I. Choose the correct alternative.

1. Transition capacitance and Diffusion capacitance occurs when the diode is connected in [d]
   a. Forward bias and Reverse bias
   b. Reverse bias and Reverse bias
   c. Forward bias and Forward bias
   d. Reverse bias and Forward bias
2. The most commonly used transistor arrangement is _____ arrangement [a]
   a. common emitter
   b. common base
   c. common collector
   d. none of the above
3. A JFET is a _____ driven device [b]
   a. current
   b. voltage
   c. both current and voltage
   d. none of the above
4. The collector of a transistor is _____ doped [c]
   a. Heavily
   b. Lightly
   c. Moderately
   d. None of the above
5. In a transistor, collector current is controlled by [d]
   a. Collector voltage
   b. Base current
   c. Collector resistance
   d. All of the above
6. Which of the following statement is true about FET? [b]
   a. It has high output impedance
   b. It has high input impedance
   c. It has low input impedance
   d. It does not offer any resistance
7. The reverse current in a diode is of the order of _____ [c]
   a. kA
   b. mA
   c. μA
   d. A

8. For a clipper circuit if biasing value is same as input value, what happens to the output? [b]
   a. The total signal will be clipped off
   b. The output will be same as input
   c. The desired signal is obtained
   d. All of the above
9. If the voltage of potential barrier is V_t, a voltage V_{in} is applied at input, at what moment the barrier will disappear? [c]
   a. $V_t < V_{in}$
   b. $V_t = V_{in}$
   c. $V_t > V_{in}$
   d. $V_t << V_{in}$
10. Efficiency of Half wave rectifier and Full wave rectifier [d]
   a. 81.2% and 40.6%
   b. Both 40.6%
   c. Both 81.2%
   d. 40.6% and 81.2%

II Fill in the blanks:

11. Reverse voltage at which the junction breakdown occurs is known as cut off voltage.
12. The output frequency of Full wave rectifier is same the input frequency.
13. The diode current I_D = $I_D = I_0(e^{V/\eta V_T} - 1)$.
14. Saturation drain current I_{DSS} = V_{GS} at 0.
15. Transistor works as a switch in cutoff and saturation regions.
16. Relation between α, β, γ = $\alpha = \frac{\beta}{\gamma}$.
17. The value of α is less than 1 ≈ 0.81
18. The function of filter is eliminates ac component
19. In ohmic region FET is used as Source & Drain.
20. The collector junction in a transistor should be in Reverse biase for active region

SREYAS
INSTITUTE OF ENGINEERING AND TECHNOLOGY
EXAMINATION BRANCH

Set No. 1

(2)

9-39, Sy No.107, Tattiannaram (V), GSI, Bandlaguda, Nagole, Hyderabad-500 068.

II B.TECH I SEM I MID TERM EXAMINATIONS - OBJECTIVE QUESTION PAPER - DECEMBER, 2021

Subject: **ELECTRONIC DEVICES AND CIRCUITS**

Duration: **20 Minutes** Date: 15-12-2021 (FN) Branch: **ECE**

Max Marks: **10**

Name of the Student: K. Rajesh Hall Ticket No 2 0 4 E 1 A 0 4 8 2

Answer All Questions. All Questions Carry Equal Marks.

I. Choose the correct alternative.

1. The reverse current in a diode is of the order of _____ [a]
   a. kA
   b. mA
   c. μA
   d. A
2. The most commonly used transistor arrangement is _____ arrangement [b]
   a. common emitter
   b. common base
   c. common collector
   d. none of the above
3. A JFET is a _____ driven device [b]
   a. current
   b. voltage
   c. both current and voltage
   d. none of the above
4. Which of the following statement is true about FET? [d]
   a. It has high output impedance
   b. It has high input impedance
   c. It has low input impedance
   d. It does not offer any resistance
5. The collector of a transistor is _____ doped [b]
   a. Heavily
   b. Lightly
   c. Moderately
   d. None of the above
6. If the voltage of potential barrier is V_t, a voltage V_{in} is applied at input, at what moment the barrier will disappear? [a]
   a. $V_t < V_{in}$
   b. $V_t = V_{in}$
   c. $V_t > V_{in}$
   d. $V_t << V_{in}$
7. In a transistor, collector current is controlled by [d]
   a. Collector voltage
   b. Base current
   c. Collector resistance
   d. All of the above

8. Transition capacitance and Diffusion capacitance occurs when the diode is connected in[d]
   a. Forward bias and Reverse bias
   b. Reverse bias and Reverse bias
   c. Forward bias and Forward bias
   d. Reverse bias and Forward bias
9. Efficiency of Half wave rectifier and Full wave rectifier [a]
   a. 81.2% and 40.6%
   b. Both 40.6%
   c. Both 81.2%
   d. 40.6% and 81.2%
10. For a clipper circuit if biasing value is same as input value, what happens to the output?[a]
   a. The total signal will be clipped off
   b. The output will be same as input
   c. The desired signal is obtained
   d. All of the above

II Fill in the blanks:

11. The function of filter is _____.
12. Reverse voltage at which the junction breakdown occurs is known as _____.
13. The output frequency of Full wave rectifier is _____ the input frequency.
14. The diode current I_D = _____.
15. The collector junction in a transistor should be in _____.
16. Transistor works as a switch in _____ and _____ regions.
17. Relation between α, β, γ = _____.
18. The value of α of transistor is _____.
19. In ohmic region FET is used as _____.
20. Saturation drain current I_{DSS} = _____.

S.No	Yr/Br/Sc	Hall Ticket No.	Student Name	Descriptive Question Wise Marks(MID-I)												I DES (10)	I OBJ (10)	I ASN (5)	I MID (25)
				Q1			Q2			Q3			Q4						
				CO1	CO2	CO3	CO1	CO2	CO3	CO1	CO2	CO3	CO1	CO2	CO3				
				A 2	B 2	C 1	A 2	B 2	C 1	A 2	B 2	C 1	A 2	B 2	C 1				
1	II-I ECE-A	20VE1A0401	AKKENAPALLY SHIVA BHANU				1.5	1.5					1.5	0.5		5	4.5	5	15
2	II-I ECE-A	20VE1A0402	ALUGUVELLI RUCHITHA				1	2					2			5	2.5	5	13
3	II-I ECE-A	20VE1A0403	AMANCHI MANI MEKHALA	1.5	1.5	0.5							2	2	1	8.5	3	5	17
4	II-I ECE-A	20VE1A0404	APPIDI YOGESHWAR REDDY	0.5			0.5	1								2	5	5	12
5	II-I ECE-A	20VE1A0405	B SOWMYA	0.5			1	1.5					2		1	5.5	6.5	5	17
6	II-I ECE-A	20VE1A0406	BHOOMI REDDY VARUN REDDY				0.5	1					2		1	4.5	7	5	17
7	II-I ECE-A	20VE1A0407	BUKKALA PRAVALYA	1.5	0.5								2			4	3.5	5	13
8	II-I ECE-A	20VE1A0408	GOLKONDA RACHANA				1	2	0.5				2	0.5	1	7	3.5	5	16
9	II-I ECE-A	20VE1A0409	GOPI REDDY MANASA REDDY				1	2					2	1.5	1	7.5	4	5	17
10	II-I ECE-A	20VE1A0410	GUNTI NAGARAJU				1.5	1.5					2		0	5	4	5	14
11	II-I ECE-A	20VE1A0411	KOLANU VARUN RAJU	1.5	1	1	0.5	2	0.5							6.5	6.5	5	18
12	II-I ECE-A	20VE1A0412	KOLLURU KAUSHIK				0.5									0.5	3	5	9
13	II-I ECE-A	20VE1A0413	KONDOJU VAISHNAVI				1.5	2		1.5	0.5					5.5	3.5	5	14
14	II-I ECE-A	20VE1A0414	KORIPELLY SHIVANANDH REDDY							2	2	1	2	2	1	10	8	5	23
15	II-I ECE-A	20VE1A0415	MAHAMMAD NAZEERUDDIN				1.5			1.5		0			0.5	3	4.5	5	13
16	II-I ECE-A	20VE1A0416	MARAGANI GANESH MAHA DEV				0									0	3	5	8
17	II-I ECE-A	20VE1A0417	MARAGANI RUKMINI				1.5	2							1	4.5	3	5	13
18	II-I ECE-A	20VE1A0418	MARKU SAI HRUSHIK				1	1.5		0.5						3	5.5	5	14
19	II-I ECE-A	20VE1A0419	MUDDAM CHITTI TEJASWINI				0.5	2			1.5	0.5	0.5	2	1	6	4.5	5	16
20	II-I ECE-A	20VE1A0420	MUSKU MANISHA				1.5	1.5	0.5	2			2		1	6.5	5.5	5	17
21	II-I ECE-A	20VE1A0421	NALLA PRIYA	1.5		1	0.5	2	0				0.5	1		5	6	5	16
22	II-I ECE-A	20VE1A0422	NALLABOINA MUNI SAI			0.5	1			0.5						1.5	5.5	5	12
23	II-I ECE-A	20VE1A0423	NAMDHAR VISHAL	0.5		0.5	0.5	1.5		0.5		0.5				3	5.5	5	14
24	II-I ECE-A	20VE1A0424	NYAYAM SANTHOSH REDDY	1.5	0.5	0	0.5	0.5	0							3	4	5	12
25	II-I ECE-A	20VE1A0425	PADARAJU VAISHNAVI				2	1.5	0.5	1.5	1.5	0.5				7.5	3	5	16
26	II-I ECE-A	20VE1A0426	PAGIDIMARRY CHARAN	1	0.5		2	1.5	0							5	6	5	16
27	II-I ECE-A	20VE1A0427	PANAK[redacted]NANDU				2	2	1	1.5	2	0.5				[redacted]	4.5	5	19
28	II-I ECE-A	20VE1A0428	PARSHI SRAVYA				2	1.5	0.5				2	0	1	7	5	5	17
29	II-I ECE-A	20VE1A0429	PARVATHANENI SNEHA SREE				1.5	1.5	0.5						1	4.5	5	5	15
30	II-I ECE-A	20VE1A0430	POKALA MANIK PRABHU	0.5			2	1.5	0.5	1.5	2					7.5	7.5	5	20
31	II-I ECE-A	20VE1A0431	POKALA SAI GOPAL	2	2	1	2	1.5	0.5							9	5.5	5	20
32	II-I ECE-A	20VE1A0432	POLICE PATEL RAVINDER REDDY	0												0	2.5	3	6
33	II-I ECE-A	20VE1A0433	POLOJU MANASA	2			1.5		0.5							5	3.5	5	14
34	II-I ECE-A	20VE1A0434	POTHULA GOURINATH REDDY		0.5	1	1.5	0.5		1					1	3.5	4	5	13
35	II-I ECE-A	20VE1A0435	PRADYUMNA KINHALKAR				1	2	0				1.5	1	1	6.5	4.5	5	16
36	II-I ECE-A	20VE1A0436	PULLURI MAHALAXMI				0	2	0.5				1.5	2	1	7	2	5	14
37	II-I ECE-A	20VE1A0437	PUPPALA BHANU PRASAD				1.5	2	0	1.5	2					7	5	5	17
38	II-I ECE-A	20VE1A0438	RACHAKONDA HARI VARMA				1.5	0.5	0	1						3	3	5	11
39	II-I ECE-A	20VE1A0439	RAJNISH CHAUBEY	0.5		0.5	1.5									2.5	3.5	5	11
40	II-I ECE-A	20VE1A0440	RAMAVATH ABHINAY	0.5			1.5	0.5								2.5	2	5	10
41	II-I ECE-A	20VE1A0441	RAMAVATH DHARMA TEJA				1.5	1.5		1.5	2	0.5				7	5	5	17
42	II-I ECE-A	20VE1A0443	SAMA VIGNESH REDDY	2			1.5	2					1.5		1	6	4	5	15
43	II-I ECE-A	20VE1A0444	SAMANURI SRIHARI VARMA	0.25			0.25									0.5	3.5	5	9
44	II-I ECE-A	20VE1A0445	SAMUDRAM HARSHITH TEJA				1.5			1.5		0.5				3.5	3	5	12
45	II-I ECE-A	20VE1A0446	SEELAM SAKET				1.5	2					1.5		1	6	2.5	5	14
46	II-I ECE-A	20VE1A0447	SHATHAM SANDEEP KUMAR				1.5	1	0.5						0.5	3.5	3	5	12
47	II-I ECE-A	20VE1A0448	SIPATHI MANOJ KUMAR		0	0	0.5		0						0	0.5	1.5	5	7
48	II-I ECE-A	20VE1A0449	SRIRAMOJU SRIKAR				1				0					1	1.5	5	8
49	II-I ECE-A	20VE1A0450	SUNKARA HARIKA				2	1	0.5				1.5	2	0.5	7.5	3	5	16
50	II-I ECE-A	20VE1A0451	SURABHI MAHESH											2		2	2.5	5	10
51	II-I ECE-A	20VE1A0452	TALLA SRI SWAPNA REDDY				1.5						1.5	2	0	5	2	5	12
52	II-I ECE-A	20VE1A0453	TANNERU HEMA LATHA				2	1.5					2		0	5.5	5	5	16
53	II-I ECE-A	20VE1A0454	THOKALA GANESH				1	1							0.5	2.5	3	5	11
54	II-I ECE-A	20VE1A0455	THUDI MANASWI				1	1.5					0		1	3.5	5	5	14
55	II-I ECE-A	20VE1A0456	THUMMALAPALLI HIMABINDHU	0	1.5	1				1		0	1.5		0.5	4.5	2.5	5	12
56	II-I ECE-A	20VE1A0457	VARRA NAVEEN REDDY	0			1						1.5			2.5	1	3	7
57	II-I ECE-A	20VE1A0458	YATIRAJAM B KUMAR	1.5												1.5	2	4	8
58	II-I ECE-A	20VE1A0459	YELLAMPALLI VENKATA NAGA			1	1									2	2	5	9
59	II-I ECE-A	20VE1A0460	YELLAMPALLI VENKATA SIVA SAI			1	1									2	2.5	5	10
60	II-I ECE-A	21VE5A0401	ALUGADDA VIGNESH				1.5	1.5	0.5						1	4.5	4	5	14
61	II-I ECE-A	21VE5A0402	BOJJA NITHIN																
62	II-I ECE-A	21VE5A0403	BOODIDA KIREETI GOUD	2	1.5	1	1									5.5	8	5	19
63	II-I ECE-A	21VE5A0404	BUNREDDY VISHNU VARDHAN	0.5	1	1	1	0.5								4	6	5	15
64	II-I ECE-A	21VE5A0405	DEVUNOORI PRIYANKA	1	1	1	1.5	1.5	1							7	8	5	20
65	II-I ECE-A	21VE5A0406	KODALI SHALEM	1	1.5	1	2	1	1	1	0.5	1				7.5	7	5	20
66	II-I ECE-A	21VE5A0407	VALLALA MOHITH	1.5	1.5	0.5	1	1.5	0.5							6.5	6	5	18

Signature of the Faculty

Signature of the HOD

1	II-I ECE-B	20VE1A0461	ADDALA VIMALA KUMARI	0.5			2	2	0.5	0	1.5	0.5				6.5	4.5	5	16
2	II-I ECE-B	20VE1A0462	ADLA DEEPTHI				1.5	2	0.5	2	1.5	0.5				8	6.5	5	20
3	II-I ECE-B	20VE1A0463	AKARAPU YAMINI					1.5	0.5							6	6.5	5	18
4	II-I ECE-B	20VE1A0464	AKSHAY RAGIPHANI	2	1.5	0.5	2						1			8	7.5	5	16
5	II-I ECE-B	20VE1A0465	AMDA HARSHITHA	0			1.5	2	0	2	0.5	0.5				6.5	6.5	5	18
6	II-I ECE-B	20VE1A0466	AVULA PALLAVI				2	2	0				1.5	0.5	1	7	6.5	5	19
7	II-I ECE-B	20VE1A0467	BACHSHANKAR YUVRAJ SINGH				1.5	2	0	2						2	5	5	12
8	II-I ECE-B	20VE1A0468	BANDARI KUSHI				1.5	1.5					1.5		1	6	5	5	16
9	II-I ECE-B	20VE1A0469	BARAKA CHARAN KUMAR				2	2	0.5	2	2	0.5	2	2	1	8	5.5	5	19
10	II-I ECE-B	20VE1A0471	BODDUPALLY NANDINI													9	7.5	5	22
11	II-I ECE-B	20VE1A0472	DADINABOYINA AKSHAY YADAV				1	1.5											
12	II-I ECE-B	20VE1A0473	DASARI SIDDHARTHA												1	3.5	3.5	4	11
13	II-I ECE-B	20VE1A0474	DEVULAPALLY SWATHI	0.5	2	0.5							2	2	1	8	4	5	17
14	II-I ECE-B	20VE1A0475	DINDU MANI KRISHNA GOUD																
15	II-I ECE-B	20VE1A0476	GANDHAM VEERABABU							2						2.5	5.5	3	11
16	II-I ECE-B	20VE1A0477	GATTU SHREYA REDDY	0.5	0					1	1		1.5		1	6	6.5	5	18
17	II-I ECE-B	20VE1A0478	GAYANI SATHVIKA VEMPATI				1.5	2				0.5	1.5	2	1	7	5	5	17
18	II-I ECE-B	20VE1A0479	JALLA ANUSHA	1.5		1		1.5					1		1	5.5	4.5	5	15
19	II-I ECE-B	20VE1A0480	JEELA NAVEEN				1.5	2					1.5			2.5	5	5	13
20	II-I ECE-B	20VE1A0481	KARNATI VAMSHIKRISHNA	0.5			0.5	1.5											
21	II-I ECE-B	20VE1A0482	KOLLIPARA RAJESH													2.5	2	5	10
22	II-I ECE-B	20VE1A0483	KOTAPATI SATHYA VARA PRASAD	0.5			0.5	1.5					0.5			0	5	3	8
23	II-I ECE-B	20VE1A0484	LODANGI RAKESH	0	0		0							0	0	4.5	5	5	15
24	II-I ECE-B	20VE1A0485	M JAGALINGA	1	1	1	0.5	0	1				0.5		1	6.5	3.5	5	15
25	II-I ECE-B	20VE1A0486	MACHIPEDDI PRAVALIKA				1	1					2	1.5	1	8.5	5	5	19
26	II-I ECE-B	20VE1A0487	MANCHALA SAI HARSHITH				1.5	2					2	2	1	4.5	4	5	14
27	II-I ECE-B	20VE1A0488	MARRIPELLI NITHIN				1.5	0.5					1.5		1		4.5		5
28	II-I ECE-B	20VE1A0489	MERUGU PAVAN GOUD													4.5	4.5	5	14
29	II-I ECE-B	20VE1A0490	NADIMGERI ANIL KUMAR				1	2					0.5		1				
30	II-I ECE-B	20VE1A0491	NARAHARI ANUDEEP REDDY					1.5					0.5		1	3	5	5	13
31	II-I ECE-B	20VE1A0492	NELLIKONDI AJAY KUMAR REDDY	1.5	2								0.5	1.5	1	6.5	4	5	16
32	II-I ECE-B	20VE1A0493	NUTANAKANTI PAVAN	2	1	1	1	0.5								5.5	4.5	5	15
33	II-I ECE-B	20VE1A0494	P PRANATHI																
34	II-I ECE-B	20VE1A0495	PENDYALA MAHANTH	1	1	1	2	2	0.5							8.5	4.5	5	18
35	II-I ECE-B	20VE1A0497	PONUGOTI SWATHANTRA RAO				1.5									2.5	3.5	5	11
36	II-I ECE-B	20VE1A0498	RAMISETTI KIREETI		1	1	1.5	1	0.5							5	4	5	14
37	II-I ECE-B	20VE1A0499	RANGINEENI YASASWINI SATHYA	1	1.5	1	1	1.5	0.5							6.5	5.5	5	17
38	II-I ECE-B	20VE1A04A0	RAPOL BHARGAV REDDY				1.5	2								6.5	3.5	5	15
39	II-I ECE-B	20VE1A04A1	SEELAM SUNIL					0.5		0.5			1.5	0.5	1	1	3	3	7
40	II-I ECE-B	20VE1A04A2	SHAIK NASIR HUSSAIN		0.5								0.5			0.5		5	6
41	II-I ECE-B	20VE1A04A3	SHAMPURI BINDHU SRI										0.5			1	2	5	8
42	II-I ECE-B	20VE1A04A4	SINGIREDDY CHANDRA SHEKAR				1	2					2		0.5	5.5	2.5	5	13
43	II-I ECE-B	20VE1A04A5	SUREPALLY ADITH				0.5								0.5	1	2.5	5	9
44	II-I ECE-B	20VE1A04A6	TADI NAGA BHAGYA SRI	1.5	1	0.5	1.5	1								5.5	6	5	17
45	II-I ECE-B	20VE1A04A7	THORRURU SONYPRIYA	1		1	2	2	0.5							6.5	4	5	16
46	II-I ECE-B	20VE1A04A8	VALLAKATI NANDU	2		1	1.5	2								6.5	6.5	5	18
47	II-I ECE-B	20VE1A04A9	VANJA LAHARI REDDY	0.5	1.5	1	1.5	1.5								6	4.5	5	16
48	II-I ECE-B	20VE1A04B0	VIGRAHALA VENKATA DHRITI				1	1.5								5	4	5	14
49	II-I ECE-B	20VE1A04B1	VISLAVATH MACHENDER				2	2					1	0.5	1	6.5	4.5	5	16
50	II-I ECE-B	20VE1A04B2	VYDYULA RISHITHA	0.5	0.5	1	1.5		0.5				1.5		1	4	4	5	13
51	II-I ECE-B	20VE1A04B3	YEJARLA NARASIMHA							2	2	0.5	2	2		8.5	6.5	5	20
52	II-I ECE-B	20VE1A04B4	B KISHORE CHAND				2		0.5				0.5		1	4	4	4	12
53	II-I ECE-B	20VE1A04B5	CHAMA VAMSHIDHAR REDDY	0.5	0.4	0.5	1									2.4	4	5	12
54	II-I ECE-B	20VE1A04B6	SHAIK AYAZ																
55	II-I ECE-B	21VE5A0408	BAGANI SHAIK ALTHAF BASHA				2	0.5	0.5						0	0	0.5	0	1
56	II-I ECE-B	21VE5A0409	CHAMBETI VENKATA SAI	0.5		1	1.5	0.5					0.5	0.5	1	5	4	5	14
57	II-I ECE-B	21VE5A0410	GAVVALA SAI TEJA	1	1.5	1	2	2								3.5	6	5	15
58	II-I ECE-B	21VE5A0411	GUGULOTHU SRINATH				1.5	2								7.5	6	5	19
59	II-I ECE-B	21VE5A0412	JINKALA KARTHIK	1		1							2	0.5	1	7	6.5	5	19
60	II-I ECE-B	21VE5A0413	MATAM SAI NITHIN	1.5	1.5	0.5	2	2	0.5				2	2	1	7	2.5	5	15
61	II-I ECE-B	21VE5A0414	VEERABOMMA PRASANTH				2	2	1							8	3	5	16
62	II-I ECE-B	21VE5A0415	MANGALI MADHU LOHITH				0.5						1.5	0.5	1	8	5.5	5	19
																0.5	2.5	0	3
Total Marks				CO1	CO2	CO3	CO1	CO2	CO3	CO1	CO2	CO3	CO1	CO2	CO3				
No of Students Answered				49.75	32.4	30	130.25	124	18	37	24.5	8	74	36.5	44.5	582.4	529	582	1725
No of Students scoring > threshold				50	31	37	101	82	41	27	17	16	52	28	54	121	121	121	122
% of students scoring > thershold				28	21	35	83	71	31	22	13	14	40	18	48	67	49	119	85
				56.0	67.7	94.6	82.2	86.6	75.6	81.5	76.5	87.5	76.9	64.3	88.9	55.4	40.5	98.3	69.7

Sl.No	MID -II Question paper	BTLs	COs	Marks
1a	Analyse the transistor amplifier circuit using h-parameters	4	5	2
1b	Explain JFET parameters and small signal model of JFET	2	6	2
1c	Explain the working of Tunnel diode with energy band diagrams	4	4	1
2a	Explain simplified hybrid model. Analyse CE amplifier using simplified hybrid model.	2	5	2
2b	Explain CS FET amplifier and derive the expressions of A_I, Zi, A_V, Z_o	2	6	2
2c	Explain the characteristics of UJT	2	4	1
3a	A CE amplifier is driven by a voltage source of internal resistance R_s=800Ω. The load impedance is a resistance of 2KΩ. The h-parameters are h_{ie}=1.1KΩ, h_{fe}=50, h_{oe}=μʊ, h_{re}=2.5*10^{-4}. Compute A_I, Z_i, A_V, Z_0 and Z_0', A_p using (i) Exact analysis, (ii) Approximate analysis. Compute % error in A_I.	3	5	2
3b	Compare (i)BJT, FET, (ii)JFET, MOSFET, (iii)EMOSFET, DMOSFET	4	6	2
3c	Explain how Zener diode works as a voltage regulator	2	4	1
4a	Determine CE h-parameters from transistor characteristics	4	5	2
4b	Explain CS D-MOSFET amplifier	2	6	2
4c	Explain different working modes of SCR	2	4	1

College Code : VE

BOOKLET NUMBER : 6701

SREYAS

INSTITUTE OF ENGINEERING AND TECHNOLOGY

Nagole, Hyderabad - 500 068.

MID TERM EXAMINATION ANSWER BOOKLET

Course : B.Tech / M.Tech

Branch : ECE, Section A,

Year : II, Semester : I, Mid Term Examination : I, Month & Year : 16/02/22

Hall Ticket No : 2 0 V E 1 A 0 4 0 3

A.Mani Mekhala 16/02/22
Signature of the Student with date

Name of the Student : A.Mani Mekhala

Name of the Subject : EDC

Date of the Exam : 16/02/22

16/2/22
Signature of the Invigilator with date

MARKS AWARDED FOR QUESTIONS

Q. No.	*		Marks Awarded	Sub Total
1.		a	2	4½
		b	1½	
		c	1	
2.		a	2	5
		b	2	
		c	1	
3.		a		
		b		
		c		
4.		a		
		b		
		c		
			Total	9½

* Student must indicate ✔ mark against the attempted question

Marks	Maximum	Awarded
Subjective	10	9½
Objective	10	8½
Assignment	05	5
Total	**25**	23

Pavani 24/2/22
Signature of the Evaluator with date

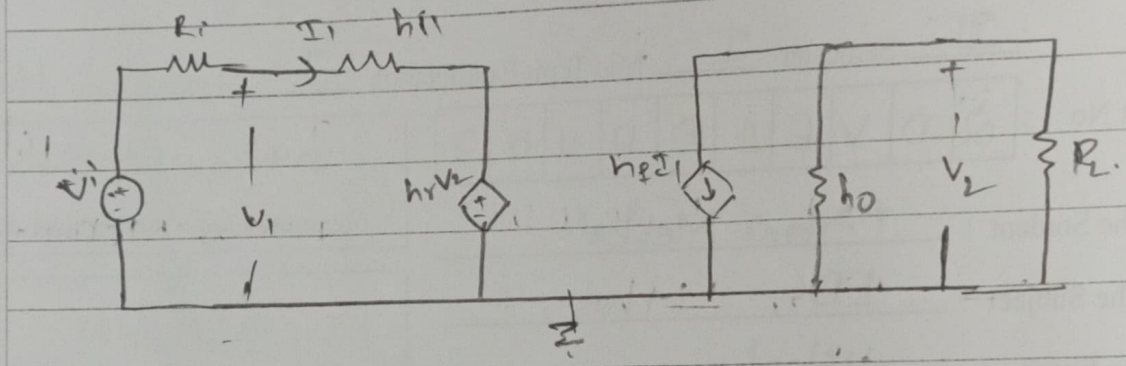
INSTRUCTIONS TO THE CANDIDATES :

1. Students must be present in the examination hall 15 minutes before the commencement of the examination.
2. Write H.T. No. Name etc., correct & legible and must be signed on the main answer book and attendance sheet.
3. Student must adhere to all instructions given by an Invigilator prior to, during and immediately after an examination.
4. Students are required to ensure submission of answer scripts at the end of the examination, failure to submission of answer script would be treated as absent.

START WRITING FROM HERE

1a) H-parameters : $V_1 = h_i I_1 + h_r V_2$ — (1)

$I_2 = h_f I_1 + h_o V_2$ — (2)



1) Current gain: $A_i = \frac{I_2}{I_1} = \frac{-I_2}{I_1}$

$$\boxed{I_2 = -I_2}$$

From eq (2) $I_2 = h_f I_1 + h_o V_2$ — (3)

$V_2 = -I_2 Z_L = -I_2 R_L$

$I_2 = h_f I_1 + h_o (-I_2 Z_L)$

$I_2 = h_f I_1 - h_o I_2 Z_L$

$I_2 + h_o I_2 Z_L = h_f I_1$

$I_2 (1 + h_o Z_L) = h_f I_1$

$\frac{I_2}{I_1} = \frac{h_f}{1 + h_o Z_L}$

$$\boxed{A_i = \frac{-I_2}{I_1} = \frac{-h_f}{1 + h_o Z_L}}$$

input impedance:

$$Z_i = \frac{V_1}{I_1}$$

from eq ①

$$V_1 = h_i I_1 + h_r V_2$$

$$Z_i = \frac{h_i I_1 + h_r V_2}{I_1}$$

$$h_i + \frac{h_r V_2}{I_1} \rightarrow ②$$

$V_2 = A_i I_1 Z_L$ sub in ②

$$h_i + \frac{h_r (A_i I_1 Z_L)}{I_1}$$

$$Z_i = h_i + \frac{h_r (A_i I_1 Z_L)}{I_1}$$

$$Z_i = h_i + h_r (A_i Z_L)$$

$$h_i + h_r \left(\frac{-h_f}{1 - h_o Z_L} \right) Z_L$$

$$h_i - \frac{h_r h_f}{Z_L \left(\frac{1}{Z_L} - h_o \right)} Z_L$$

$$\boxed{Z_i = h_i - \frac{h_r h_f}{\frac{1}{Z_L} - h_o}}$$

Voltage gain:

$$A_v = \frac{V_2}{V_1}$$

$$V_2 = A_i I_1 Z_L$$

$$A_v = \frac{A_i I_1 Z_L}{V_1}$$

$$\boxed{A_v = \frac{A_i Z_L}{Z_i}}$$

Output admitance

$$Y_o = \frac{I_2}{V_2} \quad \ldots 1$$

$$I_2 = h_f I_1 + h_o V_2$$

$$V_2 = A I_1 Z_L$$

$$Y_o = \frac{h_f I_1 + h_o (A I_1 Z_L)}{V_2}$$

$$Y_o = \frac{I_1 (h_f + h_o A Z_L)}{V_2} \quad \rightarrow (1)$$

from ckt

$$R_1 I_1 + h_{11} I_1 + h_r V_2 = 0$$

$$I_1 (R_1 + h_{11}) = -h_r V_2$$

$$\frac{I_1}{V_2} = \frac{-h_r}{R_1 + h_{11}} \quad \rightarrow (2)$$

(2) in (1)

$$Y_o = h_f \left[\frac{-h_r}{R_1 + h_{11}} \right] + \frac{h_r (A I_1 Z_L)}{V_2}$$

$$Y_o = A_o - \frac{h_r h_f}{h_i + R_s}$$

4b) Small signal model of JFET:- In FET there are 2 types of they are low frequency analyses and High frequency analysis

Low frequency analysis:-

$$I_D = g_m \mu V_{gs} + \frac{V_{ds}}{r_d}$$

Here the drain current is obtained from transconductance and gate to source voltage. The product of g_m and μV_{gs} describes drain current I_D also depends upon internal resistance 'r_d' described as impedence If also depends upon V_{ds}.

1½

High frequency analysis:- In high frequency analysis the junction capacitances like C_{GS}, C_{DS}, C_{GD} creates a feed back in between input and output. This feedback plays a crucial role in high frequency analysis. This feedback decrease voltage amplification and increases frequency.

→ There are three JFET parameters
→ Transconductance (g_m)
→ dynamic drain component (r_{ds})
→ Amplifaction factor (μ)

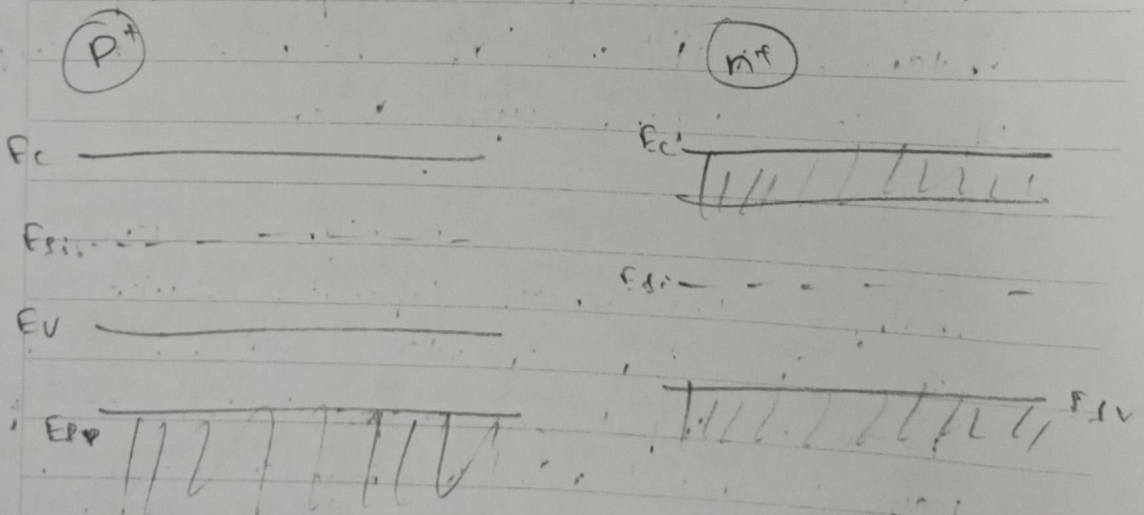
→ Trans Conductance:- It is the ration of

$$g_m = \left.\frac{\partial V_{ds}}{\partial V_{GS}}\right|_{g_{DS}=\text{constant}}$$

→ dynamic drain resistance = $\frac{1}{\text{slope of drain characteristics}}$

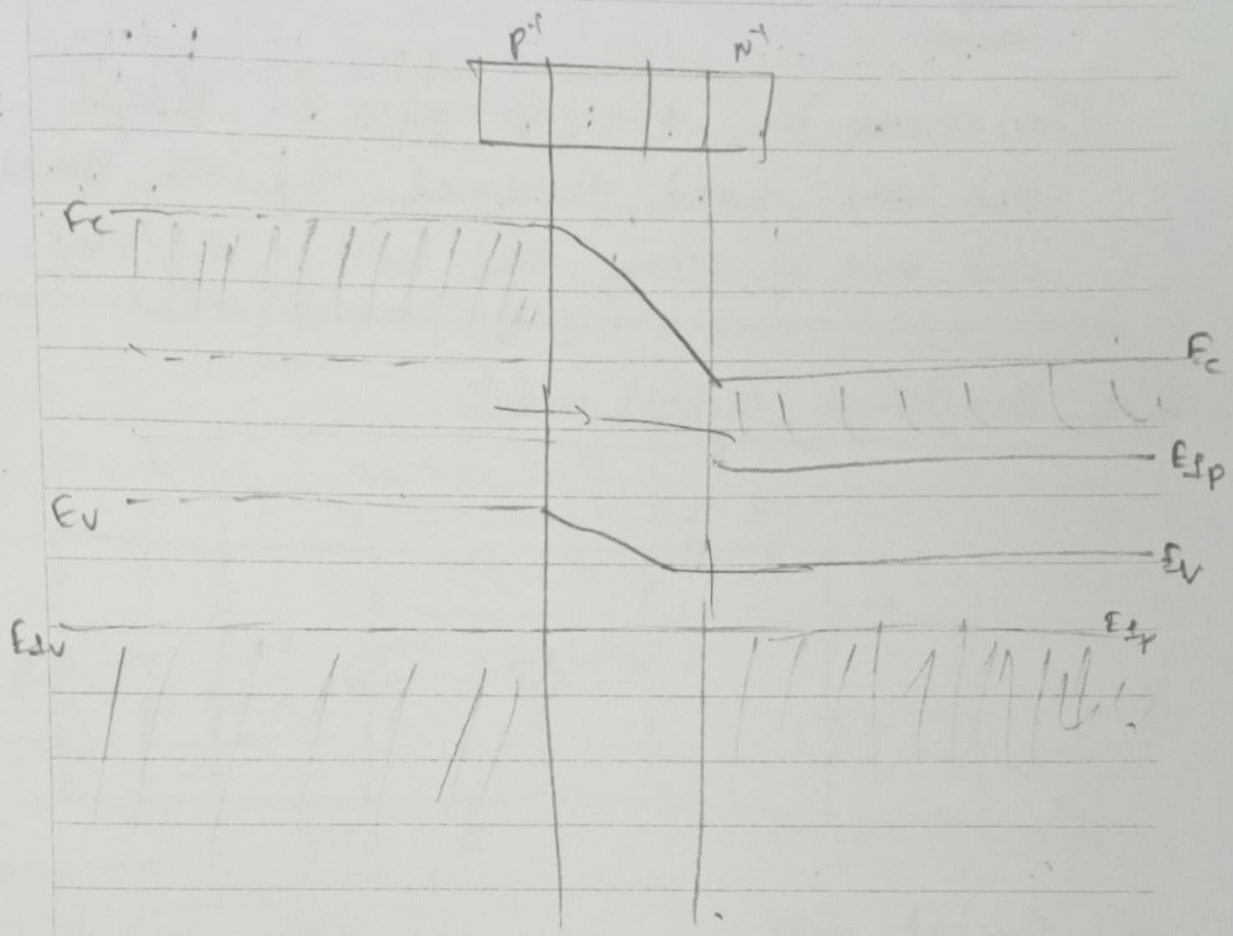
→ Amplification factor:- $\mu = g_m * r_{ds}$

4c) Tunnel diode is heavily doped.

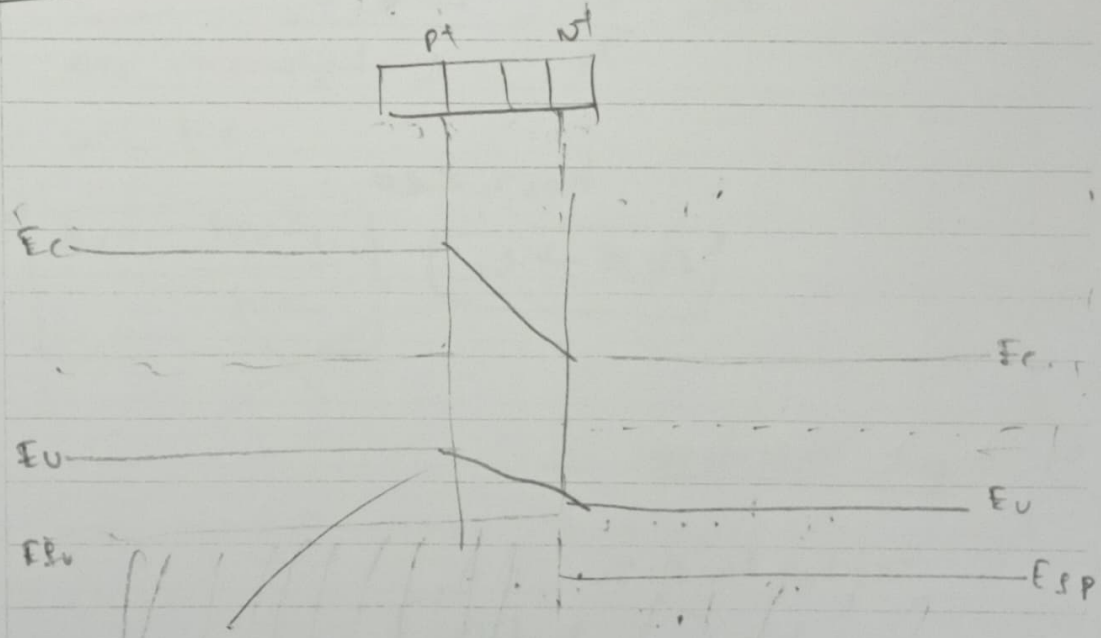


In forward bias:-

When +ve is given to ~~and~~ N type then the band increases +eV times and net of energy band width = $e(V-V_o)$

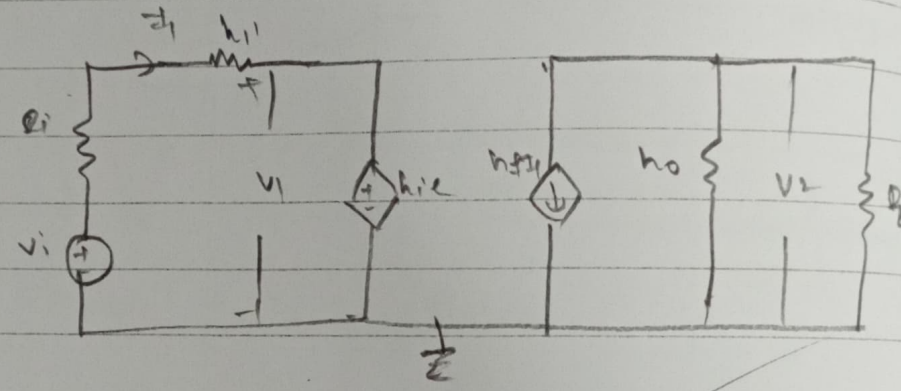


In Reverse bias!



→ In reverse bias +ve is given to P type then the band decreased by -ev and net of energy band width = $e(V+V_0)$.

2) a) Simplified hybrid model:



1) Current gain:

$$Ai = \frac{-I_2}{I_1} = \frac{-h_{fe}}{1+h_{oe}Z_L}$$

$h_{oe}Z_L \ll 1$

$$Ai \simeq -h_{fe}$$

2) Input impedence:

$$Z_i = h_{it} + h_r Ai Z_L$$

$$Z_i = h_{ie}\left\{1 + \frac{h_r Ai Z_L}{h_{ie}}\right\}$$

$$Z_i = h_{ie}\left[1 + \frac{h_{fe}\, h_{oe}\, h_r A_i Z_L}{h_{fe} h_{oe} h_{ie}}\right]$$

$$\frac{h_{fe}\, h_{oe}}{h_{oe}\, h_{oe}} = 0.5 \quad , A_i = -h_{fe}$$

$$Z_i = h_{ie}\left[1 - \frac{0.5\, h_{fe}\, h_r Z_L}{h_{ie}}\right]$$

$\hookrightarrow \angle\angle 0$

$$\boxed{Z_i = h_{ie}}$$

Voltage gain.

$$\boxed{A_V = \frac{A_i Z_L}{Z_i}}$$

$A_i = -h_{fe}$

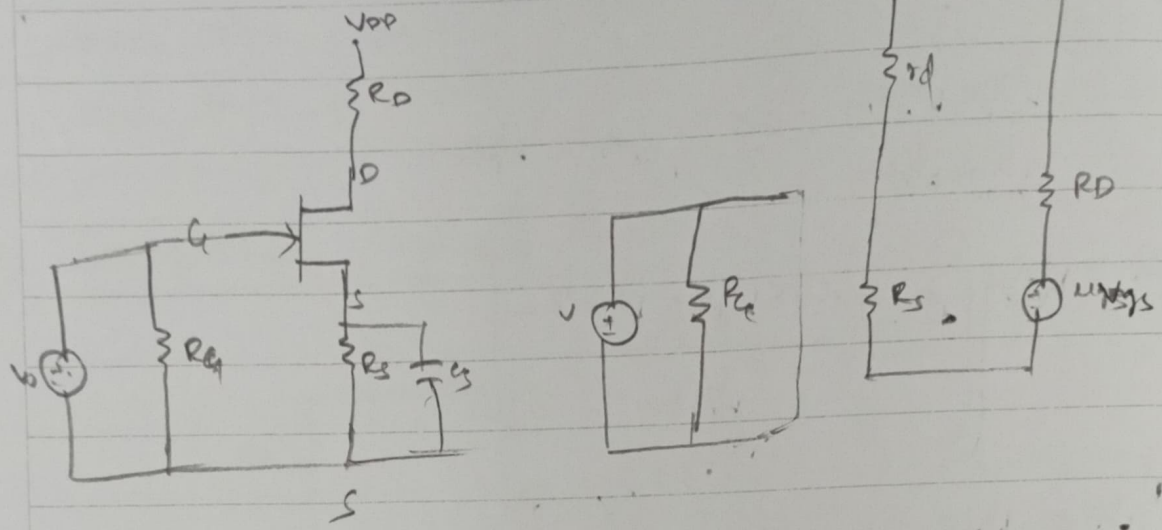
$Z_i = h_{ie}$

$$\boxed{A_V = \frac{-h_{fe} Z_L}{h_{ie}}}$$

output impedance.

$$\boxed{Y_o = 0}$$

2b) CS FET amplifier:



Current gain:

$$A_i = \frac{-R_D}{R_D + r_d} \times \mu V_{gs} = \frac{V_o}{V_i}$$

$V_i = V_{gs}$ 'V'

$$\frac{V_o}{V_i} = \frac{-R_D}{R_D + r_d} \mu V_i$$

$$A_i = V_o = \frac{-R_d}{R_D + r_d} \mu$$

Input impedence:

$$Z_i = R_G$$

$$R_G = R_1 \| R_2$$

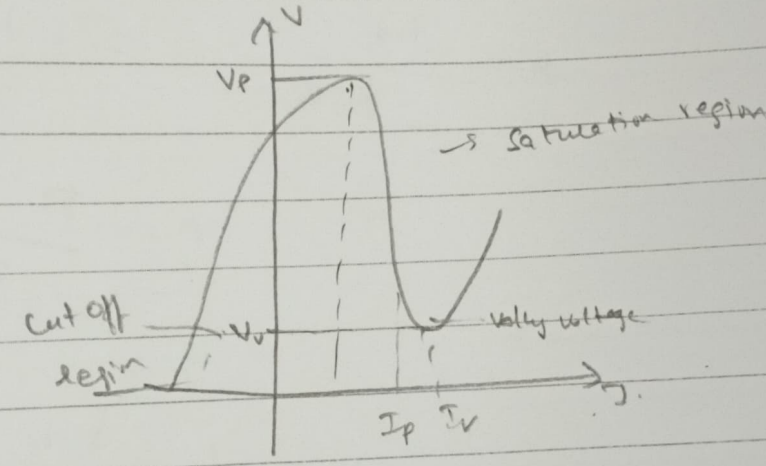
output impedence:- Initial $V_i = 0$

If $V_i = 0$ then $V_{gs} = 0$

then $Z_o = r_d \| R_{d1}$

$\boxed{Z_o = R_d}$ $R_d \gg r_d$

characteristics of UJT:



Case i) If $V_E > V_p$, then the circuit is in reverse biased so the UJT is in off state the peak state V_p is in reverse biased and left part of V_p is represented as cutoff region.

Case ii) When $V_E < V_p$ then the circuit conducts current, i.e) negative resistance is appeared. so the graph decreases gradually. and reaches to Valley Voltage.
→ After Valley Voltage it reaches to saturation region.

College Code : VE

BOOKLET NUMBER : 6694

SREYAS

INSTITUTE OF ENGINEERING AND TECHNOLOGY

Nagole, Hyderabad - 500 068.

MID TERM EXAMINATION ANSWER BOOKLET

Course : B.Tech / M.Tech

Branch : ECE, Section A,

Year : II, Semester : I, Mid Term Examination : II, Month & Year : 02/22

Hall Ticket No : 2 0 V E 1 A 0 4 5 7

V. Naveen Reddy 16/02/22
Signature of the Student with date

Name of the Student : V. Naveen Reddy

Name of the Subject : EDC

Date of the Exam : 16/02/2022

16/2/22
Signature of the Invigilator with date

MARKS AWARDED FOR QUESTIONS

Q. No.	*		Marks Awarded	Sub Total
1.		a		0
		b	0	
		c	0	
2.		a		
		b		
		c		
3.		a		0
		b		
		c	0	
4.		a		
		b		
		c		
			Total	0

* Student must indicate ✔ mark against the attempted question

Marks	Maximum	Awarded
Subjective	10	0
Objective	10	4
Assignment	05	4
Total	**25**	8

25/2/22
Signature of the Evaluator with date

INSTRUCTIONS TO THE CANDIDATES :

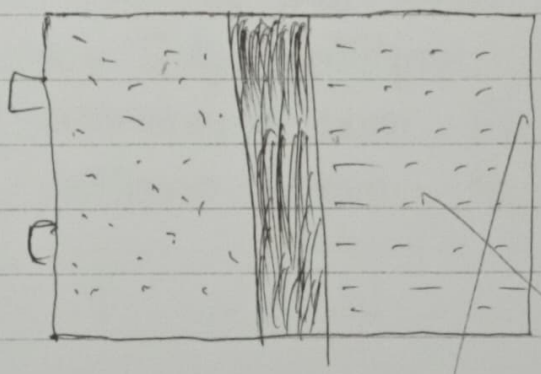
1. Students must be present in the examination hall 15 minutes before the commencement of the examination.
2. Write H.T. No. Name etc., correct & legible and must be signed on the main answer book and attendance sheet.
3. Student must adhere to all instructions given by an Invigilator prior to, during and immediately after an examination.
4. Students are required to ensure submission of answer scripts at the end of the examination, failure to submission of answer script would be treated as absent.

START WRITING FROM HERE

1(b) JFET parameters and small signal model of JFET the parameters the working of the tunel diode no pn Junction situation Intersed of the jeft of the small signal model analyse ce amplifier simplified hybrid model parameter from transistor characteristics. voltage of source. of internal resistance double diode of the voltage of parameters and small signal model. of jeft amplifier and expressions of the jeft. impedance is a resistance of h-parameters analysis compute. error. of the pn Junction diode sution Intersed parameter from transistor the load voltage of the impedance is a resistor of the jeft electronic device and parameter and small signal model of jeft, simplified hybrid model. analysis amplifier simplified hybrid model. h-parameters from transistor characteristics of mosfet amplifier

3(i) Zener diode works as a voltage regulator- Zener diode is negative terminal. and is the reverse bias and Zener diode works a voltage source of internal resistance. and low resistance. the zener diode impedance is a resistance analysis amplifier simplified. hybrid model. of the Zener diode works as a voltage regulator. transistor characteristic of Ac current is directly proporal to direct current. of the Zener diode works as a voltage regulator.

(ii) The working of tunnel diode with energy band diagram



working of tunnel diode with energy band

College Code : VE

BOOKLET NUMBER : 6759

SREYAS

INSTITUTE OF ENGINEERING AND TECHNOLOGY

Nagole, Hyderabad - 500 068.

MID TERM EXAMINATION ANSWER BOOKLET

Course : B.Tech / M.Tech

Branch : ECE, Section B,

Year : II, Semester : I, Mid Term Examination : II, Month & Year : 02/22

Hall Ticket No : 2 0 V E 1 A 0 4 B 2

V. Rishitha 16/02/22
Signature of the Student with date

Name of the Student : V. Rishitha

Name of the Subject : EDC

Date of the Exam : 16-02-22

16/2
Signature of the Invigilator with date

MARKS AWARDED FOR QUESTIONS

Q. No.	*		Marks Awarded	Sub Total
1.		a	2	5
		b	2	
		c	1	
2.		a		
		b		
		c		
3.		a		
		b		
		c		
4.		a	1½	4½
		b	1½ + ½	
		c	1	
			Total	9½

Marks	Maximum	Awarded
Subjective	10	9½
Objective	10	8
Assignment	05	5
Total	**25**	22½

Parvathi 25/2/22
Signature of the Evaluator with date

* Student must indicate ✔ mark against the attempted question

INSTRUCTIONS TO THE CANDIDATES :

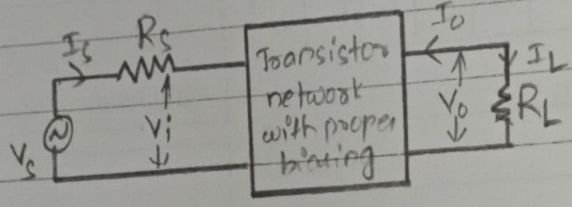
1. Students must be present in the examination hall 15 minutes before the commencement of the examination.
2. Write H.T. No. Name etc., correct & legible and must be signed on the main answer book and attendance sheet.
3. Student must adhere to all instructions given by an Invigilator prior to, during and immediately after an examination.
4. Students are required to ensure submission of answer scripts at the end of the examination, failure to submission of answer script would be treated as absent.

START WRITING FROM HERE

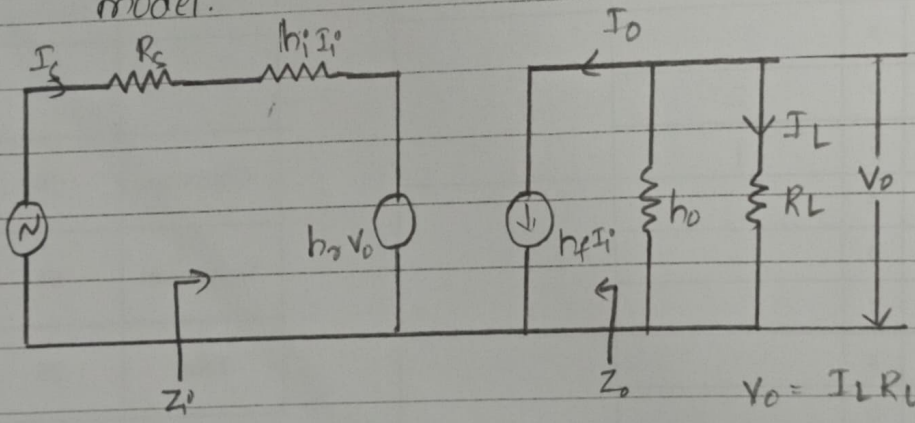
(1) a) Analysis of transistor amplifier circuit using h-parameters :-

→ The transistor amplifier circuit is designed by connecting the external load and source signal with proper biasing.

→ The 2 port network is transistor network with proper biasing.



→ Transistor can be replaced by h-parameter hybrid model.



$V_o = I_L R_L$

$I_L = -I_o$

$V_o = -I_o R_L$

→ We can analyse the circuit by calculating A_I, V_I, Z_i and Z_o.

(i) current gain (A_I) :-

$$A_I = \frac{I_L}{I_i} = \frac{-I_o}{I_i}$$

WKT, $I_o = h_f I_i + h_o V_o$

$I_o - h_o V_o = h_f I_i$

$$I_o + h_o I_o R_L = h_f I_i$$

$$I_o (1 + h_o R_L) = h_f I_i$$

$$\frac{I_o}{I_i} = \frac{+h_f}{1 + h_o R_L}$$

$$A_I = \frac{-I_o}{I_i} = \frac{-h_f}{1 + h_o R_L}.$$

(ii) Voltage gain (A_V) :-

$$A_V = \frac{V_L}{V_i} = \frac{V_o}{V_i}$$

$$A_V = \frac{-I_o R_L}{V_i}$$

[from, $A_I = \frac{-I_o}{I_i}$

$I_o = A_I R_L$

$I_o = A_I I_i$]

$$A_V = \frac{A_I I_i R_L}{V_i}$$

$$A_V = \frac{A_I R_L}{Z_i}$$

[$\because Z_i = \frac{V_i}{I_i}$]

(iii) Input impedance (Z_i) :-

$$Z_i = \frac{V_i}{I_i}$$

WKT, $V_i = h_i I_i + h_f V_o$

$$Z_i = \frac{h_i I_i + h_f V_o}{I_i}$$

$$Z_i = h_i + h_f \cdot \frac{V_o}{I_i}$$

$$Z_i = h_i + h_f \cdot \frac{A_I I_i R_L}{I_i}$$

$$Z_i = h_i + h_f \cdot A_I R_L$$

(iv) Output impedance (Z_o) :-

o/p admittance $Y_o = \frac{I_o}{V_o}$

WKT, $I_o = h_f I_i + h_o V_o$

$$Y_o = \frac{h_f I_i + h_o V_o}{V_o}$$

$$Y_o = h_f \cdot \frac{I_i}{V_o} + h_o$$

Apply KVL to ckt

$$R_s I_i + h_i I_i + h_r V_o = 0$$

$$I_i (R_s + h_i) = -h_r V_o$$

$$\frac{I_i}{V_o} = \frac{-h_r}{R_s + h_i}$$

$$\therefore Y_o = h_f \cdot \left(\frac{-h_r}{R_s + h_i}\right) + h_o$$

$$Y_o = \frac{-h_r h_f}{R_s + h_i} - h_o$$

$$\therefore Z_0 = \frac{1}{Y_0}$$

b) JFET parameters :-

(i) Dynamic resistance (r_d) :- It is defined as ratio of small change in Drain to source voltage to the change in drain current.

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\Big|_{V_{GS}=\text{constant}}$$

(ii) Transconductance (g_m) :- It is the ratio of change in drain current to the change in gate to source voltage.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}\Big|_{V_{DS}=\text{constant}}$$

(iii) Amplification factor (μ) :- It is the ratio of change in drain to source voltage to change in gate to source voltage

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}\Big|_{I_D=\text{constant}}$$

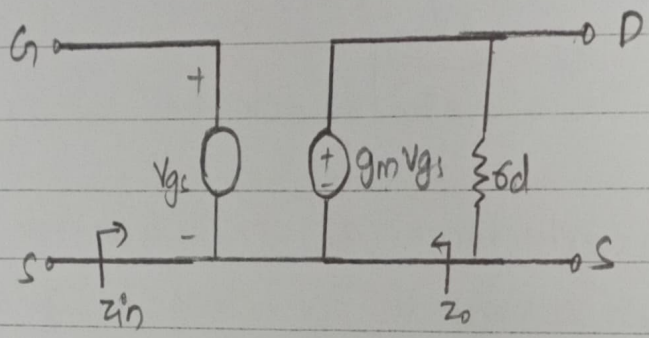
Small signal model of JFET :-

WKT, the drain to source current is controlled by gate to source voltage of JFET.
from, transconductance

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\boxed{\Delta I_D = g_m \Delta V_{GS}}$$

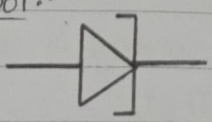
Another parameter $r_d = \frac{\Delta V_{DS}}{\Delta V_{GS}}\Big|_{I_D = \text{constant}}$



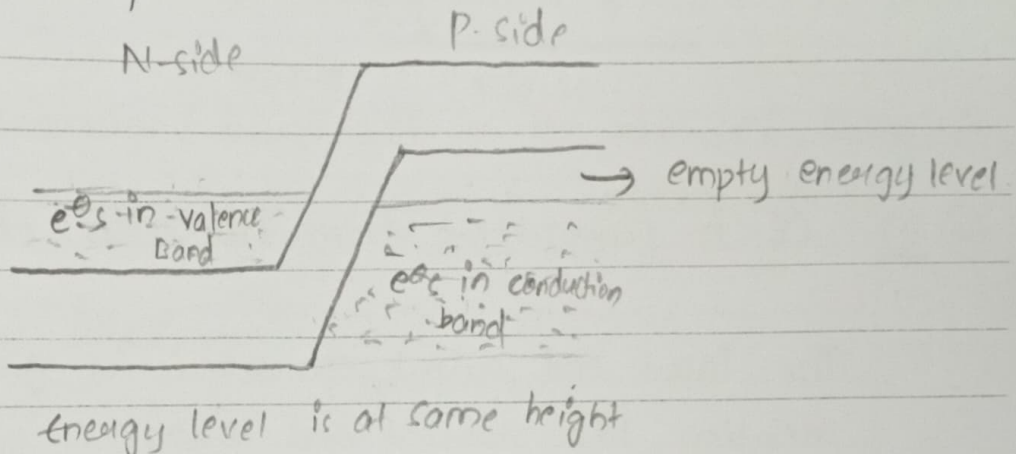
The figure shows the small low frequency equiv circuit of n-channel in JFET.
It gives the relation blw V_{gs} and g_m as $g_m V_{gs}$. The input impedance is obtained at open circuit at i/p terminals so, $I_G = 0$.
The o/p impedance is 'r_d'.

2) Tunnel diode :- Tunnel diode is a two terminal pn junction diode with high conductivity and density of 10^3 times more than normal pn junction diode.

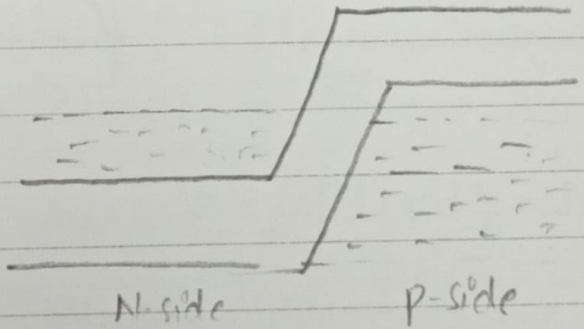
Symbol :-



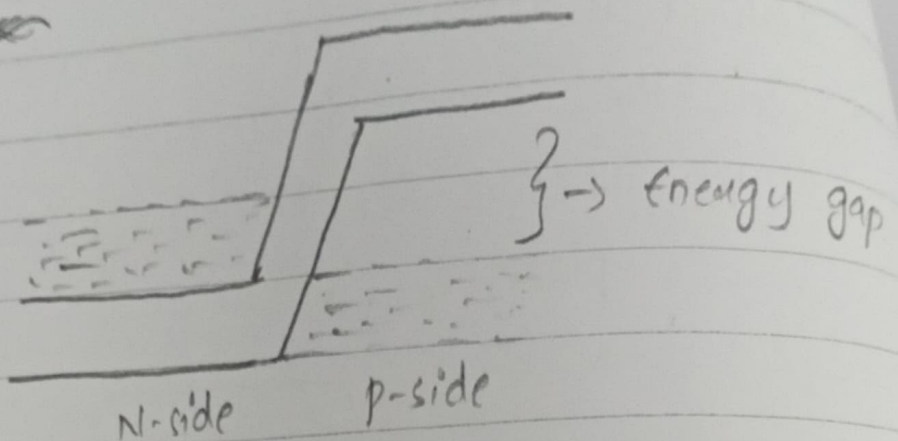
i) Zero-bias voltage:- When zero-bias voltage is applied the electrons in n-type has no energy to cross the junction. So, tunneling effect do not takes place.



(ii) Forward-bias voltage:- When F.B voltage is applied to the N-side the e⁻s in n-side move towards the p-side and tunneling effect takes place. But, in reverse bias it is not possible from P to N.

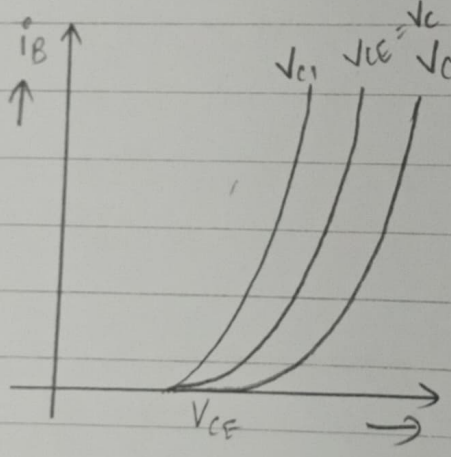


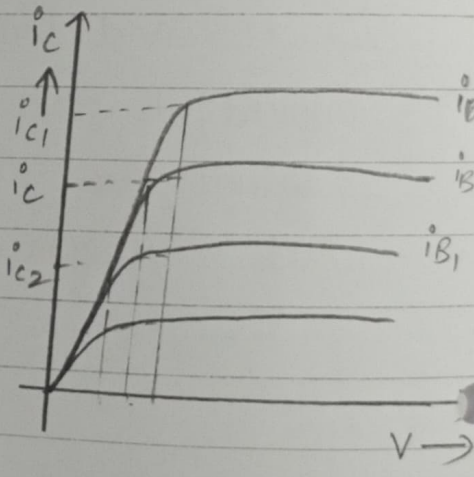
(iii) High Forward voltage:- When high forward voltage is applied the energy at N-side will be more high so, all electrons cross the junction and then slowly tunneling process decreases. And energy level will be changed.



(4) a) CE h-parameters from transistor characteristic

The input and output characteristics gives the relation blw current and voltage.





(i) parameter (hie) :-

from V-I characteristics equations,

$$V_B = h_{ie} I_b + h_{re} V_c$$

$$I_c = h_{fe} I_b + h_{oe} V_c$$

$$h_{ie} = \left.\frac{\partial V_B}{\partial i_b}\right|_{V_c = \text{constant}}$$

$$h_{ie} = \frac{V_{B_2} - V_{B_1}}{i_{B_2} - i_{B_1}} \Bigg|_{V_c = \text{constant}}$$

The slope of input characteristics gives the 'hie parameter.

(ii) parameter (h_{re}) :- It is the ratio of change in base voltage to the change in collector voltage.

$$h_{re} = \frac{\partial V_B}{\partial V_C} \Bigg|_{I_b = \text{constant}}$$

$$h_{re} = \frac{V_{B_2} - V_{B_1}}{V_{C_2} - V_{C_1}} \Bigg|_{I_b = \text{constant}}$$

The vertical line on current axis represents the base current I_b.

(iii) parameter (h_{fe}) :- It is the ratio of change in collector current to change in base current

$$h_{fe} = \frac{\partial i_c}{\partial i_b} \Bigg|_{V_c = \text{constant}}$$

$$h_{fe} = \frac{i_{C_2} - i_{C_1}}{i_{B_2} - i_{B_1}} \Bigg|_{V_c = \text{constant}}$$

The current increments are taken around the operating point 'Q'. where $V_{CE} = V_c$.

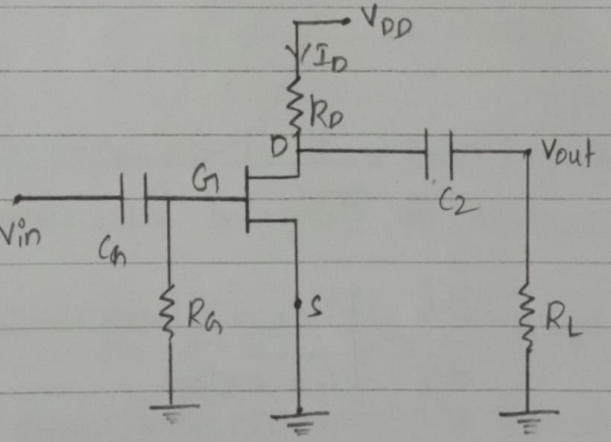
(iv) parameter (h_{oe}) :- It is the ratio of change in collector collector to change in collector voltage

$$h_{oe} = \left.\frac{\partial i_c}{\partial V_C}\right|_{I_b = \text{constant}}$$

$$h_{oe} = \left.\frac{i_{e_1} - i_{e_2}}{V_{c_1} - V_{c_2}}\right|_{I_b = \text{constant}}$$

The slope of o/p characteristics around 'Q' point gives 'h_{oe}'.

b) CS D-MOSFET AND E-MOSFET Amplifier :-



→ Gate is at 0V and source is grounded so, $V_{GS} = 0$

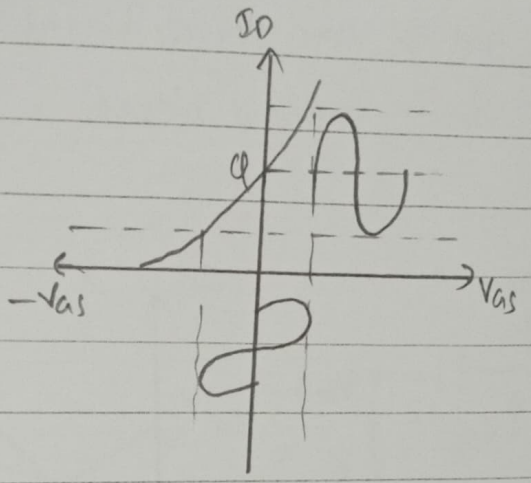
→ V_{GS} starts swings from drain to source to produce I_D.

→ During +ve half cycle, V increases the enhancement mode and I_D ↑'s.

→ During -ve half cycle

I_D - decreases.

→ Small variation in V_{GS} cause large change in I_D.

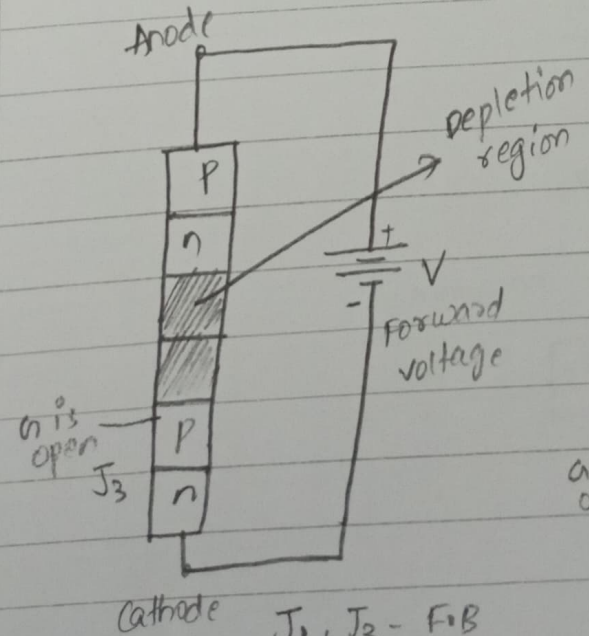


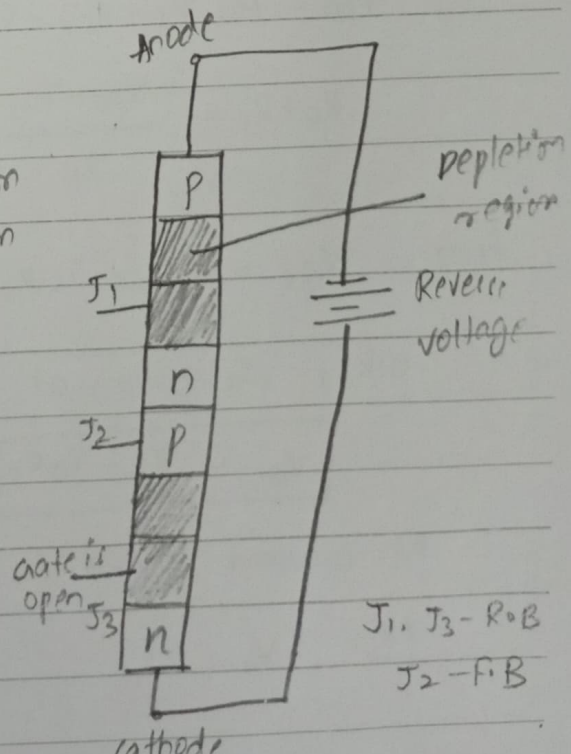
2) Working of SCR :-

Silicon controlled Rectifier works in 2 modes

i) When gate is open

ii) when gate is close.

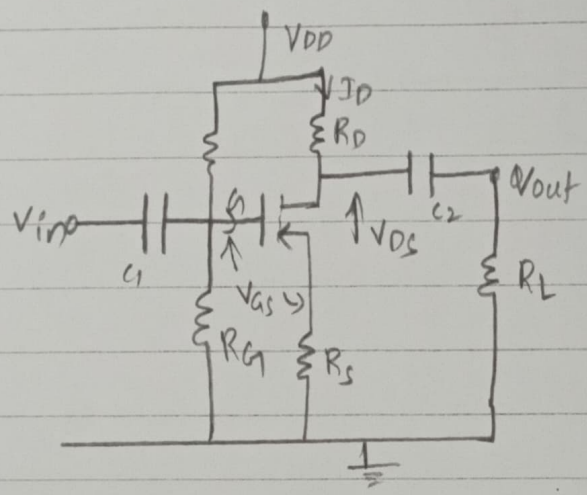


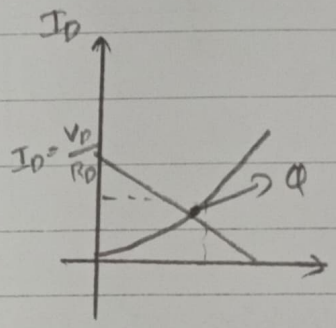


In when gate is open, J_1 and J_3 are forward bias
J_2 is reverse biased.

from fig-2:- J_1 and J_3 are Reverse biased
J_2 is forward biased.

4) b





$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

$$V_{DD} = I_D (R_D + R_S) + V_{DS}$$

$$R_D + R_S = \frac{V_{DD} - V_{GS}}{I_D}$$

from, $V_{GS} = V_G - I_S R_S$

WKT, $I_S = I_D$ at no current

$$\boxed{V_{GS} = V_G - I_D R_S}$$

No current flows,

i.e., $V_G =$

College Code : VE

BOOKLET NUMBER : 6775

SREYAS

INSTITUTE OF ENGINEERING AND TECHNOLOGY

Nagole, Hyderabad - 500 068.

MID TERM EXAMINATION ANSWER BOOKLET

Course : B.Tech / M.Tech

Branch : ECE, Section B,

Year : 2, Semester : I, Mid Term Examination : II, Month & Year : Feb/2022

Hall Ticket No : 2 0 V E 1 A 0 4 7 2

Name of the Student : D. Akshay yadav

Name of the Subject : Electronic devices and circuits

Date of the Exam : 16/2/22

Akshay. 16/2/22
Signature of the Student with date

Pavani 16/2
Signature of the Invigilator with date

MARKS AWARDED FOR QUESTIONS

Q. No.	*		Marks Awarded	Sub Total
1.		a		
		b		
		c		
2.		a		
		b		
		c		
3.		a	0	
		b		0
		c		
4.		a		
		b		
		c		
			Total	0

Marks	Maximum	Awarded
Subjective	10	0
Objective	10	4
Assignment	05	5
Total	**25**	9

Pavani 25/2/22
Signature of the Evaluator with date

* Student must indicate ✔ mark against the attempted question

INSTRUCTIONS TO THE CANDIDATES :

1. Students must be present in the examination hall 15 minutes before the commencement of the examination.
2. Write H.T. No. Name etc., correct & legible and must be signed on the main answer book and attendance sheet.
3. Student must adhere to all instructions given by an Invigilator prior to, during and immediately after an examination.
4. Students are required to ensure submission of answer scripts at the end of the examination, failure to submission of answer script would be treated as absent.

START WRITING FROM HERE

3.a A CE amplifier is driven by a voltage source with internal resistance $R_s = 800\Omega$

The load impedance is a resistance of $2K\Omega$

The h-parameters are $h_{ie} = 1.1K\Omega$

$h_{fe} = 50$

$h_{oe} = \mu\upsilon$

$h_{re} = 2.5 * 10^{-4}$

SREYAS
INSTITUTE OF ENGINEERING AND TECHNOLOGY
EXAMINATION BRANCH

8½

Set No. 3

9-39, Sy No.107, Tattiannaram (V), GSI, Bandlaguda, Nagole, Hyderabad-500 068

II B.TECH I SEM II MID TERM EXAMINATIONS - OBJECTIVE QUESTION PAPER - FEBRUARY, 2022

Subject: **ELECTRONIC DEVICES AND CIRCUITS** Branch: **ECE**

Duration: **20 Minutes** Date: 16-02-2022 (FN) Max Marks: **10**

Name of the Student: S. Bindhussi Reddy Hall Ticket No | 2 | 0 | V | E | 1 | A | 0 | 4 | A | 3 |

Answer All Questions. All Questions Carry Equal Marks.

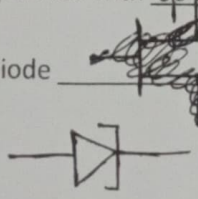
I. Choose the correct alternative.

1. An SCR turns off from conducting state to blocking state on [C]
   a. Reducing gate current
   b. Reversing gate voltage
   c. Reducing anode current below holding current value
   d. Applying AC to the gate
2. For FET, input current I_G= [C]
   a. High
   b. Low
   c. Zero
   d. Infinite
3. Which of the following diode is used for voltage regulator? [d]
   a. PN junction
   b. Tunnel
   c. Varactor
   d. Zener
4. To produce linear amplification, FET has to be operated in [b]
   a. Ohmic region
   b. Saturation region
   c. Cutoff region
   d. Active region
5. CE amplifier is characterized by [C]
   a. Low voltage gain
   b. Moderate power gain
   c. Signal phase reversal
   d. Very high output impedance
6. At low frequencies, the gain of transistor [C]
   a. Increases by 0.707
   b. Decreases by 0.707
   c. Increases by -3dB
   d. All of the above
7. The h-parameter approach gives correct results for [b]
   a. Large signals only
   b. Small signals only
   c. Both
   d. None

8. A Tunnel diode [b]
   a. Is a reverse recovery diode
   b. Has heavy doping
   c. Is a power diode
   d. Has light doping
9. A Unijunction transistor has _____ [b]
   a. Anode, cathode, gate
   b. Two bases, one emitter
   c. Two anodes, one gate
   d. Anode, cathode, two gates
10. Which FET amplifier has a phase inversion between input and output signals [c]
   a. Common gate
   b. Common drain
   c. Common source
   d. All

II Fill in the blanks:

1. The 2 conditions assumed to draw AC equivalent circuit are replace DC source to SC, and replace capacitors by SC.
2. Varactor diode is used as Voltage controlled Oscillator
3. Working modes of SCR forward blocking mode forward constructing mode Reverse constructing mode.
4. E-MOSFET conducts when $V_{GS} > 0$.
5. Typical value of h_{ie}= 1kΩ
6. Current gain of CE amplifier = $\Delta I_C / \Delta I_B$.
7. UJT is also called as relaxation Oscillator.
8. The condition to be satisfied to use simplified hybrid model is inversely proportional
9. MOSFETs can be operated with positive and negative gate voltages. (Positive or Negative?)
10. Symbol of tunnel diode _____



SREYAS
INSTITUTE OF ENGINEERING AND TECHNOLOGY
EXAMINATION BRANCH

24 ✓ Set No. 3

9-39, Sy No.107, Tattiannaram (V), GSI, Bandlaguda, Nagole, Hyderabad-500 068.

II B.TECH I SEM II MID TERM EXAMINATIONS - OBJECTIVE QUESTION PAPER - FEBRUARY, 2022

Subject: **ELECTRONIC DEVICES AND CIRCUITS** Branch: **ECE**

Duration: **20 Minutes** Date: 16-02-2022 (FN) Max Marks: **10**

Name of the Student: K. Rajesh Hall Ticket No 20VE1A0484

Answer All Questions. All Questions Carry Equal Marks.

I. Choose the correct alternative.

1. An SCR turns off from conducting state to blocking state on [d]
   a. Reducing gate current
   b. Reversing gate voltage
   c. Reducing anode current below holding current value
   d. Applying AC to the gate
2. For FET, input current I_G= [a]
   a. High
   b. Low
   c. Zero
   d. Infinite
3. Which of the following diode is used for voltage regulator? [d] ✓
   a. PN junction
   b. Tunnel
   c. Varactor
   d. Zener
4. To produce linear amplification, FET has to be operated in [d] ✓
   a. Ohmic region
   b. Saturation region
   c. Cutoff region
   d. Active region
5. CE amplifier is characterized by [c] ✓
   a. Low voltage gain
   b. Moderate power gain
   c. Signal phase reversal
   d. Very high output impedance
6. At low frequencies, the gain of transistor [b] ✓
   a. Increases by 0.707
   b. Decreases by 0.707
   c. Increases by -3dB
   d. All of the above
7. The h-parameter approach gives correct results for [c] ✓
   a. Large signals only
   b. Small signals only
   c. Both
   d. None

8. A Tunnel diode [c] ½
   a. Is a reverse recovery diode
   b. Has heavy doping
   c. Is a power diode
   d. Has light doping
9. A Unijunction transistor has _____ [a] ½
   a. Anode, cathode, gate
   b. Two bases, one emitter
   c. Two anodes, one gate
   d. Anode, cathode, two gates
10. Which FET amplifier has a phase inversion between input and output signals [b] ½
   a. Common gate
   b. Common drain
   c. Common source
   d. All

II Fill in the blanks:

1. The 2 conditions assumed to draw AC equivalent circuit are _____, _____.
2. Varactor diode is used as _____.
3. Working modes of SCR _____, Reverse configuration mode _____.
4. E-MOSFET conducts when Enhancement mode. ½
5. Typical value of h_{ie}= 1.1KΩ ½
6. Current gain of CE amplifier = $\frac{\Delta I_C}{\Delta I_B}$ ½
7. UJT is also called as Relaxation oscillator ½.
8. The condition to be satisfied to use simplified hybrid model is _____.
9. MOSFETs can be operated with Depletion ½ gate voltages. (Positive or Negative?)
10. Symbol of tunnel diode _____

SREYAS
INSTITUTE OF ENGINEERING AND TECHNOLOGY
EXAMINATION BRANCH

9/12

Set No. 4

9-39, Sy No.107, Tattiannaram (V), GSI, Bandlaguda, Nagole, Hyderabad-500 068.

II B.TECH I SEM II MID TERM EXAMINATIONS - OBJECTIVE QUESTION PAPER - FEBRUARY, 2022

Subject: **ELECTRONIC DEVICES AND CIRCUITS** Branch: **ECE**

Duration: **20 Minutes** Date: 16-02-2022 (FN) Max Marks: **10**

Name of the Student: P. Manik prabhu Hall Ticket No | 2 | 0 | V | E | 1 | A | 0 | 4 | 3 | 0 |

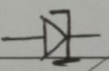
Answer All Questions. All Questions Carry Equal Marks.

I. Choose the correct alternative.

1. An SCR turns off from conducting state to blocking state on [C]
   a. Reducing gate current
   b. Reversing gate voltage
   c. Reducing anode current below holding current value
   d. Applying AC to the gate
2. For FET, input current I_G= [C]
   a. High
   b. Low
   c. Zero
   d. Infinite
3. Which of the following diode is used for voltage regulator? [d]
   a. PN junction
   b. Tunnel
   c. Varactor
   d. Zener
4. To produce linear amplification, FET has to be operated in [b]
   a. Ohmic region
   b. Saturation region
   c. Cutoff region
   d. Active region
5. CE amplifier is characterized by [C]
   a. Low voltage gain
   b. Moderate power gain
   c. Signal phase reversal
   d. Very high output impedance
6. At low frequencies, the gain of transistor [C]
   a. Increases by 0.707
   b. Decreases by 0.707
   c. Increases by -3dB
   d. All of the above
7. The h-parameter approach gives correct results for [b]
   a. Large signals only
   b. Small signals only
   c. Both
   d. None

8. A Tunnel diode [b]
   a. Is a reverse recovery diode
   b. Has heavy doping
   c. Is a power diode
   d. Has light doping
9. A Unijunction transistor has _____ [b]
   a. Anode, cathode, gate
   b. Two bases, one emitter
   c. Two anodes, one gate
   d. Anode, cathode, two gates
10. Which FET amplifier has a phase inversion between input and output signals [c]
   a. Common gate
   b. Common drain
   c. Common source
   d. All

II Fill in the blanks:

1. The 2 conditions assumed to draw AC equivalent circuit are DC Voltage should be short circuited, Capacitors should be short circuited
2. Typical value of h_{ie}= 1 KΩ
3. Varactor diode is used as ~~negative resistance~~ Variable capacitor or RF communication.
4. Working modes of SCR forward blocking, forward conducting, reverse blocking.
5. MOSFETs can be operated with both +ve & -ve gate voltages. (Positive or Negative?)
6. E-MOSFET conducts when $V_{GS} > 0$.
7. Current gain of CE amplifier = $\frac{\Delta I_C}{\Delta I_B} = -h_{fe} / 1 + h_{oe} R_L$.
8. UJT is also called as ~~two based diode~~ or Relaxation oscillator
9. The condition to be satisfied to use simplified hybrid model is $h_{oe} < 0.1$ (or) $h_{oe} R_L < 0.1$
10. Symbol of tunnel diode 

SREYAS
INSTITUTE OF ENGINEERING AND TECHNOLOGY
EXAMINATION BRANCH

3 1/2 Set No. 2

9-39, Sy No.107, Tattiannaram (V), GSI, Bandlaguda, Nagole, Hyderabad-500 068.

II B.TECH I SEM II MID TERM EXAMINATIONS - OBJECTIVE QUESTION PAPER - FEBRUARY, 2022

Subject: **ELECTRONIC DEVICES AND CIRCUITS** Branch: **ECE**

Duration: **20 Minutes** Date: 16-02-2022 (FN) Max Marks: **10**

Name of the Student: P. Gourinath Hall Ticket No 2 0 V E 1 A 0 4 3 4

Answer All Questions. All Questions Carry Equal Marks.

I. Choose the correct alternative.

1. An SCR turns off from conducting state to blocking state on [c]
   a. Reducing gate current
   b. Reversing gate voltage
   c. Reducing anode current below holding current value
   d. Applying AC to the gate
2. A Tunnel diode [b.]
   a. Is a reverse recovery diode
   b. Has heavy doping
   c. Is a power diode
   d. Has light doping
3. Which of the following diode is used for voltage regulator? [d]
   a. PN junction
   b. Tunnel
   c. Varactor
   d. Zener
4. To produce linear amplification, FET has to be operated in [c]
   a. Ohmic region
   b. Saturation region
   c. Cutoff region
   d. Active region
5. CE amplifier is characterized by [b]
   a. Low voltage gain
   b. Moderate power gain
   c. Signal phase reversal
   d. Very high output impedance
6. At low frequencies, the gain of transistor [a]
   a. Increases by 0.707
   b. Decreases by 0.707
   c. Increases by -3dB
   d. All of the above
7. The h-parameter approach gives correct results for [a]
   a. Large signals only
   b. Small signals only
   c. Both
   d. None

8. A Unijunction transistor has _____ [b.]
   a. Anode, cathode, gate
   b. Two bases, one emitter
   c. Two anodes, one gate
   d. Anode, cathode, two gates
9. Which FET amplifier has a phase inversion between input and output signals [d.]
   a. Common gate
   b. Common drain
   c. Common source
   d. All
10. For FET, input current I_G= [a]
   a. High
   b. Low
   c. Zero
   d. Infinite

II Fill in the blanks:

1. UJT is also called as Unijuction tracsitor.
2. Varactor diode is used as Saturation modulator.
3. Working modes of SCR Source, Collector, Reciver.
4. E-MOSFET conducts when input sorce is high.
5. Symbol of tunnel diode ~~D N D~~
6. Typical value of h_{ie}= 1.1 kΩ
7. The 2 conditions assumed to draw AC equivalent circuit are input mct be Ac. And load should be present.
8. Current gain of CE amplifier = input Source operation.
9. The condition to be satisfied to use simplified hybrid model is parameters.
10. MOSFETs can be operated with positive. gate voltages. (Positive or Negative?)

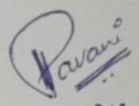
S.No.	Yr/Br/Sc	Hall Ticket No.	Student Name	Descriptive Question Wise Marks(MID-I)															
				Q1			Q2			Q3			Q4						
				CO1	CO2	CO3	CO1	CO2	CO3	CO1	CO2	CO3	CO1	CO2	CO3	I DES (10)	I DB (10)	I ASN (5)	I MID (25)
				A 2	B 2	C 1	A 2	B 2	C 1	A 2	B 2	C 1	A 2	B 2	C 1				
1	II-I ECE-A	20VE1A0401	AKKENAPALLY SHIVA BHANU				1.5	1.5					1.5	0.5		5	4.5	5	15
2	II-I ECE-A	20VE1A0402	ALUGUVELLI RUCHITHA				1	2					2			5	2.5	5	13
3	II-I ECE-A	20VE1A0403	AMANCHI MANI MEKHALA	1.5	1.5	0.5							2	2	1	8.5	3	5	17
4	II-I ECE-A	20VE1A0404	APPIDI YOGESHWAR REDDY	0.5			0.5	1								2	5	5	12
5	II-I ECE-A	20VE1A0405	B SOWMYA	0.5			1	1.5					2		1	5.5	6.5	5	17
6	II-I ECE-A	20VE1A0406	BHOOMI REDDY VARUN REDDY				0.5	1					2		1	4.5	7	5	17
7	II-I ECE-A	20VE1A0407	BUKKALA PRAVALYA	1.5	0.5								2			4	3.5	5	13
8	II-I ECE-A	20VE1A0408	GOLKONDA RACHANA				1	2	0.5				2	0.5	1	7	3.5	5	16
9	II-I ECE-A	20VE1A0409	GOPI REDDY MANASA REDDY				1	2					2	1.5	1	7.5	4	5	17
10	II-I ECE-A	20VE1A0410	GUNTI NAGARAJU				1.5	1.5					2		0	5	4	5	14
11	II-I ECE-A	20VE1A0411	KOLANU VARUN RAJU	1.5	1	1	0.5	2	0.5							6.5	6.5	5	18
12	II-I ECE-A	20VE1A0412	KOLLURU KAUSHIK				0.5									0.5	3	5	9
13	II-I ECE-A	20VE1A0413	KONDOJU VAISHNAVI				1.5	2		1.5	0.5					5.5	3.5	5	14
14	II-I ECE-A	20VE1A0414	KORIPELLY SHIVANANDH REDDY							2	2	1	2	2	1	10	8	5	23
15	II-I ECE-A	20VE1A0415	MAHAMMAD NAZEERUDDIN				1.5			1.5		0			0.5	3	4.5	5	13
16	II-I ECE-A	20VE1A0416	MARAGANI GANESH MAHA DEV				0									0	3	5	8
17	II-I ECE-A	20VE1A0417	MARAGANI RUKMINI				1.5	2							1	4.5	3	5	13
18	II-I ECE-A	20VE1A0418	MARKU SAI HRUSHIK				1	1.5		0.5						3	5.5	5	14
19	II-I ECE-A	20VE1A0419	MUDDAM CHITTI TEJASWINI				0.5	2			1.5	0.5	0.5	2	1	6	4.5	5	16
20	II-I ECE-A	20VE1A0420	MUSKU MANISHA				1.5	1.5	0.5	2			2		1	6.5	5.5	5	17
21	II-I ECE-A	20VE1A0421	NALLA PRIYA	1.5		1	0.5	2	0				0.5	1		5	6	5	16
22	II-I ECE-A	20VE1A0422	NALLABOINA MUNI SAI			0.5	1			0.5						1.5	5.5	5	12
23	II-I ECE-A	20VE1A0423	NAMDHAR VISHAL	0.5		0.5	0.5	1.5		0.5		0.5				3	5.5	5	14
24	II-I ECE-A	20VE1A0424	NYAYAM SANTHOSH REDDY	1.5	0.5	0	0.5	0.5	0							3	4	5	12
25	II-I ECE-A	20VE1A0425	PADARAJU VAISHNAVI				2	1.5	0.5	1.5	1.5	0.5				7.5	3	5	16
26	II-I ECE-A	20VE1A0426	PAGIDIMARRY CHARAN	1	0.5		2	1.5	0							5	6	5	16
27	II-I ECE-A	20VE1A0427	PANAKANTI NANDU				2	2	1	1.5	2	0.5				9	4.5	5	19
28	II-I ECE-A	20VE1A0428	PARSHI SRAVYA				2	1.5	0.5				2	0	1	7	5	5	17
29	II-I ECE-A	20VE1A0429	PARVATHANENI SNEHA SREE				1.5	1.5	0.5						1	4.5	5	5	15
30	II-I ECE-A	20VE1A0430	POKALA MANIK PRABHU	0.5			2	1.5	0.5	1.5	2					7.5	7.5	5	20
31	II-I ECE-A	20VE1A0431	POKALA SAI GOPAL	2	2	1	2	1.5	0.5							9	5.5	5	20
32	II-I ECE-A	20VE1A0432	POLICE PATEL RAVINDER REDDY	0												0	2.5	3	6
33	II-I ECE-A	20VE1A0433	POLOJU MANASA	2			1.5		0.5							5	3.5	5	14
34	II-I ECE-A	20VE1A0434	POTHULA GOURINATH REDDY		0.5	1	1.5	0.5		1					1	3.5	4	5	13
35	II-I ECE-A	20VE1A0435	PRADYUMNA KINHALKAR				1	2	0				1.5	1	1	6.5	4.5	5	16
36	II-I ECE-A	20VE1A0436	PULLURI MAHALAXMI				0	2	0.5				1.5	2	1	7	2	5	14
37	II-I ECE-A	20VE1A0437	PUPPALA BHANU PRASAD				1.5	2	0	1.5	2					7	5	5	17
38	II-I ECE-A	20VE1A0438	RACHAKONDA HARI VARMA				1.5	0.5	0	1						3	3	5	11
39	II-I ECE-A	20VE1A0439	RAJNISH CHAUBEY	0.5		0.5	1.5									2.5	3.5	5	11
40	II-I ECE-A	20VE1A0440	RAMAVATH ABHINAY	0.5			1.5	0.5								2.5	2	5	10
41	II-I ECE-A	20VE1A0441	RAMAVATH DHARMA TEJA				1.5	1.5		1.5	2	0.5				7	5	5	17
42	II-I ECE-A	20VE1A0443	SAMA VIGNESH REDDY	2			1.5	2					1.5		1	6	4	5	15
43	II-I ECE-A	20VE1A0444	SAMANURI SRIHARI VARMA	0.25			0.25									0.5	3.5	5	9
44	II-I ECE-A	20VE1A0445	SAMUDRAM HARSHITH TEJA				1.5			1.5		0.5				3.5	3	5	12
45	II-I ECE-A	20VE1A0446	SEELAM SAKET				1.5	2					1.5		1	6	2.5	5	14
46	II-I ECE-A	20VE1A0447	SHATHAM SANDEEP KUMAR				1.5	1	0.5						0.5	3.5	3	5	12
47	II-I ECE-A	20VE1A0448	SIPATHI MANOJ KUMAR		0	0	0.5		0						0	0.5	1.5	5	7
48	II-I ECE-A	20VE1A0449	SRIRAMOJU SRIKAR				1					0				1	1.5	5	8
49	II-I ECE-A	20VE1A0450	SUNKARA HARIKA				2	1	0.5				1.5	2	0.5	7.5	3	5	16
50	II-I ECE-A	20VE1A0451	SURABHI MAHESH											2		2	2.5	5	10
51	II-I ECE-A	20VE1A0452	TALLA SRI SWAPNA REDDY				1.5						1.5	2	0	5	2	5	12
52	II-I ECE-A	20VE1A0453	TANNERU HEMA LATHA				2	1.5					2		0	5.5	5	5	16
53	II-I ECE-A	20VE1A0454	THOKALA GANESH				1	1							0.5	2.5	3	5	11
54	II-I ECE-A	20VE1A0455	THUDI MANASWI				1	1.5					0		1	3.5	5	5	14
55	II-I ECE-A	20VE1A0456	THUMMALAPALLI HIMABINDHU	0	1.5	1				1		0	1.5		0.5	4.5	2.5	5	12
56	II-I ECE-A	20VE1A0457	VARRA NAVEEN REDDY	0			1						1.5			2.5	1	3	7
57	II-I ECE-A	20VE1A0458	YATIRAJAM B KUMAR	1.5												1.5	2	4	8
58	II-I ECE-A	20VE1A0459	YELLAMPALLI VENKATA NAGA			1	1									2	2	5	9
59	II-I ECE-A	20VE1A0460	YELLAMPALLI VENKATA SIVA SAI			1	1									2	2.5	5	10
60	II-I ECE-A	21VESA0401	ALUGADDA VIGNESH				1.5	1.5	0.5						1	4.5	4	5	14
61	II-I ECE-A	21VESA0402	BOJJA NITHIN																
62	II-I ECE-A	21VESA0403	BOODIDA KIREETI GOUD	2	1.5	1	1									5.5	8	5	19
63	II-I ECE-A	21VESA0404	BUNREDDY VISHNU VARDHAN	0.5	1	1	1	0.5								4	6	5	15
64	II-I ECE-A	21VESA0405	DEVUNOORI PRIYANKA	1	1	1	1.5	1.5	1							7	8	5	20
65	II-I ECE-A	21VESA0406	KODALI SHALEM	1	1.5	1	2	1	1	1	0.5	1				7.5	7	5	20
66	II-I ECE-A	21VESA0407	VALLALA MOHITH	1.5	1.5	0.5	1	1.5	0.5							6.5	6	5	18

1	II-I ECE-B	20VE1A0461	ADDALA VIMALA KUMARI	0.5			2	2	0.5	0	1.5	0.5				6.5	4.5	5	16
2	II-I ECE-B	20VE1A0462	ADLA DEEPTHI				1.5	2	0.5	2	1.5	0.5				8	6.5	5	20
3	II-I ECE-B	20VE1A0463	AKARAPU YAMINI	2	1.5	0.5		1.5	0.5				1			6	6.5	5	18
4	II-I ECE-B	20VE1A0464	AKSHAY RAGIPHANI	0			2									3	7.5	5	16
5	II-I ECE-B	20VE1A0465	AMDA HARSHITHA				1.5	2	0	2	0.5	0.5				6.5	6.5	5	18
6	II-I ECE-B	20VE1A0466	AVULA PALLAVI				2	2	0				1.5	0.5	1	7	6.5	5	19
7	II-I ECE-B	20VE1A0467	BACHSHANKAR YUVRAJ SINGH							2						2	5	5	12
8	II-I ECE-B	20VE1A0468	BANDARI KUSHI				1.5	2	0	2			1.5		1	6	5	5	16
9	II-I ECE-B	20VE1A0469	BARAKA CHARAN KUMAR				1.5	1.5					2	2	1	8	5.5	5	19
10	II-I ECE-B	20VE1A0471	BODDUPALLY NANDINI				2	2	0.5	2	2	0.5				9	7.5	5	22
11	II-I ECE-B	20VE1A0472	DADINABOYINA AKSHAY YADAV																
12	II-I ECE-B	20VE1A0473	DASARI SIDDHARTHA				1	1.5							1	3.5	3.5	4	11
13	II-I ECE-B	20VE1A0474	DEVULAPALLY SWATHI	0.5	2	0.5							2	2	1	8	4	5	17
14	II-I ECE-B	20VE1A0475	DINDU MANI KRISHNA GOUD																
15	II-I ECE-B	20VE1A0476	GANDHAM VEERABABU	0.5	0					2						2.5	5.5	3	11
16	II-I ECE-B	20VE1A0477	GATTU SHREYA REDDY				1.5	2		1	1		1.5		1	6	6.5	5	18
17	II-I ECE-B	20VE1A0478	GAYANI SATHVIKA VEMPATI	1.5		1		1.5			2	0.5	1.5	2	1	7	5	5	17
18	II-I ECE-B	20VE1A0479	JALLA ANUSHA				1.5	2					1		1	5.5	4.5	5	15
19	II-I ECE-B	20VE1A0480	JEELA NAVEEN	0.5			0.5	1.5								2.5	5	5	13
20	II-I ECE-B	20VE1A0481	KARNATI VAMSHIKRISHNA																
21	II-I ECE-B	20VE1A0482	KOLLIPARA RAJESH	0.5			0.5	1.5					0.5			2.5	2	5	10
22	II-I ECE-B	20VE1A0483	KOTAPATI SATHYA VARA PRASAD	0	0		0							0	0	0	5	3	8
23	II-I ECE-B	20VE1A0484	LODANGI RAKESH	1	1	1	0.5	0	1				0.5		1	4.5	5	5	15
24	II-I ECE-B	20VE1A0485	M JAGALINGA				1	1					2	1.5	1	6.5	3.5	5	15
25	II-I ECE-B	20VE1A0486	MACHIPEDDI PRAVALIKA				1.5	2					2	2	1	8.5	5	5	19
26	II-I ECE-B	20VE1A0487	MANCHALA SAI HARSHITH				1.5	0.5					1.5		1	4.5	4	5	14
27	II-I ECE-B	20VE1A0488	MARRIPELLI NITHIN														4.5		5
28	II-I ECE-B	20VE1A0489	MERUGU PAVAN GOUD				1	2					0.5		1	4.5	4.5	5	14
29	II-I ECE-B	20VE1A0490	NADIMGERI ANIL KUMAR					1.5					0.5		1	3	5	5	13
30	II-I ECE-B	20VE1A0491	NARAHARI ANUDEEP REDDY	1.5	2								0.5	1.5	1	6.5	4	5	16
31	II-I ECE-B	20VE1A0492	NELLIKONDI AJAY KUMAR REDDY	2	1	1	1	0.5								5.5	4.5	5	15
32	II-I ECE-B	20VE1A0493	NUTANAKANTI PAVAN																
33	II-I ECE-B	20VE1A0494	P PRANATHI [redacted]	2	1	1	2	2	0.5							8.5	[redacted]	5	18
34	II-I ECE-B	20VE1A0495	PENDYALA MAHANTH	1			1.5									2.5	3.5	5	11
35	II-I ECE-B	20VE1A0497	PONUGOTI SWATHANTRA RAO		1	1	1.5	1	0.5							5	4	5	14
36	II-I ECE-B	20VE1A0498	RAMISETTI KIREETI	1	1.5	1	1	1.5	0.5							6.5	5.5	5	17
37	II-I ECE-B	20VE1A0499	RANGINEENI YASASWINI SATHYA				1.5	2					1.5	0.5	1	6.5	3.5	5	15
38	II-I ECE-B	20VE1A04A0	RAPOL BHARGAV REDDY					0.5		0.5						1	3	3	7
39	II-I ECE-B	20VE1A04A1	SEELAM SUNIL										0.5			0.5		5	6
40	II-I ECE-B	20VE1A04A2	SHAIK NASIR HUSSAIN		0.5								0.5			1	2	5	8
41	II-I ECE-B	20VE1A04A3	SHAMPURI BINDHU SRI				1	2					2		0.5	5.5	2.5	5	13
42	II-I ECE-B	20VE1A04A4	SINGIREDDY CHANDRA SHEKAR				0.5								0.5	1	2.5	5	9
43	II-I ECE-B	20VE1A04A5	SUREPALLY ADITH	1.5	1	0.5	1.5	1								5.5	6	5	17
44	II-I ECE-B	20VE1A04A6	TADI NAGA BHAGYA SRI	1		1	2	2	0.5							6.5	4	5	16
45	II-I ECE-B	20VE1A04A7	THORRURU SONYPRIYA	2		1	1.5	2								6.5	6.5	5	18
46	II-I ECE-B	20VE1A04A8	VALLAKATI NANDU	0.5	1.5	1	1.5	1.5								6	4.5	5	16
47	II-I ECE-B	20VE1A04A9	VANJA LAHARI REDDY				1	1.5					1	0.5	1	5	4	5	14
48	II-I ECE-B	20VE1A04B0	VIGRAHALA VENKATA DHRITI				2	2					1.5		1	6.5	4.5	5	16
49	II-I ECE-B	20VE1A04B1	VISLAVATH MACHENDER	0.5	0.5	1	1.5		0.5							4	4	5	13
50	II-I ECE-B	20VE1A04B2	VYDYULA RISHITHA							2	2	0.5	2	2		8.5	6.5	5	20
51	II-I ECE-B	20VE1A04B3	YEJARLA NARASIMHA				2		0.5				0.5		1	4	4	4	12
52	II-I ECE-B	20VE1A04B4	B KISHORE CHAND	0.5	0.4	0.5	1									2.4	4	5	12
53	II-I ECE-B	20VE1A04B5	CHAMA VAMSHIDHAR REDDY																
54	II-I ECE-B	20VE1A04B6	SHAIK AYAZ												0	0	0.5	0	1
55	II-I ECE-B	21VESA0408	BAGANI SHAIK ALTHAF BASHA				2	0.5	0.5				0.5	0.5	1	5	4	5	14
56	II-I ECE-B	21VESA0409	CHAMBETI VENKATA SAI	0.5		1	1.5	0.5								3.5	6	5	15
57	II-I ECE-B	21VESA0410	GAVVALA SAI TEJA	1	1.5	1	2	2								7.5	6	5	19
58	II-I ECE-B	21VESA0411	GUGULOTHU SRINATH				1.5	2					2	0.5	1	7	6.5	5	19
59	II-I ECE-B	21VESA0412	JINKALA KARTHIK	1		1							2	2	1	7	2.5	5	15
60	II-I ECE-B	21VESA0413	MATAM SAI NITHIN	1.5	1.5	0.5	2	2	0.5							8	3	5	16
61	II-I ECE-B	21VESA0414	VEERABOMMA PRASANTH				2	2	1				1.5	0.5	1	8	5.5	5	19
62	II-I ECE-B	21VESA0415	MANGALI MADHU LOHITH				0.5									0.5	2.5	0	3
				CO1	CO2	CO3	CO1	CO2	CO3	CO1	CO2	CO3	CO1	CO2	CO3				
Total Marks				49.75	32.4	30	130.25	124	18	37	24.5	8	74	36.5	44.5	582.4	529	582	1725
No of Students Answered				50	31	37	101	82	41	27	17	16	52	28	54	121	121	121	122
No of Students scoring > threshold				28	21	35	83	71	31	22	13	14	40	18	48	67	49	119	85
% of students scoring > thershold				56.0	67.7	94.6	82.2	86.6	75.6	81.5	76.5	87.5	76.9	64.3	88.9	55.4	40.5	98.3	69.7

S.No	Date of Review	Remarks	Signature

COURSE COMPLETION CERTIFICATE

I M.Pavani faculty in the Dept of ECE has completed entire (5 Units) syllabus and the course work for the subject ELECTRONIC DEVICES AND CIRCUITS of II year I Semester, for the academic year 2021-2022.



Signature of the faculty

This is to certify that Mr/Mrs M. PAVANI had completed the syllabus and course work for the allocated subject ELECTRONIC DEVICES AND CIRCUITS of II year I semester for the academic year 2021-2022.

Remarks if any:

HOD, ECE

Head of the Department
Electronics & Communication Engineering
Sreyas Institute of Engineering and Technology
Beside Indu Aranya Nagole, Hyderabad-500068.