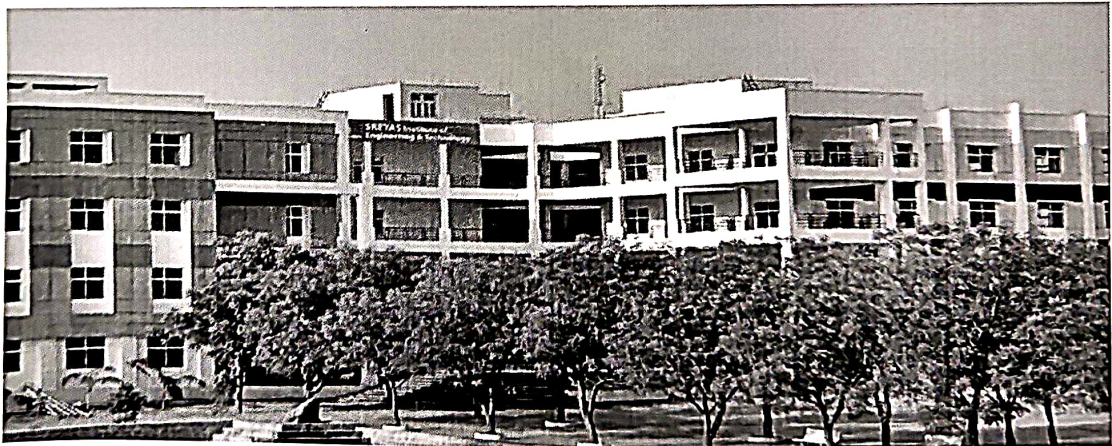


COURSE FILE

**MICROPROCESSORS AND MICROCONTROLLERS**



**Department of Electronics & Communication Engineering**  
**SREYAS INSTITUTE OF ENGINEERING AND TECHNOLOGY**

*An Autonomous Institution*

Approved by AICTE, Affiliated to JNTUH

Accredited by NAAC-A Grade, NBA (CSE, ECE & ME) & ISO 9001:2015 Certified

**2023-24**



# COURSE DESCRIPTION

Faculty Name	<b>Ravali Maraju</b>
Designation	Asst. Professor
Department	Electronics and Communication Engineering
Batch	2023-2024
Academic Year	2023-24
Year & Semester	III-I
Section (Branch and Section)	ECE-A&B

Course title	<b>MICROPROCESSORS AND MICROCONTROLLERS</b>			
Course code	EC501PC			
Regulation	R-18			
Course Duration	16 WEEKS			
Course structure	Lectures	Tutorials	Practical	Credits
	4	0	0	4
Main Coordinator	Ch. S. V. Maruthi Rao			
Team of instructors	Ch. S. V. Maruthi Rao	M.RAVALI		

Prerequisites	Graduation Level	Credits	Periods/Week
1. Switching Theory and Logic Design	UG	4	4
2. Computer Organization	UG	3	3

Evaluation Scheme:				
S.No	Component		Duration	Marks
1	I - mid exam	Descriptive - answer any 2 of 4 - (10) Objective -answer all 20 Questions- (10)	80 Min	20
2	I - Assignment	Descriptive	-	5
3	II - Mid exam	Descriptive - answer any 2 of 4 - (10) Objective -answer all - (10)	80 Min	20
4	II - Assignment	Descriptive	-	5
6	External exam	Descriptive	3 Hours	75

Attainment target for the semester	CO1-T	CO2-T	CO3-T	CO4-T	CO5-T	CO6-T
	3	3	3	3	3	3





## COURSE DESCRIPTION

Faculty Name	<b>Ravali Maraju</b>
Designation	Asst. Professor
Department	Electronics and Communication Engineering
Batch	2023-2024
Academic Year	2023-24
Year & Semester	III-I
Section (Branch and Section)	ECE-A&B

Course title	<b>MICROPROCESSORS AND MICROCONTROLLERS</b>			
Course code	EC501PC			
Regulation	R-18			
Course Duration	16 WEEKS			
Course structure	Lectures	Tutorials	Practical	Credits
	4	0	0	4
Main Coordinator	Ch. S. V. Maruthi Rao			
Team of instructors	Ch. S. V. Maruthi Rao	M.RAVALI		

Prerequisites	Graduation Level	Credits	Periods/Week
1. Switching Theory and Logic Design	UG	4	4
2. Computer Organization	UG	3	3

Evaluation Scheme:				
S.No	Component		Duration	Marks
1	I - mid exam	Descriptive – answer any 2 of 4 – (10) Objective –answer all 20 Questions– (10)	80 Min	20
2	I - Assignment	Descriptive	-	5
3	II - Mid exam	Descriptive – answer any 2 of 4 – (10) Objective –answer all – (10)	80 Min	20
4	II - Assignment	Descriptive	-	5
6	External exam	Descriptive	3 Hours	75

Attainment target for the semester	CO1-T	CO2-T	CO3-T	CO4-T	CO5-T	CO6-T
	3	3	3	3	3	3



## VISION - MISSION - PEOS

	<p><b>Institute Vision :</b></p> <p>Sreyas will be a global leader in imparting future Education with human values. It fosters ethical, social &amp; moral values through holistic learning to groom young minds into responsible and successful global citizens.</p>
	<p><b>Institute Mission :</b></p> <p>To strive relentlessly &amp; vigorously – to realize the vision by making the best use of quality infrastructure, resources &amp; experienced, talented &amp; committed faculty.</p>

	<p><b>Department Vision :</b></p> <p>To excel in Electronics &amp; Communication Engineering education with the knowledge of innovation, research and ethics.</p>
	<p><b>Department Mission:</b></p> <ol style="list-style-type: none"><li>1. To provide academic environment that promotes student centric learning through quality education and state of the art infrastructure.</li><li>2. To make the students aspire towards innovation and research to meet the technological needs of society.</li><li>3. To engage the students in activities which inculcate professional practices with social concern.</li></ol>



**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD****ACADEMIC CALENDAR 2023-24****B. Tech./B. Pharm. III YEAR I & II SEMESTERS****I SEM**

S. No	Description	Duration	
		From	To
1	Commencement of I Semester classwork	11.10.2023	
2	1 <sup>st</sup> Spell of Instructions (including Dussehra Recess)	11.10.2023	12.12.2023 (9 Weeks)
3	Dussehra Recess	23.10.2023	28.10.2023 (1 Week)
4	First Mid Term Examinations	13.12.2023	19.12.2023 (1 Week)
5	Submission of First Mid Term Exam Marks to the University on or before	23.12.2023	
6	2 <sup>nd</sup> Spell of Instructions	20.12.2023	19.02.2024 (8 Weeks)
7	Second Mid Term Examinations	20.02.2024	24.02.2024 (1 Week)
8	Preparation Holidays and Practical Examinations	26.02.2024	02.03.2024 (1 Week)
9	Submission of Second Mid Term Exam Marks to the University on or before	28.02.2024	
10	End Semester Examinations	04.03.2024	16.03.2024 (2 Weeks)

Note: No. of Working/ instructional days: 90

**EC501PC: MICROPROCESSORS & MICROCONTROLLERS****B.Tech. III Year I Sem.**

<b>UNIT-1</b>	<p><b>8086 Architecture:</b> 8086 Architecture – Functional Diagram, Organization, Memory Segmentation, Programming Address, Physical Memory Organization, Architecture Descriptions of 8086, Interrupts of 8086.</p> <p><b>Instruction Set and Assembly Language Programming of 8086:</b> Instruction Formats, Addressing Modes, Instruction Set, Assembler Directives, Macros and Simple Programs involving Logical, Branch and Call Instructions, Sorting, String Manipulations.</p>
<b>UNIT-2</b>	<p><b>Introduction to Microcontrollers:</b> Overview of 8051 Microcontroller, Architecture, I/O Ports, Memory Organization, Addressing Modes and Instruction Set of 8051.</p> <p><b>8051 Real Time Control:</b> Programming Timer Interrupts, Programming External Hardware Interrupts, Programming the Serial Communication Interrupts, Programming 8051 Timers and Counters.</p>
<b>UNIT-3</b>	<p><b>I/O and Memory Interface:</b> LCD, Keyboard, External Memory RAM, ROM Interface, ADC, DAC Interface to 8051.</p> <p><b>Serial Communication and Bus Interface:</b> Serial Communication Standards, Serial Data Transfer Scheme, Onboard Communication Interfaces – I<sup>2</sup>C Bus, SPI Bus, UART; External Communication Interfaces – RS232, USB.</p>
<b>UNIT-4</b>	<p><b>ARM Architecture:</b> ARM Processor Fundamentals, ARM Architecture – Register, CPSR, Pipeline, Exceptions and Interrupts, Interrupt Vector Table, ARM Instruction Set – Data Processing, Branch Instructions, Load Store Instructions, Software Interrupt Instructions, Program Status Register Instructions, Loading Constants, Conditional Execution, Introduction to Thumb Instructions.</p>
<b>UNIT-5</b>	<p><b>Advanced ARM Processors:</b> Introduction to CORTEX Processor and its Architecture, OMAP Processor and its Architecture.</p>





## TEXT/REF/WEB/JOURNALS /BEYOND SYLLABUS/GAPS

S.No.	Text Books	Publication
1.	Advanced Microprocessors and Peripherals – A. K. Ray and K. M. Bhurchandani.	MHE, 2nd Edition, 2006
2.	The 8051 Microcontroller, Kenneth J. Ayala	Cengage Learning, 3rd Ed.
3.	ARM System Developers Guide, Andre N SLOSS, Dominic SYMES, Chris WRIGHT	Elsevier, 2012

S.No.	Ref Books	Publication
1.	Microprocessors and Interfacing, D. V. Hall	MGH, 2nd edition, 2006
2.	Introduction to Embedded Systems, Shibu K. V.	
3.	The 8051 Microcontrollers – Architecture, Programming and Applications – K. Uma Rao, Andhe Pallavi	

Text Books & P  
B  
WEB/Journals

S.No.	Web Link
1.	<a href="https://onlinecourses.nptel.ac.in/noc19_ee11/student/home">https://onlinecourses.nptel.ac.in/noc19_ee11/student/home</a>
2.	<a href="http://www.ocw.mit.edu">www.ocw.mit.edu</a> MIT Open Courseware

S.No.	Journal
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S.No.	Topics Beyond Syllabus
1.	Instruction Cycle and Machine Cycle execution in 8086
2.	Minimum and Maximum mode of 8086
3.	UART Interfacing with 8086
4.	Programming using ARM instructions

S.No.	Gaps In Curriculum
1.	16 Bit Microprocessor
2.	Differences between Processor, Controller and SOC
3.	Application of Thumb Instructions



Program Outcomes	
PO 1	<b>Engineering Knowledge:</b> Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO 2	<b>Problem analysis:</b> Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO 3	<b>Design/development of solutions:</b> Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO 4	<b>Conduct investigations of complex problems:</b> Use knowledge and research methods including design analysis and interpretation of data, and synthesis of the system to provide valid conclusions.
PO 5	<b>Modern tool usage:</b> Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO 6	<b>The engineer and society:</b> Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO 7	<b>Environment and sustainability:</b> Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO 8	<b>Ethics:</b> Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO 9	<b>Individual and team work:</b> Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO 10	<b>Communication:</b> Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions
PO 11	<b>Project management and finance:</b> Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO 12	<b>Life-long learning:</b> Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.





**Program specific outcomes**

PSO1	Design, analyze and develop modules and systems for applications in advanced electronics and communication systems.
PSO2	Utilize modern tools for modeling and computational techniques in IC fabrication and RF technologies.



## COURSE OBJ, CO, CO-PO MAPPING

C301		Course Objectives
A	To understand the architecture of 8086 Microprocessor both at functional level and as programmers model and develop assembly language programs by understanding the instruction set and addressing modes.	
B	To understand the architecture of 8051 Microcontroller and develop assembly language programs by understanding the instruction set and addressing modes. And also understand the real time control of 8051 through interrupts, timers and counters.	
C	Understand and apply the interfacing techniques for 8086 and 8051 to various I/O and ADC/DAC devices.	
D	Understand the various serial communication standards for onboard and external communication interfaces.	
E	Learn the basics of the internal architecture and registers of ARM and understand the ARM / Thumb instruction set.	
	Understand the internal architecture of advanced arm processors like CORTEX & OMAP	

Course  
Course  
CO - PO

C301		Course Outcomes
1	Able to understand the internal architecture and organization of 8086 and develop assembly programs using various instructions.	
2	Able to understand the internal architecture, organization and interrupts of 8051 and develop assembly programs using various instructions.	
3	Able to understand the various I/O interfacing techniques to 8086 and 8051.	
4	Able to understand the various onboard and external serial communication standards and schemes.	
5	Able to understand the internal architecture and organization of ARM and develop assembly programs using various instructions.	
6	Able to understand the architecture of advanced ARM processors - CORTEX and OMAP	

COURSE OBJECTIVES						COs	PROGRAM OUTCOMES (POs)												PSOs	
A	B	C	D	E	F		1	2	3	4	5	6	7	8	9	10	11	12	I	II
X						CO1	2	1	3	1	2	0	0	1	1	0	0	0	1	1
	X					CO2	2	1	3	1	2	0	0	1	1	0	0	0	1	1
		X				CO3	2	1	3	1	2	0	0	0	1	0	0	1	1	1
			X			CO4	2	0	0	0	0	0	0	0	1	0	0	1	0	0
				X		CO5	2	1	1	2	2	0	0	1	1	1	0	1	1	0
					X	CO6	2	1	0	0	0	0	0	0	0	0	0	1	0	0
Signature Faculty												Signature HOD								





## COURSE OBJECTIVES & COURSE OUTCOME

### Course Objectives:

1	To understand the architecture of 8086 Microprocessor both at functional level and as programmers model and develop assembly language programs by understanding the instruction set and addressing modes.
2	To understand the architecture of 8051 Microcontroller and develop assembly language programs by understanding the instruction set and addressing modes. And also understand the real time control of 8051 through interrupts, timers and counters.
3	Understand and apply the interfacing techniques for 8086 and 8051 to various I/O and ADC/DAC devices.
4	Understand the various serial communication standards for onboard and external communication interfaces.
5	Learn the basics of the internal architecture and registers of ARM and understand the ARM / Thumb instruction set.
6	Understand the internal architecture of advanced arm processors – CORTEX & OMAP.

**Course Outcomes:** Upon completion of this course, the student will be able to

CO1:	Able to understand the internal architecture and organization of 8086 and develop assembly programs using various instructions.
CO2:	Able to understand the internal architecture, organization and interrupts of 8051 and develop assembly programs using various instructions.
CO3:	Able to understand the various I/O interfacing techniques to 8086 and 8051
CO4:	Able to understand the various onboard and external serial communication standards and schemes.
CO5:	Able to understand the internal architecture and organization of ARM and develop assembly programs using various instructions.
CO6:	Able to understand the architecture of advanced ARM processors – CORTEX and OMAP



# TIME TABLE

SEC-A	1	2	3	4	Break	5	6	7
MON		Batch-1					MPMC	
TUE								
WED	MPMC							MPMC
THU		Batch-2						
FRI			MPMC				MPMC	
SAT						MPMC		

SEC-B	1	2	3	4	Break	5	6	7
MON	MPMC							
TUE		Batch-1					MPMC	
WED								MPMC
THU	MPMC					Batch-2		
FRI								MPMC
SAT				MPMC				

Time







# COURSE PLAN

Cou

MICROPROCESSORS AND MICROCONTROLLERS III YEAR – I SEM ECE

  
Dr. K. SAGAR  
B.E. M.Tech. Ph.D.  
Principal & Professor in CSE  
Sreyas Institute of Engineering and Technology  
Hyderabad, Telangana-500 068.



# SREYAS INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Approved by AICTE, New Delhi | Affiliated to JNTUII, Hyderabad | Accredited by NAAC & NBA)  
Hyderabad | PIN: 500068

## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

### COURSE INFORMATION SHEET

Course Code : EC501PC

Name of the Course : MICROPROCESSORS & MICROCONTROLLERS

Name of the faculty : RAVALI M

Designation : ASSISTANT PROFESSOR

Year / Branch / Section: III A&B

Academic Year / Semester: 2023-24 I-Semester

No. of Lecture Hours per week : 5

No. of Tutorial classes per week : 1

Prerequisite : Digital System Design

#### Course Objectives:

- To understand the architecture of 8086 Microprocessor both at functional level and as programmers model and develop assembly language programs by understanding the instruction set and addressing modes.
- To understand the architecture of 8051 Microcontroller and develop assembly language programs by understanding the instruction set and addressing modes. And also understand the real time control of 8051 through interrupts, timers and counters.
- Understand and apply the interfacing techniques for 8086 and 8051 to various I/O and ADC/DAC devices.
- Understand the various serial communication standards for onboard and external communication interfaces.
- Learn the basics of the internal architecture and registers of ARM and understand the ARM / Thumb instruction set.
- Understand the internal architecture of advanced arm processors – CORTEX & OMAP.

#### Course Outcomes:

Course Name	Course Outcomes
C301.1	Able to understand the internal architecture and organization of 8086 and develop assembly programs using various instructions.
C301.2	Able to understand the internal architecture, organization and interrupts of 8051 and develop assembly programs using various instructions.
C301.3	Able to understand the various I/O interfacing techniques to 8086 and 8051
C301.4	Able to understand the various onboard and external serial communication standards and schemes.
C301.5	Able to understand the internal architecture and organization of ARM and develop assembly programs using various instructions.
C301.6	Able to understand the architecture of advanced ARM processors – CORTEX and OMAP

#### CO-PO / PSOs Mapping:

COs	PROGRAM OUTCOMES (POs)												PSOs	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
C301.1	2	1	3	1	2	-	-	1	1	-	-	-	1	1
C301.2	2	1	3	1	2	-	-	1	1	-	-	-	1	1
C301.3	2	1	3	1	2	-	-	-	1	-	-	1	1	1
C301.4	2	-	-	-	-	-	-	-	1	-	-	1	-	-
C301.5	2	1	1	2	2	-	-	1	1	1	-	1	1	1
C301.6	2	1	-	-	-	-	-	-	-	-	-	1	1	1

Sign.of the faculty

Domain Lead

Page 1 of 4

Head of the Dept

Dr. K. SAGAR  
B.E., M.Tech., Ph.D.  
Principal & Professor in CSE  
Sreyas Institute of Engineering and Technology  
Hyderabad, Telangana-500 068.





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Hyderabad | PIN: 500068

## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

### COURSE INFORMATION SHEET

Course Code : EC501PC

Name of the Course : MICROPROCESSORS & MICROCONTROLLERS

Name of the faculty : RAVALI M

Designation : ASSISTANT PROFESSOR

Year / Branch / Section: III A&B

Academic Year / Semester: 2022-23 I-Semester

No. of Lecture Hours per week : 4

No. of Tutorial classes per week : 1

Prerequisite : Digital System Design

#### GAPS IN CURRICULUM AND MAPPING WITH POs & PSOs

S.No.	GAP IN CURRICULUM	MODE OF DELIVERY	PROGRAM OUTCOMES (POs)												PSOs	
			1	2	3	4	5	6	7	8	9	10	11	12	1	2
1.	Instruction cycle and Machine cycle execution in 8086.	Guest lecture	1	-	-	-	-	-	-	-	1	-	-	2	2	2
2.	UART Interfacing with 8086	Guest lecture	1	-	-	-	-	-	-	-	1	-	-	2	2	2
3.	Programming using ARM Instructions	Guest lecture	1	-	-	-	-	-	-	-	1	-	-	2	2	2

#### CONTENT BEYOND SYLLABUS AND MAPPING WITH PO's & PSO's

S.No.	TOPICS BEYOND SYLLABUS	MODE OF DELIVERY	PROGRAM OUTCOMES (POs)												PSOs	
			1	2	3	4	5	6	7	8	9	10	11	12	1	2
1.	16 Bit Micro controller	Guest lecture	1	-	-	-	-	-	-	-	1	-	-	2	2	2
2.	Difference between processor, controller and SOC	Guest lecture	1	-	-	-	-	-	-	-	1	-	-	2	2	2
3.	Applications of thumb instructions	Guest lecture	1	-	-	-	-	-	-	-	1	-	-	2	2	2

Sign.of the faculty

Domain Lead

Head of the Department



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Hyderabad | PIN: 500068

## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

### LESSON PLAN SESSION WISE

Course Code : EC501PC

Name of the Course : MICROPROCESSORS & MICROCONTROLLERS

Name of the faculty : RAVALI M

Designation : ASSISTANT PROFESSOR

Year / Branch / Section: III ECE A&B

Academic Year / Semester: 2022-23 I-Semester

No. of Lecture Hours per week : 5

No. of Tutorial classes per week : 1

Prerequisite : Digital System Design

Unit	Week	Cumulative Period	Topic(s) to be covered	Text Book/ Reference Book	Mode of Teaching	Planned Date	Actual Date of completion
UNIT-I	WEEK-1	1	Introduction to Course, Course outcomes, CO-PO mapping		WB	11/10/23	12-10-23
		2	Introduction to Microprocessors & Microcontrollers		WB	12/10/23	13-10-23
		3	Block diagram of MP & MC; Differences of MP & MC		WB	13/10/23	14-10-23
		4	<b>8086 Architecture:</b> 8086 Architecture – Functional Diagram	T1, Ch1	WB	14/10/23	16-10-23
		5	Register Organization	T1, Ch1	WB	16/10/23	17-10-23
	WEEK-2	5	Memory Segmentation	T1, Ch1	WB	17/10/23	18-10-23
		6	Programming Model	T1, Ch1	WB	18/10/23	18-10-23
		7	Memory Addresses	T1, Ch1	WB	19/10/23	19-10-23
		8	Physical Memory Organization	T1, Ch1	WB	20/10/23	20-10-23
	WEEK-3	9	Architecture of 8086	T1, Ch1	WB	30/10, 31/11/23	31-10-23
		10	Signal Descriptions of 8086	T1, Ch1	WB	1/11/23	2-11-23
		11	Interrupts of 8086	T1, Ch4	WB	2/11,3/11,4/11/23	3-11-23
		12	<b>Instruction Set and Assembly Language Programming of 8086:</b> Instruction Formats	T1, Ch2	WB	6/11/23	7-11-23
		13	Addressing Modes	T1, Ch2	WB	7/11/23	8-11-23
WEEK-4	14	Instruction Set	T1, Ch2	WB	8/11,9/11	8-11-23	
	15	Assembler Directives	T1, Ch2	WB	9/11/23	10-11-23	
	16	Macros	T1, Ch4	WB	10/11/23	13-11-23	
	17	Simple Programs involving Logical, Branch and Call Instructions	T1, Ch3	WB	13/11/23	14-11-23	
UNIT-II	WEEK-5	18	Sorting	T1, Ch3	WB	14/11/23	15-11-23
		19	String Manipulations	T1, Ch2	WB	15/11/23	16-11-23
		20	<b>Introduction to Microcontrollers:</b> Overview of 8051 Microcontroller	T2, Ch2	WB	16/11/23	17-11-23
	WEEK-6	21	Architecture	T2, Ch2	WB	17/11/23	20-11-23
		22	I/O Ports	T2, Ch2	WB	20/11, 21/11, 22/11/23	22-11-23 23-11-23
		23	Memory Organization	T2, Ch2	WB	23/11/23	24-11-23
		24	Addressing Modes	T2, Ch3	WB	24/11/23	26-11-23
	WEEK-7	25	Instruction Set of 8051	T2, Ch4	WB	26/11/23	28-11-23
		26	<b>8051 Real Time Control:</b> Programming Timer Interrupts	T2, Ch2	WB	28/11/23	29-11-23
		27	Programming External Hardware Interrupts	T2, Ch2	WB	29/11/23	30-11-23



UNIT	WEEK	Topic	Chapters	Mode	Start Date	End Date	
UNIT-III	WEEK-8	28	Programming Serial Commn. Interrupts	T2, Ch2	WB	30/11, 1/12/23	2-12-23
		29	Programming 8051 Timers & Counters	T2, Ch2	WB	2/12/23	4-12-23
		30	I/O and Memory Interface: LCD	T2, Ch8	WB	4/12/23	6-12-23
		31	Keyboard	T2, Ch8	WB	5/12/23	5-12-23
		32	External Memory RAM	T2, Ch3	WB	6/12/23	6-12-23
	WEEK-9	33	ROM Interface	T2, Ch3	WB	7/12/23	7-12-23
		34	ADC, DAC Interface to 8051	T2, Ch3	WB	8/12/23	8-12-23
		35	Serial Communication and Bus Interface: Serial Communication Standards	T2, Ch9	WB	11/12/23	11-12-23
		36	Serial Data Transfer Scheme	T2, Ch9	WB	12/12/23	12-12-23
		37	On-Board Communication Interfaces	T2, Ch9	WB	20/12/23	20-12-23
	WEEK-10	38	I2C Bus	T2, Ch9	WB	21/12/23	21-12-23
		39	SPI Bus	T2, Ch9	WB	22/12/23	27-12-23
40		UART	R2, Ch2	WB	27/12/23	28-12-23	
41		External Communication Interfaces	R2, Ch2	WB	28/12/23	29-12-23	
WEEK-11	42	RS-232	R2, Ch2	WB	29/12/23	2-1-24	
	43	USB	R2, Ch2	WB	2/1/24	3-1-24	
	44	ARM Architecture: ARM Processor Fundamentals & Features	T3, Ch2	WB	3/1/24	4-1-24	
	45	ARM Architecture	T3, Ch2	WB	4/1/24	5-1-24	
	46	Register Organization	T3, Ch2	WB	5/1/24	8-1-24	
	47	CPSR, Pipeline	T3, Ch2	WB	8/1, 9/1/24	9-1-24	
WEEK-12	48	Exceptions and Interrupts	T3, Ch2	WB	10/1/24	10-1-24	
	49	Interrupt Vector Table, Interrupt priority table	T3, Ch2	WB	11/1/24	11-1-24	
	50	ARM Instruction Set – Data transfer Instructions	T3, Ch3	WB	12/1/24	12-1-24	
	51	Arithmetic, Logical, Multiplication Instructions	T3, Ch3	WB	17/1/24	17-1-24	
	52	Branch Instructions	T3, Ch3	WB	18/1/24	18-1-24	
	53	Load-Store Instructions	T3, Ch3	WB	19/1/24	22-1-24	
	54	Software Interrupt Instructions	T3, Ch3	WB	22/1/24	24-1-24	
	55	Program Status Register Instructions	T3, Ch3	WB	23/1/24	28-1-24	
WEEK-13	56	Loading Constants	T3, Ch3	WB	24/1/24	1-2-24	
	57	Conditional Execution	T3, Ch3	WB	28/1/24	2-2-24	
	58	Introduction to Thumb Instructions	T3, Ch3	WB	1/2/24	5-2-24	
	59	Thumb Instruction set	T3, Ch3	WB	2/2/24	6-2-24	
UNIT-IV	WEEK-14	60	Thumb Instruction set	T3, Ch3	WB	5/2/24	6-2-24
		61	Advanced ARM Processors: Introduction to CORTEX Processor and its Architecture	T3, Ch11	WB	6/2/24	7-2-24
		62	Cont...	T3, Ch11	WB	7/2/24	8-2-24
	WEEK-15	63	Cont...	T3, Ch11	WB	8/2/24	9-2-24
		64	OMAP Processor and its Architecture	T3, Ch11	WB	9/2/24	12-2-24
		65	Cont...	T3, Ch11	WB	12/2/24	13-2-24
		66	Revision on Unit-1	T3, Ch11	WB	13/2/24	14-2-24
		67	Revision on Unit-2	T3, Ch11	WB	14/2/24	15-2-24
		68	Revision on Unit-3	T3, Ch11	WB	15/2/24	15-2-24
		69	Revision on Unit-4	T3, Ch11	WB	16/2/24	16-2-24
70	Revision on Unit-5	T3, Ch11	WB	18/2/24	18-2-24		

\*WB: White Board

Sign. of the faculty

Text Books:

1. Advanced Microprocessors and Peripherals – A. K. Ray and K. M. Bhurchandani, MHE, 2<sup>nd</sup> Edition, 2006.
2. The 8051 Microcontroller, Kenneth J. Ayala, Cengage Learning, 3<sup>rd</sup> Ed.
3. ARM System Developers Guide, Andre N SLOSS, Dominic SYMES, Chris WRIGHT, Elsevier, 2012.

Reference Books:

1. Microprocessors and Interfacing, D. V. Hall, MGH, 2<sup>nd</sup> Edition, 2006.
2. Introduction to Embedded Systems, Shibu K. V., MHE, 2009.
3. The 8051 Microcontrollers – Architecture, Programming and Applications – K. Uma Rao, Andhe Pallavi, Pearson, 2009.

Domain Lead

Head of the Department





## MID QUESTION PAPERS (PDF)

Mid Q  
with c



## MID QUESTION PAPERS WITH KEY

### III B.TECH I SEM. I-MID EXAMINATIONS SUBJECTIVE QUESTION PAPER – DEC, 2023 (A.Y. 2023-24)

Subject: Microprocessor & Microcontrollers.

Branch: ECE

Duration: **1 Hour**

Date: 13-12-2023 (FN)

Max Marks: **10**

Answer any TWO Questions

All Questions Carries Equal Marks

- 1) a) Explain the architecture of 8086 microprocessor with a neat sketch. [CO-1, BTL-2,2M]  
b) Differentiate between microprocessor and microcontroller. [CO-2, BTL-4,2M]  
c) Sketch the interfacing diagram of LCD with 8051 microcontroller. [CO-3, BTL-3,1M]
- 2) a) Explain five addressing modes of 8086 microprocessor with examples. [CO-1, BTL-2,2M]  
b) Explain the architecture of 8051 microcontroller with a neat sketch. [CO-2, BTL-2,2M]  
c) Sketch the interfacing diagram of DAC with 8051 microcontroller. [CO-3, BTL-3,1M]
- 3) a) Explain all the fields of flag register used in 8086 microprocessor. [CO-1, BTL-2,2M]  
b) Explain the internal RAM organization of 8051 microcontroller with a neat sketch. [CO-2, BTL-2,2M]  
c) Discuss on 16\*2 LCD with pin diagram. [CO-3, BTL-2,1M]
- 4) a) Explain following instructions with examples: [CO-1, BTL-2,2M]  
(i)DAA (ii)CMPS (iii)MOVX (iv)CALL  
b) Explain all the bits of TCON and TMOD registers. [CO-2, BTL-2,2M]  
c) Sketch the interfacing diagram of ADC with 8051 microcontroller. [CO-3, BTL-3,1M]

MICROPROCESSORS AND MICROCONTROLLERS

III YEAR – ISEM ECE

**III B.TECH I SEM. I-MID EXAMINATIONS SUBJECTIVE QUESTION PAPER – DEC, 2023 (A.Y. 2023-24)**

Subject: Microprocessor & Microcontrollers.

Branch: ECE

Duration: **1 Hour**

Date: 13-12-2023 (FN)

Max Marks: **10**

Answer any **TWO** Questions

All Questions Carries Equal Marks

- |  |                  |
|--|------------------|
| 1) a) Explain the architecture of 8086 microprocessor with a neat sketch.            | [CO-1, BTL-2,2M] |
| b) Differentiate between microprocessor and microcontroller.                         | [CO-2, BTL-4,2M] |
| c) Sketch the interfacing diagram of LCD with 8051 microcontroller.                  | [CO-3, BTL-3,1M] |
| 2) a) Explain five addressing modes of 8086 microprocessor with examples.            | [CO-1, BTL-2,2M] |
| b) Explain the architecture of 8051 microcontroller with a neat sketch.              | [CO-2, BTL-2,2M] |
| c) Sketch the interfacing diagram of DAC with 8051 microcontroller.                  | [CO-3, BTL-3,1M] |
| 3) a) Explain all the fields of flag register used in 8086 microprocessor.           | [CO-1, BTL-2,2M] |
| b) Explain the internal RAM organization of 8051 microcontroller with a neat sketch. | [CO-2, BTL-2,2M] |
| c) Discuss on 16*2 LCD with pin diagram.   | [CO-3, BTL-2,1M] |
| 4) a) Explain following instructions with examples:                                  | [CO-1, BTL-2,2M] |
| (i)DAA      (ii)CMPS      (iii)MOVX      (iv)CALL                                    |                  |
| b) Explain all the bits of TCON and TMOD registers.                                  | [CO-2, BTL-2,2M] |
| c) Sketch the interfacing diagram of ADC with 8051 microcontroller.                  | [CO-3, BTL-3,1M] |









# TUTORIAL QUESTIONS WITH SOLUTION

S.No.	Tutorial - I	BTL	COs	Marks	Q Check
1					
2					
3					
					HOD

S.No.	Tutorial - II	BTL	COs	Marks	Q Check
1					
2					
3					
					HOD

S.No.	Tutorial - III	BTL	COs	Marks	Q Check
1					
2					
3					
					HOD

S.No.	Tutorial - IV	BTL	COs	Marks	Q Check
1					
2					
3					
					HOD

S.No.	Tutorial - V	BTL	COs	Marks	Q Check
1					
2					
					HOD

MICROPROCESSORS AND MICROCONTROLLERS IIIYEAR - ISEM ECE

Register Block



# ASSIGNMENT QUESTIONS WITH ANSWERS

S.No.	Assignment - I	BTL	COs	Marks	Q Check
1					
2					
3					
4					
5					

HOD

S.No.	Assignment - II	BTL	COs	Marks	Q Check
1					
2					
3					
4					
5					

HOD

MICROPROCESSORS AND MICROCONTROLLERS IIIYEAR – ISEM ECE



## GUEST LECTURES / SEMINARS / FIELD VISITS

### Guest Lectures

Date	Resource person	Organization	Topic	No. of Students Attended

### Seminars

Date	Resource person	Organization	Topic	No. of Students Attended

### Industry /Field Visits

Date	Organization / field	Place of visit	Coordinator	No. of Students Attended

Guest  
So  
F





The following list of students attended / absent for the B.Tech - ECE  
remedial class conducted for III Year I Semester A2 B Section on  
7/2/24.

S.No	Roll No's	Name of the Student	Hr - 5	Hr - 6	Hr - 7
		Subject	MPMC	DCN	MPMC
1	21VE1A0466				AB
2	468	Likith	Likith	Likith	Likith
3	469				AB
4	470				AB
5	471				AB
6	472				
7	474	B.Ajay Reddy	B.Ajay	B.Ajay	B.Ajay
8	477				AB
9	478				AB
10	479				AB
11	482	D.Anjan Reddy	Anjan	Anjan	Anjan
12	483				
13	484	G. Mahesh	Mahesh	Mahesh	Mahesh
14	487	G. Alitesh Reddy	Alitesh	Alitesh	Alitesh
15	490	J. Abhinav	Abhinav	Abhinav	Abhinav
16	491	J. Mahesh	Mahesh	Mahesh	Mahesh
17	493				AB
18	494				AB
19	497	K. Saijithin	Saijithin	Saijithin	Saijithin
20	498				
21	499				
22	4A0	K. Anuram	Anuram	Anuram	Anuram
23	4A2				
24	4A3	M. Madhu Manasa	Manasa	Manasa	Manasa
25	4A4				
26	4A8	M. Vennela	Vennela	Vennela	Vennela
27	4A9				
28	4B1				
29	4B6	Preethika Chisatta	Ch. Preethika	Ch. Preethika	Ch. Preethika
30	4B7	R. Shiva	Shiva	Shiva	Shiva
31	4B8	R. Vishwanath Rahul	Rahul	Rahul	Rahul
32	4C0	S. Vishnu	Vishnu	Vishnu	Vishnu
33	4C2	E. Srija	Srija	Srija	Srija
34	4C4	T. Susan Smitha	Smitha	Smitha	Smitha
35	4C6	V. Nitin Reddy	Nitin	Nitin	Nitin
36	4C7				
37	22VE5A0412	R. Shashikanth	Shashikanth	Shashikanth	Shashikanth



# Sreyas Institute of Engineering and Technology

## An Autonomous Institution

Approved by AICTE, Affiliated to JNTUH  
Accredited by NAAC-A Grade, NBA (CSE, ECE & ME) & ISO 9001:2015 Certified

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

Date: 7/2/24

### ATTENDANCE SHEET

The following list of students attended / absent for the B.Tech ECE  
remedial class conducted for III Year I Semester A&B Section on  
7/2/24.

S.No	Roll No's	Name of the Student	Hr - 5	Hr - 6	Hr - 7
1	21VE1A0405	A. Sai Kiran	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
2	408				
3	410	B. Lokesh	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
4	411	Bathula Viswasree	<u>viswasree</u>	<u>viswasree</u>	<u>viswasree</u>
5	414	B.V. Ravitja	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
6	415	C. Jaykanth	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
7	416	Ch. Mounika	<u>mounika</u>	<u>mounika</u>	<u>mounika</u>
8	417	Shashank C	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
9	418	CH. Sreeja	<u>Sreeja</u>	<u>Sreeja</u>	<u>Sreeja</u>
10	419	D. CHARAN	<u>D. Charan</u>	<u>D. Charan</u>	<u>D. Charan</u>
11	420	D. Shirisha	<u>shirisha</u>	<u>shirisha</u>	<u>shirisha</u>
12	421	D. Sainishanth	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
13	425	G. Charan	<u>Charan</u>	<u>Charan</u>	<u>Charan</u>
14	426	G. Preetham	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
15	432				
16	434	G. Ashish	<u>Ashish</u>	<u>Ashish</u>	<u>Ashish</u>
17	436	K. Tejaswara	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
18	438	Kalyani B	<u>Kalyani</u>	<u>Kalyani</u>	<u>Kalyani</u>
19	440				
20	442				
21	443	M. Sriram Suresh	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
22	444	M. Venkat Nagesh	<u>Venkat</u>	<u>Venkat</u>	<u>Venkat</u>
23	450	P. Akhivanandan	<u>P. Akhivanandan</u>	<u>P. Akhivanandan</u>	<u>P. Akhivanandan</u>
24	455				
25	458	Syed Akis	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
26	461				
27	462	V. Madhu	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
28	22VE5A0401				
29	402				

Session Timings: 1:20 pm to 3:50 pm

Session Resource Person:

[Signature]  
Class Incharge

[Signature]  
Year Incharge

[Signature]  
Head of the Dept

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

**ATTENDANCE SHEET**

Date: \_\_\_\_\_

Dr. K. SAGAR  
BE, M.Tech, Ph.D  
Principal & Professor in CSE  
Sreyas Institute of Engineering and Technology  
Hyderabad, Telangana-500 068.



### DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Date: 6/2/24

#### ATTENDANCE SHEET

The following list of students attended / absent for the B.Tech  
remedial class conducted for III Year I Semester AKB Section on  
6/2/24.

S.No	Roll No's	Name of the Student	Hr - DCN	Hr - ca	Hr - mpm
		Subject	5	6	7
1	21VE1A0405	A. Sai Kiran	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
2	408				
3	410	B. Lokesh	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
4	411	Bathula. Viswasree	<u>viswasree</u>	<u>viswasree</u>	<u>viswasree</u>
5	414				
6	415	C. Jaykanth	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
7	416	D.H. Mounika	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
8	417	Shashank	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
9	418	CH. Sreeja	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
10	419	D. Charan Goud	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
11	420	D. Shrivisha	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
12	421	D. sainishanth	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
13	425	G. Charan	<u>Charan</u>	<u>Charan</u>	<u>Charan</u>
14	426	G. Preetham	<u>Preetham</u>	<u>Preetham</u>	<u>Preetham</u>
15	432				
16	434	G. Ashish	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
17	436	K. Tejashwar	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
18	438	Kalyani. B	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
19	440	Prjith Reddy	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
20	442				
21	443	M. Brinay Sureshith	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
22	444				
23	450	P. Akhilarandan	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
24	455				
25	458	Syed Axis	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
26	461				
27	462	Y. Madhu	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>
28	22VE5A0401				
29	402	A. Sai Krishna	<u>[Signature]</u>	<u>[Signature]</u>	<u>[Signature]</u>

Session Timings: 1:20 pm to 3:50 pm

Session Resource Person:

[Signature]  
Class Incharge

[Signature]  
Year Incharge

[Signature]  
Head of the Department

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEER

Date: \_\_\_\_\_  
Dr. K. SAGAR  
Principal & Professor in CSE  
Sreyas Institute of Engineering and Technology  
Hyderabad, Telangana-500 068.

ATTENDANCE SHEET

The following list of students attended / absent for the B.Tech  
remedial class conducted for III Year I Semester A & B Section on  
6/2/24.

S.No	Roll No's	Name of the Student	Hr - 2	Hr - 3	Hr - 4
		Subject	MPMC	COOS	COOS
1	21VE1A0466	Surya Bhagav	Surya	Surya	Surya
2	468	B.V.S Likhith	Likhith	COOS Likhith	COOS Likhith
3	469				
4	470	B. Sriyam	Suf	Suf	Suf
5	471				
6	472				
7	474	B. Ajay Kumar	Ajay	Ajay	Ajay
8	477				
9	478	Ch. Arohan	Arohan	Arohan	Arohan
10	479	Ch. Yashwanth	yashwanth	yashwanth	yashwanth
11	482				
12	483				
13	484				
14	487	G. Nitesh Reddy	alitesh	alitesh	alitesh
15	490	J. Abhinav	Abinav	Abinav	Abinav
16	491	T. Mahesh	Mahesh	Mahesh	Mahesh
17	493				
18	494				
19	497	K. Sai Nithin	Nithin	Nithin	Nithin
20	498				
21	499				
22	4A0	Anulani Kommoju	Anulani	Anulani	Anulani
23	4A2	Ch. Chandu Shaka	Chandu	Chandu	Chandu
24	4A3	M. Madhu Manasa	Manasa	Manasa	Manasa
25	4A4				
26	4A8	M. Vennela	Vennela	Vennela	Vennela
27	4A9	M. Koushik	Koushik	Koushik	Koushik
28	4B1				
29	4B6	Preethika Chiratta	Ch. Preethika	Ch. Preethika	Ch. Preethika
30	4B7	R. Shiva Kumar	Shiva	Shiva	Shiva
31	4B8	R. Vishwanth Rahul	Rahul	Rahul	Rahul
32	4C0				
33	4C2	E. Sriteja	Sriteja	Sriteja	Sriteja
34	4C4	T. Smitha	Smitha	Smitha	Smitha
35	4C6	V. Nithin Reddy	Nithin	Nithin	Nithin
36	4C7	Y. Vinay	Vinay	Vinay	Vinay
37	22VE5A0412	R. Shashi Kanth	Shashi	Shashi	Shashi





## LIST OF WEAK STUDENTS

S. No	Hall Ticket No.	Name	%
<b>ECE - A</b>			
1.	21VE1A0405	A. Sai kiran	
2.	409	B. Chandram	
3.	411	B. Vishwashree	
4.	414	B. Venkata Ravi Teja	
5.	415	C. Jaykanth	
6.	419	D. Charan kumar Goud	
7.	420	D. Shirisha	
8.	421	D. Sai Nishanth	
9.	432	G. kalyan Srinivas	
10.	434	G. Ashish	
11.	437	K. Vijay	
12.	443	M. Sriam Surarchith	
13.	444	M. Venkat Narayana	
14.	455	P. Akhil	
15.	461	V. Vamshidhar Reddy	
16.	22VE5A0401	A. Sai charan	
	402	A. Sai krishna	
<b>ECE - B</b>			
1.	21VE1A0469	B. Anirudh Reddy	
2.	470	B. Sriram	
3.	471	B. Naveen kumar	
4.	472	B. Akhil Teja	
5.	474	B. Ajay kumar Reddy	
6.	477	Ch. Karthik	
7.	478	Ch. Arohan	
8.	479	Ch. Yashwanth	
9.	482	D. Anjan Reddy	
10.	483	E. Ajay	
11.	492	J. Aravind	
12.	493	Joshi Chaitanya	
13.	494	K. Surya Vamshi Yadav	
14.	4A2	L. Chandra Sekhar	
15.	4A4	M. Venkata Saketh	
16.	4B1	G.N. Mahesh Yadav	





## COURSE ATTAINMENT, OBSERVATIONS & ACTION PROPOSED

CXXX	Course Outcomes	Course Attainment
C01	Understand the internal architecture & organisation of 8086 & develop ALP using various instructions.	2.83
C02	Understand the internal architecture & organisation of 8051 & develop ALP using various instructions.	2.74
C03	Able to interface the various I/O devices with 8086 & 8051.	2.92
C04	Understand the various on-board & external serial communication schemes.	2.92
C05	Understand the internal archi. & organ of ARM & develop ALP using various instructions.	2.89
C06	Understand the architecture of advanced ARM processors, CORTEX & OMAP.	2.88

CXXX	Action Proposed	Remarks





## COURSE COMPLETION CERTIFICATE

### Course Completion Certificate

I Ravali Maraju, faculty in the Dept. of Electronics and Communication Engineering has completed entire(5 Units) syllabus and the course work for the subject Microprocessors and Microcontrollers of III-year I-Semester, for the academic year **2023-24.**

**Signature of the faculty**

**HOD**

**Principal**

Course

**MICROPROCESSORS AND MICROCONTROLLERS IIIYEAR – ISEM ECE**





**COURSE MATERIAL**

**MICROPROCESSORS AND MICROCONTROLLERS IIIYEAR – ISEM ECE**

  
**Dr. K. SAGAR**  
B.E., M.Tech., Ph.D.  
Principal & Professor in CSE  
Sreyas Institute of Engineering and Technology  
Hyderabad, Telangana-500 068.



# QUESTION BANK (DESCRIPTIVE, OBJECTIVE)

MICROPROCESSORS AND MICROCONTROLLERS

III YEAR – I SEM

ECE

*K. Sagar*  
**Dr. K. SAGAR**  
B.E., M.Tech., Ph.D.  
Principal & Professor in CSE  
Sreyas Institute of Engineering and Technology  
Hyderabad, Telangana-500 068.

Mid



# ANSWER SCRIPT SAMPLES

MICROPROCESSORS AND MICROCONTROLLERS

III YEAR – I SEM

*ksm*  
**Dr. K. SAGAR**  
B.E., M.Tech., Ph.D.  
Principal & Professor in CSE  
Sreyas Institute of Engineering and Technology  
Hyderabad, Telangana-500 068.

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## PREVIOUS QUESTION PAPERS

MICROPROCESSORS AND MICROCONTROLLERS III YEAR - IS

Previo

*www*  
**Dr. K. SAGAR**  
B.E., M.Tech., Ph.D.  
Principal & Professor in CSE  
Sreyas Institute of Engineering and Technology  
Hyderabad, Telangana-500 068.



# CO ATTAINMENT SHEET

MICROPROCESSORS AND MICROCONTROLLERS III YEAR – IS

*K. Sagar*  
**Dr. K. SAGAR**  
B.E., M.Tech., Ph.D.  
Principal & Professor in CSE  
Sreyas Institute of Engineering and Technology  
Hyderabad, Telangana-500 068.

COURSE TITLE	MICROPROCESSORS AND MICROCONTROLLERS	COURSE CODE	EC501PC
NAME & DESIGNATION	RAVALI MAROJU, ASSISTANT PROFESSOR	SECTION	A & B
DEPARTMENT	ECE	REGULATION	R18
BATCH	2021-25	YEAR & SEMESTER	III-I
ACADEMIC YEAR	2023-24		

COURSE NAME	COURSE OUTCOMES										CPD	HOURS
C301.1	Understand the internal architecture and organization of 8086 and develop assembly programs using various instructions.										TL2	24
C301.2	Understand the internal architecture, organization and interrupts of 8051 and develop assembly programs using various instructions.										TL4	15
C301.3	Able to Interface the various I/O devices with 8086 and 8051.										TL4	8
C301.4	Understand the various onboard and external serial communication standards and schemes.										TL3	5
C301.5	Understand the internal architecture and organization of ARM and develop assembly programs using various instructions										TL3	15
C301.6	Understand the architecture of advanced ARM processors – CORTEX and OMAP										TL2	5

COURSE TITLE	LECTURE	TUTORIAL	PRACTICAL	HOURS	CREDITS	CO1-T	CO2-T	CO3-T	CO4-T	CO5-T	CO6-T	CO1-A	CO2-A	CO3-A	CO4-A	CO5-A	CO5-A
MICROPROCESSORS AND	4	0	0	72	4	2.76	2.76	2.76	2.76	2.76	2.76	2.83	2.74	2.92	2.92	2.89	2.88

CO PO MAPPING	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
C301.1	X	X	X	X	-	-	-	-	-	-	-	-	-	-
C301.2	X	X	X	X	-	-	-	-	-	-	-	X	X	-
C301.3	X	X	X	X	-	-	-	-	-	-	-	X	X	-
C301.4	X	X	X	X	-	-	-	-	-	-	-	X	X	-
C301.5	X	X	X	X	X	-	-	-	-	-	-	X	X	-
C301.6	X	X	X	X	X	-	-	-	-	-	-	X	X	-
C301_CO PO MAP	X	X	X	X	X	-	-	-	-	-	-	X	X	-

C_PO ATTAINMENT	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	CO_ATT
C301.1	3	1	2	1	-	-	-	-	-	-	-	-	-	-	2.83
C301.2	2	2	2	1	-	-	-	-	-	-	1	1	1	-	2.74
C301.3	2	3	2	2	-	-	-	-	-	-	-	1	1	-	2.92
C301.4	3	3	2	2	-	-	-	-	-	-	-	1	1	-	2.92
C301.5	3	3	2	1	1	-	-	-	-	-	-	1	1	-	2.89
C301.6	1	1	3	2	3	-	-	-	-	-	-	-	1	-	2.88
C301_PO MAP (L)	3	3	3	2	2	0	0	0	0	0	0	2	2	0	2.86
C301_PO_ATTAINMENT	2.86	2.87	2.86	1.92	1.92	0.00	0.00	0.00	0.00	0.00	0.00	1.91	1.91	0.00	

